Dual 550kHz Synchronous Switching Regulator Controller with 5-Bit VID and 150mA LDO

FEATURES

- **Three Regulated Outputs: Core, I/O and CLK in One Package**
- **Integrated Intel Mobile 5-Bit VID DAC**
- **No External Current Sense Resistors**
- All N-Channel External MOSFET Architecture
- 550kHz Switching Frequency Minimizes External Component Size and Cost
- Integrated 150mA LDO Linear Regulator
- Excellent DC Accuracy: 1.25% for Core, 2% for I/O and CLK Supplies
- PGOOD Flag Monitors All Three Outputs
- High Efficiency Over Wide Load Current Range
- Low Shutdown Current: < 100µA
- Switchers Run Out-of-Phase to Minimize C_{IN}
- Small 28-Pin Narrow SSOP Package

APPLICATIONS

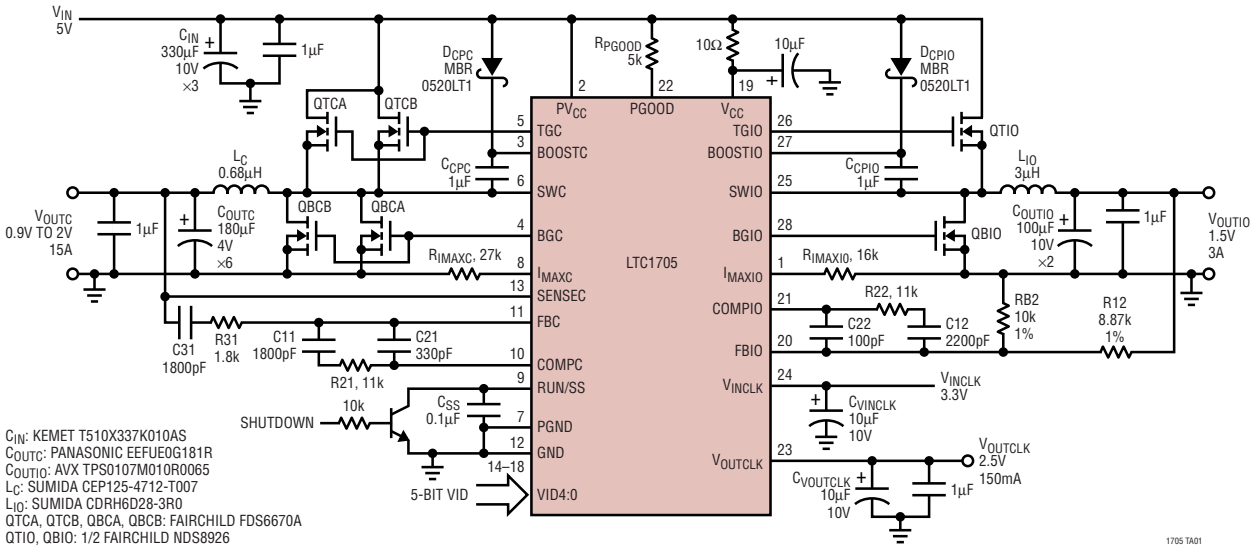
- **Complete Power Supply Controller for Intel Mobile Pentium® Processors**
- Intel Mobile Pentium Core, I/O, Clock Supplies
- Multiple Logic Supply Generator

DESCRIPTION

The LTC®1705 is a complete power supply controller for Intel Mobile Pentium processors. It includes two switching regulator controllers, each designed to drive a pair of N-channel MOSFETs in a voltage mode feedback, synchronous buck configuration, to provide the core and I/O supplies. The core controller includes a 5-bit DAC that conforms to the Intel Mobile VID specification. The IC also includes a low dropout linear regulator (LDO) that delivers up to 150mA of output current to provide the CLK supply. The LTC1705 uses a constant-frequency 550kHz PWM architecture, minimizing external component size and cost, as well as optimizing load transient performance. It provides better than 1.25% DC accuracy at its core output, and 2% at I/O and CLK outputs. The high performance feedback loops allow the circuit to keep total output regulation within ±5% under all transient conditions. An open-drain PGOOD flag indicates that all three outputs are within ±10% of their regulated values. A shutdown circuit disables all three outputs if the RUN/SS pin is pulled to ground. In this mode, the LTC1705 supply current drops to below 100µA.

TYPICAL APPLICATION

Intel Mobile Pentium VRM Supply



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC}, PV_{CC}, V_{INCLK} 6V
- BOOSTC, BOOSTIO 12V
- BOOSTC – SWC, BOOSTIO – SWIO 6V

Input Voltage
- SWC, SWIO ..... –1V to 6V
- SENSEC, FBC, FBIO, VID*n* ..... –0.3V to (V_{CC} + 0.3V)
- PGOOD, RUN/SS,
- I_{MAXC}, I_{MAXIO} ..... –0.3V to (V_{CC} + 0.3V)

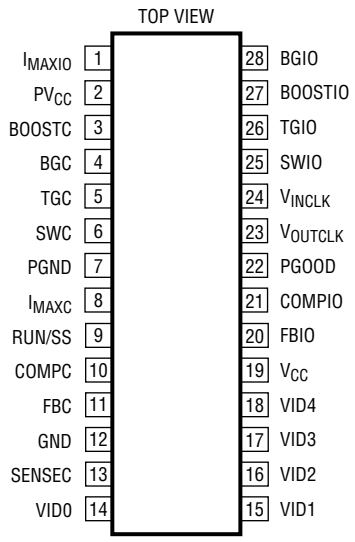
Peak Output Current <10µs
- TGC, BGC 5A
- TGIO, BGIO 1.25A

Operating Temperature Range (Note 2) .. –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 80°C/W

ORDER PART NUMBER
LTC1705EGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = PV_{CC} = BOOST = 5V, V_{INCLK} = 3.3V unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Supply Voltage		●	3.15	5	5.5	V
PV_{CC}	PV_{CC} Supply Voltage	(Note 4)	●	3.15	5	5.5	V
BV_{CC}	BOOST Pin Voltage	V_{BOOST} – V_{SW} (Note 4)	●	3.15	5	5.5	V
V_{INCLK}	V_{INCLK} Supply Voltage		●	3	3.3	5.5	V
I_{VCC}	V_{CC} Supply Current	Test Circuit 1 RUN/SS = 0V	● ●		4.5 40	8 100	mA µA
I_{PVCC}	PV_{CC} Supply Current	V_{SENSEC} = V_{FBIO} = 0V, No Load at Drivers (Note 5) RUN/SS = 0V (Note 6)	● ●		2 1	6 50	mA µA
I_{BOOST}	I_{BOOSTC} + $I_{BOOSTIO}$	V_{SENSEC} = V_{FBIO} = 0V, No Load at Drivers (Note 5) RUN/SS = 0V (Note 6)	● ●		2 1	6 50	mA µA
I_{VINCLK}	V_{INCLK} Supply Current	$I_{VOUTCLK}$ = 0mA RUN/SS = 0V	● ●		1 4	1.5 30	mA µA
V_{SHDN}	RUN/SS Shutdown Threshold	$V_{RUN/SS}$ ↑ (Rising Edge)	●	0.2	0.5		V
I_{SS}	RUN/SS Source Current	RUN/SS = 0V			–3		µA
Core, I/O Supply Control Loops							
V_{SENSEC}	Output Voltage Accuracy	Programmed from 0.9V to 2V	●	–1.25		1.25	%
V_{FBC}	Core Feedback Voltage	(Note 10)			0.800		V
V_{FBIO}	I/O Feedback Voltage		●	0.784	0.800	0.816	V
dV_{FB}	Feedback Voltage Line Regulation	V_{CC} = 3.3V to 5.5V	●		±0.01	±0.1	%/V
dV_{OUT}	Output Voltage Load Regulation	(Note 7)	●	–0.2	–0.1		%
I_{FBIO}	I/O Feedback Input Current		●			±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = PV_{CC} = BOOST = 5V, V_{INCLK} = 3.3V unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{FB}	Feedback Amplifier DC Gain		●	74	85		dB
GBW	Feedback Amplifier Gain Bandwidth Product	f = 100kHz (Note 7)			20		MHz
I_{COMP}	Feedback Amplifier Output Sink/Source Current		●	±3	±10		mA
V_{PGOOD}	Negative Power Good Threshold Positive Power Good Threshold	Relative to Nominal Output Voltage	● ●	–15 6	–10 10	–6 15	% %
A_{ILIM}	Current Limit Amplifier DC Gain		●	40	60		dB
I_{IMAX}	I_{MAX} Source Current	V_{IMAXC} = V_{IMAXIO} = 0V	●	–12	–10	–8	µA
Core, I/O Supply Switching Characteristics							
f_{OSC}	Oscillator Frequency	Test Circuit 1	●	460	550	650	kHz
Φ_{OSC}	Core and I/O Oscillator Phase Difference	(Note 7)			180		DEG
DC_{MAX}	Maximum Duty Cycle		●	87	90	93	%
t_{NOV}	Driver Nonoverlap	Test Circuit 1, 50% to 50%	●	10	25	120	ns
t_r, t_f	Driver Rise/Fall Time	Test Circuit 1, 10% to 90%	●		15	100	ns
Clock Supply Output							
V_{OUTCLK}	CLK Output Voltage	$I_{VOUTCLK}$ = 0mA	●	2.45	2.50	2.55	V
dV_{OUTCLK}	Output Voltage Line Regulation	V_{INCLK} = 3.0V to 5.5V	●		±0.02	±0.1	%/V
	Output Voltage Load Regulation	$I_{VOUTCLK}$ = 0mA to 150mA	●	–0.1	–0.05		%
ILM_{CLK}	CLK Output Short-Circuit Current	$I_{VOUTCLK}$ = 0V	●		–240	–150	mA
$V_{DROPOUT}$	CLK Output Dropout Voltage	$I_{VOUTCLK}$ = 150mA, $d_{VOUTCLK}$ = –1% (Note 8)	●		0.3	0.5	V
V_{PGOOD}	Negative V_{OUTCLK} Power Good Threshold Positive V_{OUTCLK} Power Good Threshold	Relative to V_{OUTCLK} Relative to V_{OUTCLK}	● ●	–15 6	–10 10	–6 15	% %
VID Inputs							
R1	Resistance Across SENSEC and FBC				10		kΩ
R_{VID}	VID Input Pull-Up Resistance	(Note 9)			30		kΩ
V_{VID}	VID Input Threshold		●	0.4		1.6	V
PGOOD							
I_{PGOOD}	V_{PGOOD} Sink Current	Power Good Power Bad	● ●	 10		10	µA mA
V_{OLPG}	PGOOD Output Low Voltage	I_{PGOOD} = 1mA	●		0.03	0.1	V
T_{PGOOD}	V_{PGOOD} Falling Edge Delay V_{PGOOD} Rising Edge Delay V_{PBAD} Pulse	 VID Code Change	● ● ●	2 10 10	4 20 20	8 40 40	µs µs µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1705 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: PV_{CC} and BV_{CC} (V_{BOOST} – V_{SW}) must be greater than $V_{GS(ON)}$ of the external MOSFETs to ensure proper operation.

Note 5: Supply current in normal operation is dominated by the current needed to charge and discharge the capacitance of the external MOSFET gates. This current varies with supply voltage and the choice of external MOSFETs.

Note 6: Supply current in shutdown is dominated by external MOSFET leakage and may be significantly higher than the quiescent current drawn by the LTC1705, especially at elevated temperature.

Note 7: Guaranteed by design, not subject to test.

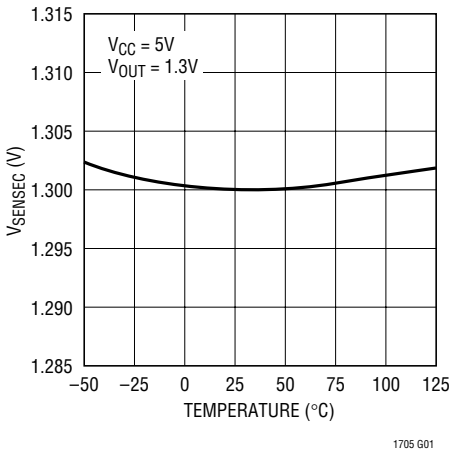
Note 8: Dropout voltage is the minimum input-to-output voltage differential required to maintain regulation at the specified output current. In dropout, the output voltage will be equal to V_{INCLK} – $V_{DROPOUT}$.

Note 9: Each internal pull-up resistor attached to the VID inputs has a series diode connected to V_{CC} to allow input voltages higher than the V_{CC} supply without damage or clamping. (See Block Diagram.)

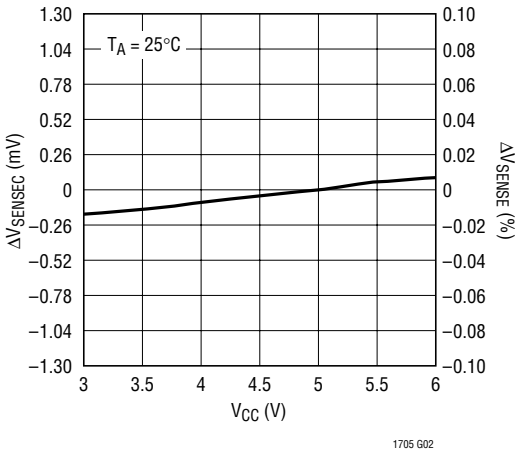
Note 10: The core feedback voltage accuracy is guaranteed by the V_{SENSE} output voltage accuracy test.

TYPICAL PERFORMANCE CHARACTERISTICS

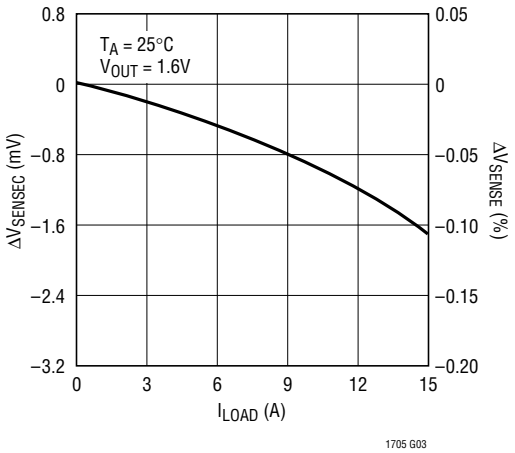
V_{SENSEC} vs Temperature



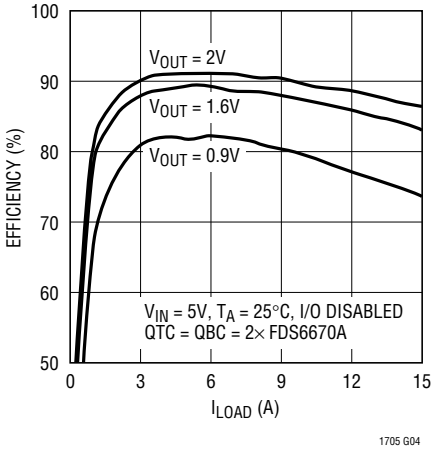
V_{SENSEC} Line Regulation



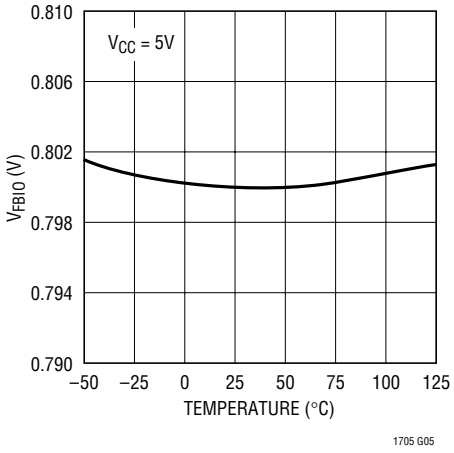
V_{SENSEC} Load Regulation



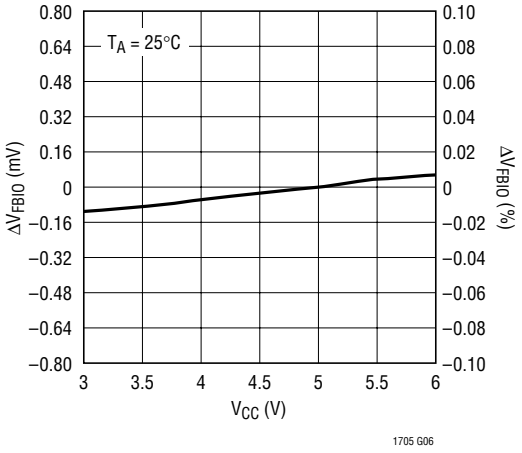
Core Supply Efficiency



V_{FBIO} vs Temperature

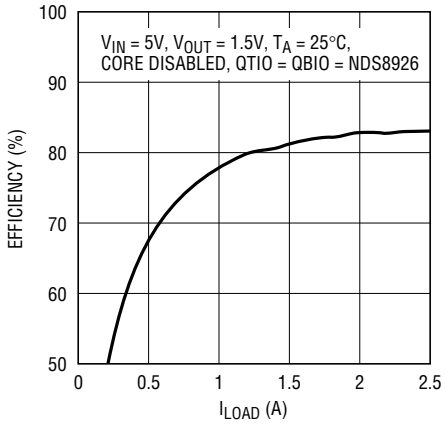


V_{FBIO} Line Regulation



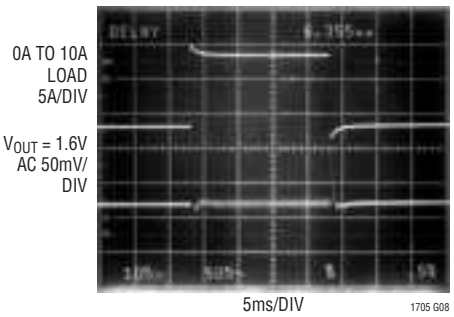
TYPICAL PERFORMANCE CHARACTERISTICS

I/O Supply Efficiency



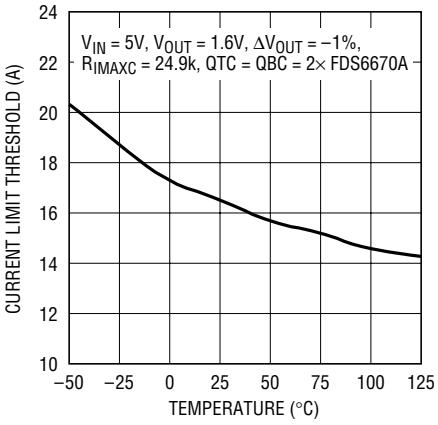
1705 G07

V_{OUTC} 0A To 10A Load Step



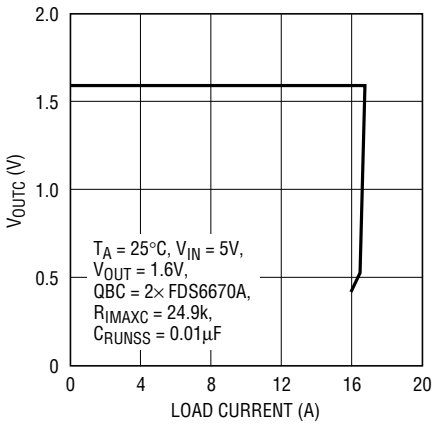
1705 G08

Current Limit Threshold vs Temperature



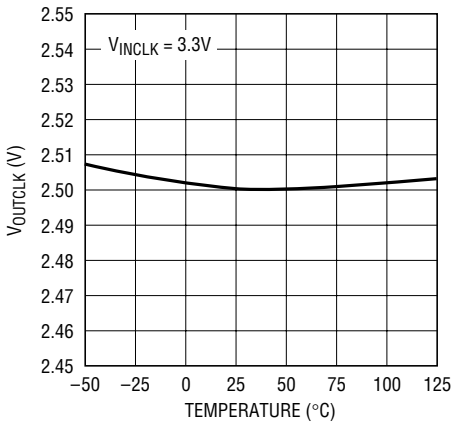
1705 G09

V_{OUTC} vs Load Current



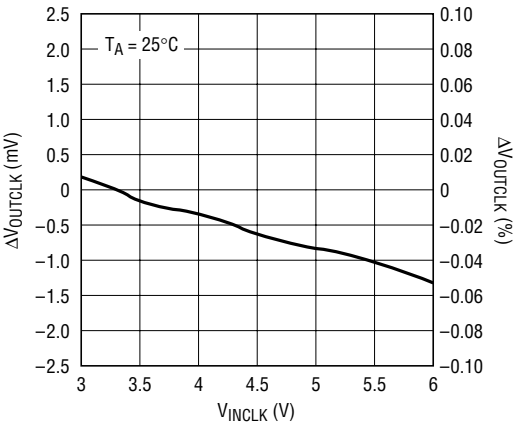
1705 G10

V_{OUTCLK} vs Temperature



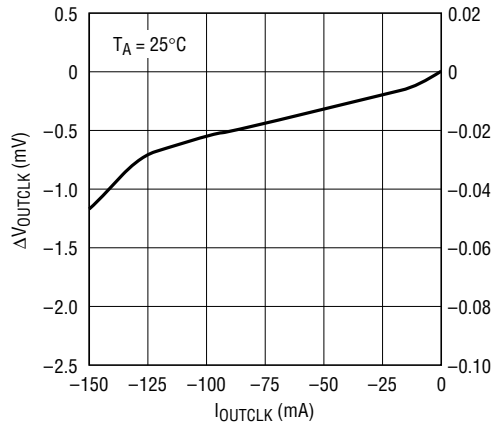
1705 G11

V_{OUTCLK} Line Regulation



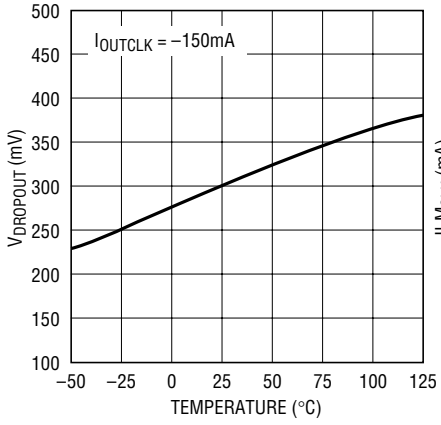
1705 G12

V_{OUTCLK} Load Regulation



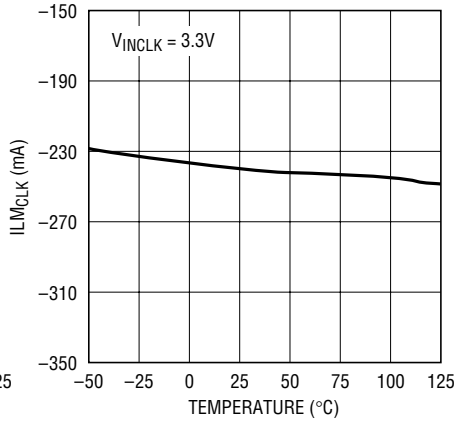
1705 G13

V_{OUTCLK} Dropout Voltage vs Temperature



1705 G14

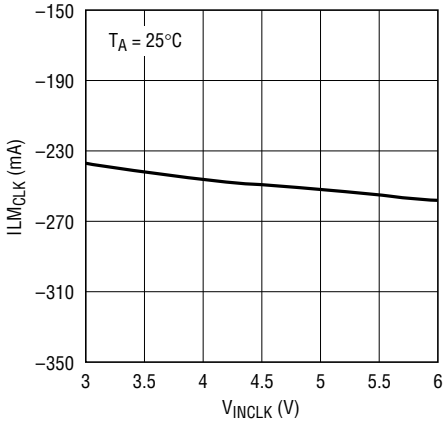
V_{OUTCLK} Short-Circuit Current vs Temperature



1705 G15

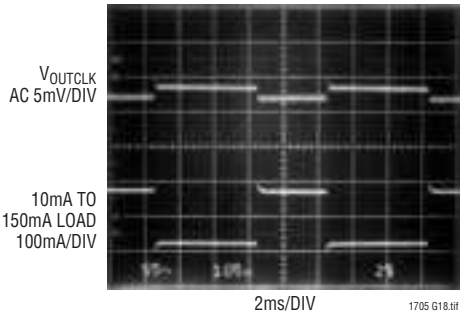
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUTCLK} Short-Circuit Current vs V_{INCLK}



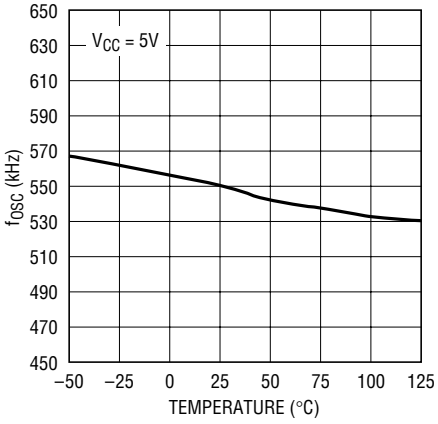
1705 G16

V_{OUTCLK} 10mA To 150mA Load Step



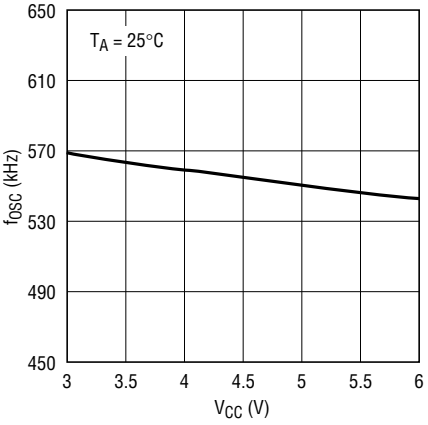
1705 G18.tif

f_{OSC} vs Temperature



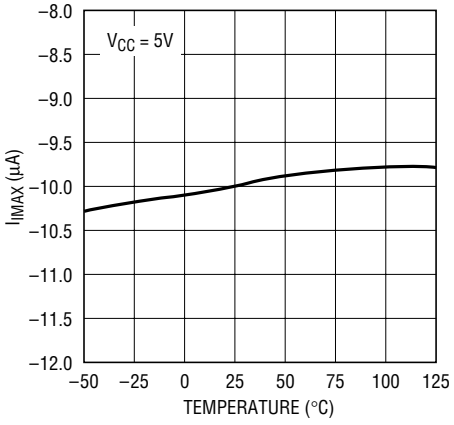
1705 G19

f_{OSC} vs V_{CC}



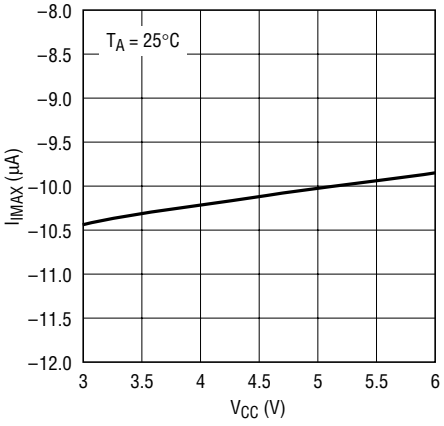
1705 G20

I_{IMAX} vs Temperature



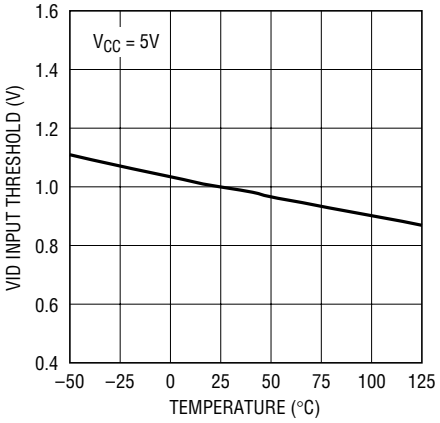
1705 G21

I_{IMAX} vs V_{CC}



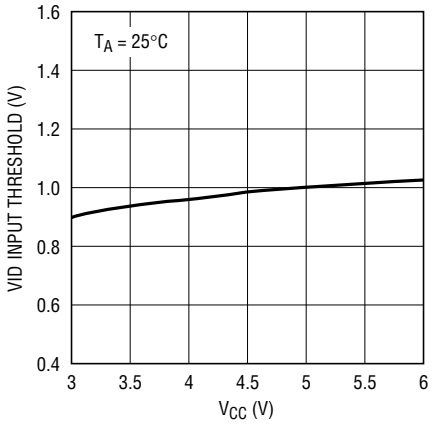
1705 G22

VID Input Threshold vs Temperature



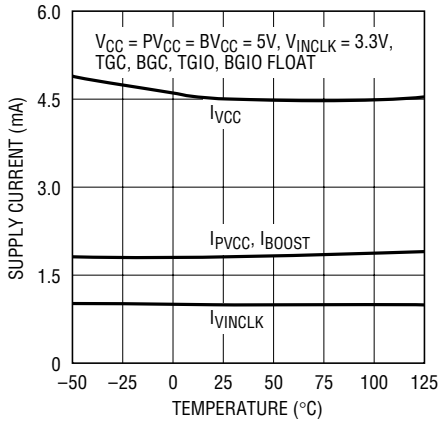
1705 G23

VID Input Threshold vs V_{CC}



1705 G24

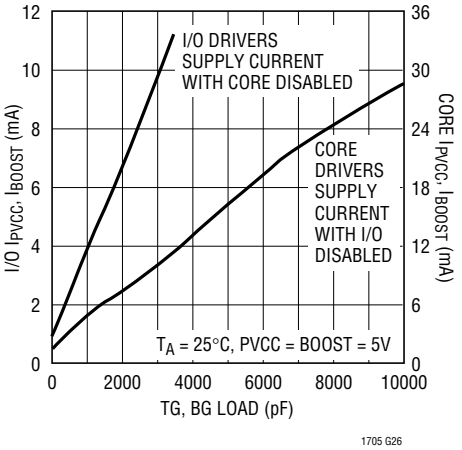
Supply Current vs Temperature



1705 G25

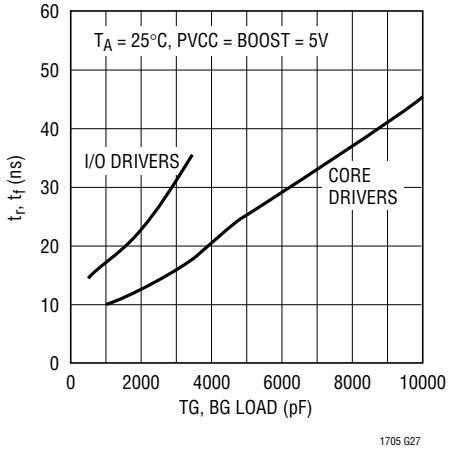
TYPICAL PERFORMANCE CHARACTERISTICS

I_{PVCC}, I_{BOOST} vs Driver Load



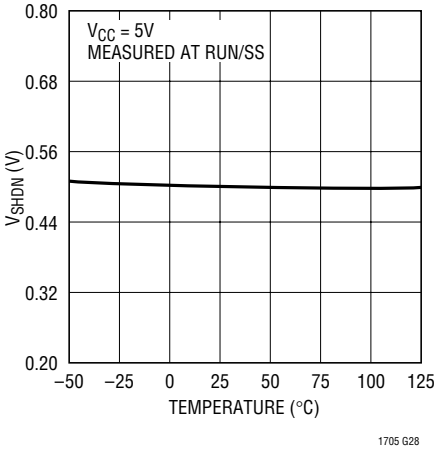
1705 G26

Drivers Rise and Fall Time vs Load



1705 G27

V_{SHDN} vs Temperature



1705 G28

PIN FUNCTIONS

I_{MAXIO} (Pin 1): I/O Supply Current Limit Set. The I_{MAXIO} pin sets the current limit comparator threshold for the I/O controller. If the voltage drop across the bottom MOSFET, QBIO, exceeds the magnitude of the voltage at I_{MAXIO}, the I/O controller enters current limit. The I_{MAXIO} pin has an internal 10µA current source pull-up, allowing the current threshold to be set with a single external resistor to PGND. Kelvin connect this current setting resistor to the source of QBIO. Refer to the Current Limit Programming section for more information on choosing the value of R_{IMAX}.

PV_{CC} (Pin 2): Driver Power Supply Input. PV_{CC} provides power to the BGC and BGIO output drivers. PV_{CC} must be connected to a voltage high enough to fully turn on the external MOSFETs QBC and QBIO. PV_{CC} should generally be connected directly to V_{IN}, the main system 5V supply. PV_{CC} requires at least a 10µF bypass capacitor directly to PGND.

BOOSTC (Pin 3): Core Controller Top Gate Driver Supply. The BOOSTC pin supplies power to the floating TGC driver. Bypass BOOSTC to SWC with a 1µF capacitor. An external schottky diode from V_{IN} to BOOSTC creates a complete floating charge-pumped supply at BOOSTC. No other external supplies are required.

BGC (Pin 4): Core Supply Bottom Gate Drive. The BGC pin drives the gate of the bottom N-channel synchronous switch MOSFET, QBC. BGC is designed to typically drive up to 10,000pF of gate capacitance. If RUN/SS goes low, BGC goes low, turning off QBC.

TGC (Pin 5): Core Supply Top Gate Drive. The TGC pin drives the gate of the top N-channel MOSFET, QTC. The TGC driver draws power from the BOOSTC pin and returns it to the SWC pin, providing true floating drive to QTC. TGC is designed to typically drive up to 10,000pF of gate capacitance. If RUN/SS goes low, TGC goes low, turning off QTC.

SWC (Pin 6): Core Supply Switching Node. Connect SWC to the switching node of the core converter. The TGC driver ground returns to SWC, providing floating gate drive to the top N-channel MOSFET switch, QTC. The voltage at SWC is compared to I_{MAXC} by the current limit comparator while the bottom MOSFET, QBC, is on.

PGND (Pin 7): Power Ground. The BGC and BGIO drivers return to this pin. Connect PGND to a high-current ground node in close proximity to the sources of external MOSFETs QBC and QBIO, and the V_{IN} and V_{OUT} bypass capacitors.

I_{MAXC} (Pin 8): Core Supply Current Limit Set. See I_{MAXIO}.

PIN FUNCTIONS

RUN/SS (Pin 9): SoftStart. Pulling RUN/SS to GND externally shuts down the LTC1705 and turns off all the external MOSFET switches. The quiescent supply current drops below 100μA. A capacitor from RUN/SS to GND controls the turn on time and rate of rise of the core and I/O output voltages at power up. An internal 3μA current source pull-up at RUN/SS sets the turn-on time at approximately 300ms/μF.

COMPC (Pin 10): Core Controller Loop Compensation. The COMPC pin is connected directly to the output of the Core controller's error amplifier and the input of the PWM comparator. Use an RC network between the COMPC pin and the FBC pin to compensate the feedback loop for optimum transient response.

FBC (Pin 11): Core Controller Feedback Input. Connect the loop compensation network for the core controller to FBC. FBC internally connects to the VID resistor network to set the Core output voltage.

GND (Pin 12): Signal Ground. All internal low power circuitry returns to the GND pin. Connect to a low impedance ground, separated from the PGND node. All feedback, compensation and softstart connections should return to GND. GND and PGND should connect only at a single point, near the PGND pin and the negative plate of the V_{IN} bypass capacitor.

SENSEC (Pin 13): Core Controller Output Sense. Connect to V_{OUTC}.

VID0 to VID4 (Pins 14 to 18): VID Programming Inputs. These are logic inputs that set the output voltage at the Core supply to a preprogrammed value (see Table 1). VID4 is the MSB, VID0 is the LSB. The codes selected by the VID inputs correspond to the Intel Mobile VID specification. Any VID code transition forces PGOOD to go low for 20μs. Each VID pin includes an on-chip 30k pull-up resistor in series with a diode (see Block Diagram).

V_{CC} (Pin 19): Power Supply Input. All internal circuits except the output drivers are powered from this pin. Connect V_{CC} to a low-noise 5V supply and bypass the pin to GND with at least a 10μF capacitor in close proximity to the LTC1705.

FBIO (Pin 20): I/O Controller Feedback Input. Connect FBIO through a resistor divider network to V_{OUTIO} to set the output voltage. Also, connect the loop compensation network for the I/O controller to FBIO.

COMPIO (Pin 21): I/O Controller Loop Compensation. See COMPC.

PGOOD (Pin 22): Power Good. PGOOD is an open-drain logic output. PGOOD pulls low if any of the three supply outputs are out of regulation (see Electrical Characteristics table for Core, I/O and CLK thresholds). An external pull-up resistor is required at PGOOD to allow it to swing positive.

V_{OUTCLK} (Pin 23): Clock Supply Output. V_{OUTCLK} is the output node of the internal linear clock supply regulator. V_{OUTCLK} provides up to 150mA at the 2.5V output to power the CPU CLK supply. Bypass V_{OUTCLK} with at least a 2.2μF capacitor to GND (refer to the V_{CLK} Linear Regulator section). If RUN/SS goes low, the V_{OUTCLK} regulator shuts down.

V_{INCLK} (Pin 24): Clock Supply Input. V_{INCLK} is the input terminal to the internal linear CLK supply regulator. Connect V_{INCLK} to a 3.3V supply to maximize efficiency. V_{INCLK} can be connected to the 5V supply, but the efficiency of the V_{OUTCLK} regulator is reduced. Bypass V_{INCLK} with a 10μF capacitor to GND.

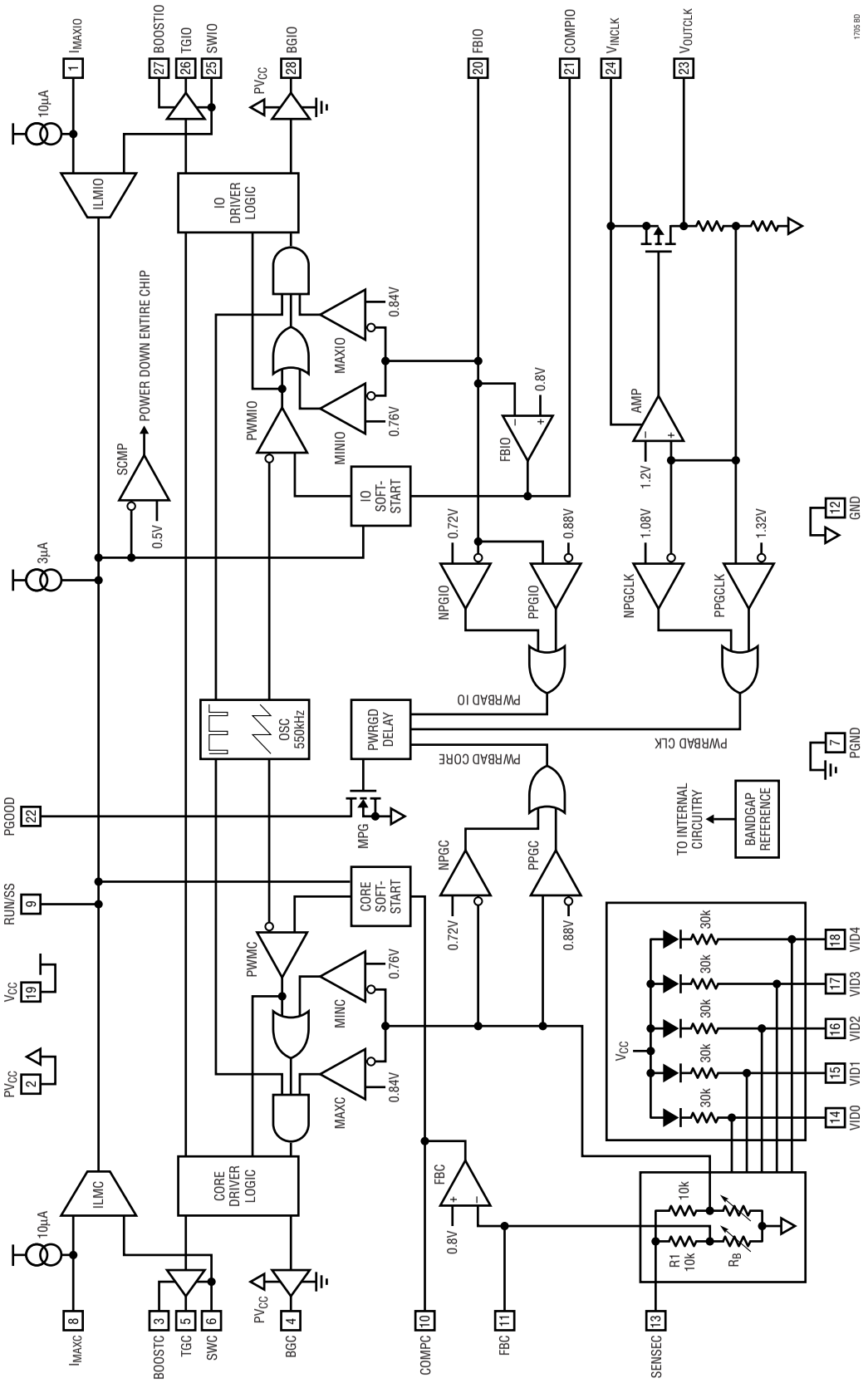
SWIO (Pin 25): I/O Controller Switching Node. See SWC.

TGIO (Pin 26): I/O Controller Top Gate Drive. See TGC. TGIO is designed to typically drive up to 2,000pF of gate capacitance.

BOOSTIO (Pin 27): I/O Controller Top Gate Driver Power. See BOOSTC.

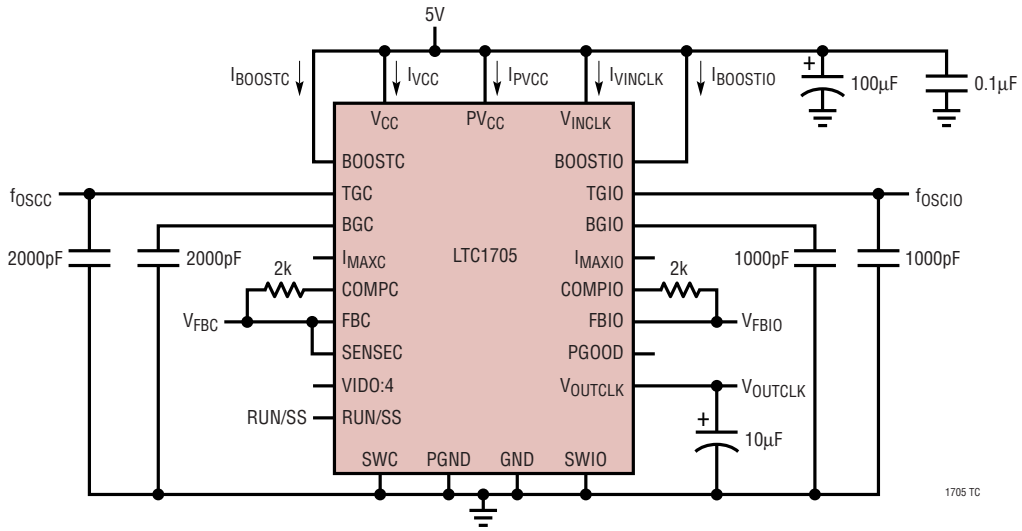
BGIO (Pin 28): I/O Controller Bottom Gate Drive. See BGC. BGIO is designed to typically drive up to 2,000pF of gate capacitance.

BLOCK DIAGRAM



TEST CIRCUIT

Test Circuit 1



VID PROGRAMMING CODES

Table 1. VID Inputs and Corresponding Core Output Voltages

CODE	VID4	VID3	VID2	VID1	VID0	V_{OUTC}
00000	Gnd	Gnd	Gnd	Gnd	Gnd	2.00V
00001	Gnd	Gnd	Gnd	Gnd	Float	1.95V
00010	Gnd	Gnd	Gnd	Float	Gnd	1.90V
00011	Gnd	Gnd	Gnd	Float	Float	1.85V
00100	Gnd	Gnd	Float	Gnd	Gnd	1.80V
00101	Gnd	Gnd	Float	Gnd	Float	1.75V
00110	Gnd	Gnd	Float	Float	Gnd	1.70V
00111	Gnd	Gnd	Float	Float	Float	1.65V
01000	Gnd	Float	Gnd	Gnd	Gnd	1.60V
01001	Gnd	Float	Gnd	Gnd	Float	1.55V
01010	Gnd	Float	Gnd	Float	Gnd	1.50V
01011	Gnd	Float	Gnd	Float	Float	1.45V
01100	Gnd	Float	Float	Gnd	Gnd	1.40V
01101	Gnd	Float	Float	Gnd	Float	1.35V
01110	Gnd	Float	Float	Float	Gnd	1.30V
01111*	Gnd	Float	Float	Float	Float	1.25V
10000	Float	Gnd	Gnd	Gnd	Gnd	1.275V
10001	Float	Gnd	Gnd	Gnd	Float	1.250V
10010	Float	Gnd	Gnd	Float	Gnd	1.225V
10011	Float	Gnd	Gnd	Float	Float	1.200V
10100	Float	Gnd	Float	Gnd	Gnd	1.175V
10101	Float	Gnd	Float	Gnd	Float	1.150V
10110	Float	Gnd	Float	Float	Gnd	1.125V
10111	Float	Gnd	Float	Float	Float	1.100V
11000	Float	Float	Gnd	Gnd	Gnd	1.075V
11001	Float	Float	Gnd	Gnd	Float	1.050V
11010	Float	Float	Gnd	Float	Gnd	1.025V
11011	Float	Float	Gnd	Float	Float	1.000V
11100	Float	Float	Float	Gnd	Gnd	0.975V
11101	Float	Float	Float	Gnd	Float	0.950V
11110	Float	Float	Float	Float	Gnd	0.925V
11111*	Float	Float	Float	Float	Float	0.900V

*01111 and 11111 are defined by Intel to signify “no CPU.” The LTC1705 generates the output voltages shown if these codes are selected.

APPLICATIONS INFORMATION

The LTC1705 includes two, step-down (buck), voltage mode feedback switching regulator controllers and a low dropout linear regulator. The three outputs are designed to power the core, I/O and CLK supplies of an Intel Mobile Pentium system. Each switching regulator controller employs a synchronous switching architecture with two external N-channel MOSFETs per channel. The chip operates from a low voltage input supply (6V maximum) and provides high power, high efficiency, precisely regulated output voltages. Several features make the LTC1705 particularly suited for microprocessor supply regulation. Output regulation at the core supply is extremely tight, with initial accuracy and DC line and load regulation better than 1.25%. Total regulation including transient response is inside of 3.5% with a properly designed circuit. The 550kHz switching frequency and the high speed internal feedback amplifiers allow the use of physically small, low value external components without compromising performance. An onboard 5-bit DAC sets the core output voltage, consistent with the Intel Mobile VID specification (Table 1).

The 800mV internal reference allows regulated output voltages as low as 800mV without external level shifting amplifiers. The linear regulator controls an internal P-channel MOSFET that can provide more than 150mA of current at an output voltage of 2.5V. A power good (PGOOD) flag goes high when all the three outputs are in regulation.

2-Step Conversion

"2-step" architectures use a primary regulator to convert the input power source (batteries or AC line voltage) to an intermediate supply voltage, often 5V. This intermediate voltage is then converted to the low voltage, high current supplies required by the system using a secondary regulator, such as the LTC1705. 2-step conversion eliminates the need for a single converter to convert a high input voltage to a very low output voltage, often an awkward design challenge. It also fits naturally into systems that continue to use the 5V supply to power portions of their circuitry or have excess 5V capacity available as newer circuit designs shift the current load to lower voltage supplies.

Each regulator in a typical 2-step system maintains a relatively low step-down ratio (5:1 or less), running at high efficiency while maintaining reasonable duty cycle. In contrast, a regulator converting in a single step from a high input voltage to a 1.xV output must operate at a very narrow duty cycle, mandating trade-offs in external component values while compromising efficiency and transient response. The efficiency loss can exceed that of a 2-step solution. Further complicating the calculation is the fact that many systems draw a significant fraction of their total power off the intermediate 5V supply, bypassing the low voltage supply. 2-step solutions using the LTC1705 usually match or exceed the total system efficiency of single-step solutions and provide the additional benefits of improved transient response, reduced PCB area and simplified power trace routing.

2-step regulation can also buy advantages in thermal management. Power dissipation in the LTC1705 portion of a 2-step circuit is lower than it would be in a typical 1-step converter, even in cases where the 1-step converter has higher total efficiency than the 2-step system. In a typical microprocessor core supply regulator, for example, the regulator is usually located directly next to the CPU. In a 1-step design, all of the power dissipated by the core regulator is located next to the already hot CPU, aggravating thermal management. In a 2-step LTC1705 design, a significant percentage of the power lost in the core regulation system happens in the 5V supply, which is usually located away from the CPU. The power lost to heat in the LTC1705 section of the system is relatively low, minimizing the added heat near the CPU.

Fast Transient Response

The LTC1705 core and I/O supplies use fast 20MHz GBW op amps as error amplifiers. This allows the compensation network to be designed with several poles and zeros in a more flexible configuration than with typical gm feedback amplifiers. The high bandwidth of the amplifier, coupled with the high 550kHz switching frequency and the low values of the external inductor and output capacitor, allow very high loop cross-over frequencies. Additionally, a typical LTC1705 circuit uses an inductor value on the order of 1μH, allowing very fast di/dt slew rates. The result is superior transient response compared with conventional solutions.

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High Efficiency

The LTC1705 core and I/O supplies use a synchronous step-down (buck) architecture, with two external N-channel MOSFETs per output. A floating topside driver and a simple external charge pump provide full gate drive to each upper MOSFET. The voltage mode feedback loops and MOSFET V_{DS} current limit sensing circuits remove the need for external current sense resistors, eliminating external components and the corresponding power losses in the high current paths. Properly designed circuits using low gate charge MOSFETs are capable of efficiencies exceeding 90% over a wide range of output voltages and load currents.

VID Programming

The LTC1705 includes an onboard feedback network that programs the core output voltage in accordance with the Intel Mobile VID specification (Table 1). This network includes a 10k resistor connected between SENSEC and FBC and a variable value resistor connected between FBC and GND, with the value set by the digital code present at the VID4:0 pins. Connect SENSEC to V_{OUTC} to allow the network to monitor the output voltage. No additional feedback components are required to set the output voltage of the core controller, although loop compensation components are still required. Each VID*n* pin includes an internal 30k pull-up resistor, allowing it to float high if left unconnected. The pull-up resistors connect to V_{CC} through diodes (see Block Diagram), allowing the VID*n* pins to be pulled above V_{CC} without damage.

Note that codes 01111 and 11111, defined by Intel to indicate "no CPU present," do generate output voltages at V_{OUTC} (1.25V and 0.9V, respectively). Also, note that the I/O and CLK outputs on the LTC1705 are not connected to the VID circuitry and work independently from the core controller.

Linear Regulator and Thermal Shutdown

The LTC1705 CLK output is an easy to use monolithic LDO. The V_{INCLK} pin powers the regulator and an internal P-channel MOS transistor provides the output current at the 2.5V output. An external 10µF capacitor frequency compensates the linear regulator feedback loop. The CLK output is short-circuit protected and the built-in thermal shutdown circuit turns off all three regulator outputs should the LTC1705 junction temperature exceed 155°C.

SWITCHING ARCHITECTURE DETAILS

The LTC1705 dual switching regulator controller includes two independent regulator channels. The two switching regulator controllers and their corresponding external components act independently of each other with the exception of the common input bypass capacitor. The RUN/SS and PGOOD pins also affect both channels. In the following discussions, when a pin is referred to without mentioning which side is involved, that discussion applies equally to both sides.

Switching Architecture

Each half of the LTC1705 is designed to operate as a synchronous buck converter (Figure 1). Each channel includes two high power MOSFET gate drivers to control external N-channel MOSFETs QT and QB. The core drivers have 0.5Ω output impedances and can carry well over an amp of continuous current with peak currents up to 5A to slew large MOSFET gates quickly. The I/O drivers have 2Ω output impedances. The external MOSFETs are connected with the drain of QT attached to the input supply and the source of QT at the switching node SW. QB is the synchronous rectifier with its drain at SW and its source at PGND. SW is connected to one end of the inductor, with the other end connected to V_{OUT}. The output capacitor is connected from V_{OUT} to PGND.

When a switching cycle begins, QB is turned off and QT is turned on. SW rises almost immediately to V_{IN} and the inductor current begins to increase. When the PWM pulse finishes, QT turns off and one nonoverlap interval later, QB turns on. Now SW drops to PGND and the inductor current decreases. The cycle repeats with the next tick of the master clock. The percentage of time spent in each mode is controlled by the duty cycle of the PWM signal, which in turn is controlled by the feedback amplifier. The master clock runs at a 550kHz rate and turns QT on once every 1.8µs. In a typical application with a 5V input and a 1.5V

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output, the duty cycle will be set at 1.5/5 • 100% or 30% by the feedback loop. This will give roughly a 540ns on-time for QT and a 1.26µs on-time for QB.

This constant frequency operation brings with it a couple of benefits. Inductor and capacitor values can be chosen with a precise operating frequency in mind and the feedback loop components can be similarly tightly specified. Noise generated by the circuit will always be in a known frequency band with the 550kHz frequency designed to leave the 455kHz IF band free of interference. Subharmonic oscillation and slope compensation, common headaches with constant frequency current mode switchers, are absent in voltage mode designs like the LTC1705.

During the time that QT is on, its source (the SW pin) is at V_{IN}. V_{IN} is also the power supply for the LTC1705. However, QT requires $V_{IN}+V_{GS(ON)}$ at its gate to achieve minimum R_{ON}. This presents a problem for the LTC1705—it needs to generate a gate drive signal at TG higher than its highest supply voltage. To accomplish this, the TG driver runs from floating supplies, with its negative supply attached to SW and its power supply at BOOST. This allows it to slew up and down with the source of QT. In combination with a simple external charge pump (Figure 2), this allows the LTC1705 to completely enhance the gate of QT without requiring an additional, higher supply voltage.

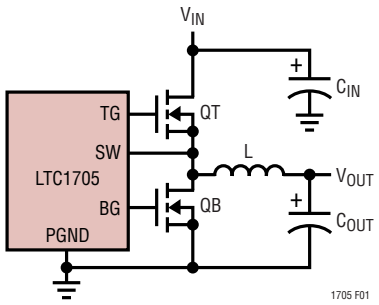

Figure 1. Synchronous Buck Architecture

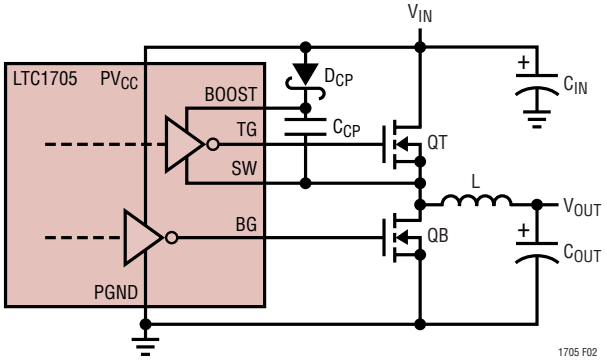

Figure 2. Floating TG Driver Supply

The two channels of the LTC1705 run from a common clock, with the phasing chosen to be 180° from the core side to the I/O side. This has the effect of doubling the frequency of the switching pulses seen by the input bypass capacitor, lowering the RMS current seen by the capacitor and reducing the value required.

Feedback Amplifier

Each side of the LTC1705 senses the output voltage at V_{OUT} with an internal feedback op amp (see Block Diagram). This is a real op amp with a low impedance output, 85dB open-loop gain and 20MHz gain bandwidth product. The positive input is connected internally to an 800mV reference, while the negative input is connected to the FB pin. The output is connected to COMP, which is in turn connected to the soft-start circuitry and from there to the PWM generator.

Unlike many regulators that use a resistor divider connected to a high impedance feedback input, the LTC1705 is designed to use an inverting summing amplifier topology with the FB pin configured as a virtual ground. This allows flexibility in choosing pole and zero locations not available with simple gm configurations. In particular, it allows the use of "Type 3" compensation, which provides a phase boost at the LC pole frequency and significantly improves loop phase margin (see Figure 3). Note that the core side of the LTC1705 includes R1 and R_B internally as part of the VID DAC circuitry.

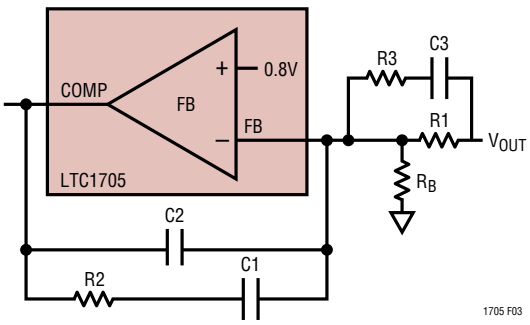

Figure 3. "Type 3" Feedback Loop (I/O Channel)

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MIN/MAX Comparators

Two additional feedback loops keep an eye on the main feedback amplifier and step in if the feedback node moves ±5% from its nominal 800mV value. The MAX comparator (see Block Diagram) activates if FB rises more than 5% above 800mV. It immediately turns the top MOSFET (QT) off and the bottom MOSFET (QB) on and keeps them that way until FB falls back within 5% of its nominal value. This pulls the output down as fast as possible, preventing damage to the (often expensive) load. If FB rises because the output is shorted to a higher supply, QB will stay on until the short goes away, the higher supply current limits or QB dies trying to save the load. This behavior provides maximum protection against overvoltage fault at the output, while allowing the circuit to resume normal operation when the fault is removed.

The MIN comparator (see Block Diagram) trips if FB is more than 5% below 800mV and immediately forces the switch duty cycle to 90% to bring the output voltage back into range. It releases when FB is within the 5% window. MIN is disabled when the soft-start or current limit circuits are active—the only two times that the output should legitimately be below its regulated value.

Notice that the FB pin is the virtual ground node of the feedback amplifier. A typical compensation network does not include local DC feedback around the amplifier, so that the DC level at FB will be an accurate replica of the output voltage, divided down by R1 and R_B (Figure 3). However, the compensation capacitors will tend to attenuate AC signals at FB, especially with low bandwidth Type 1 feedback loops. This can create a situation where the MIN, MAX and PGOOD comparators do not respond immediately to shifts in the output voltage, if they monitor the output at FB. With VID code switching on the fly, this problem is aggravated.

To overcome this, a second resistor divider is used (see Block Diagram) to provide the MIN, MAX and PGOOD comparators with an accurate replica of the output voltage. This ensures that the comparators react rapidly to code changes. For the I/O channel, the output voltage is independent of VID codes and therefore the change in V_{OUT} is minimized. Maximizing I/O feedback loop bandwidth will minimize these delays and allow MIN and MAX to operate properly. See the Feedback Loop/Compensation section.

PGOOD Flag

The LTC1705 incorporates a power good pin (PGOOD). PGOOD is an open-drain output and requires an external pull-up resistor. If all three regulators are typically within ±10% of their nominal value, transistor MPG shuts off (see Block Diagram) and PGOOD is pulled high by the external pull-up resistor. If any of the three outputs is more than 10% outside the nominal value for more than 4µs, PGOOD pulls low, indicating that an output is out of regulation. For PGOOD to pull high, all three outputs must be in regulation for more than 20µs. PGOOD remains active during soft start and current limit. On power up, PGOOD pulls low. As soon as the RUN/SS pin rises above the shutdown threshold, the three pair of power good comparators take over and control the transistor MPG directly. The 4µs and 20µs delay ensure that short output transient glitches, that are successfully "caught" by the power good comparators, don't cause momentary glitches at the PGOOD pin.

For the core channel, if there is a VID code change, the internal DAC responds by switching its output voltage immediately. However, the switching power supply output slew rate is limited by the output filter. If the VID code step change is small, the power good comparator might not register any transition. To acknowledge the code transition command , the LTC1705 forces PGOOD to pull low for 20µs once there is a VID code change. After this short interval, the power good comparators decide the PGOOD status.

Shutdown/Soft-Start

The RUN/SS pin performs two functions: if pulled to ground, it shuts down the LTC1705 and it acts as a conventional soft-start pin, enforcing a maximum duty cycle limit proportional to the voltage at RUN/SS. An internal 3µA current source pull-up is connected to the RUN/SS pin, allowing a soft-start ramp to be generated with a single external capacitor to ground. The 3µA current source is active even if the LTC1705 is shut down, ensuring the device will start when any external pull-down at RUN/SS is released. In shutdown, the LTC1705 enters micropower sleep mode and quiescent current drops typically below 50µA.

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The RUN/SS pin shuts down the LTC1705 if it falls below 0.5V (Figure 4). Between 0.5V and about 1V, the LTC1705 wakes up and the duty cycle is kept to a miminum. As the potential at RUN/SS increases, the duty cycle increases linearly between 1V and 2V, reaching its final value of 90% when RUN/SS is above 2V. Somewhere before this point, the feedback amplifier will assume control of the loop and the output will come into regulation. When RUN/SS rises to 1V below V_{CC}, the MIN feedback comparator is enabled and the LTC1705 is in full operation.

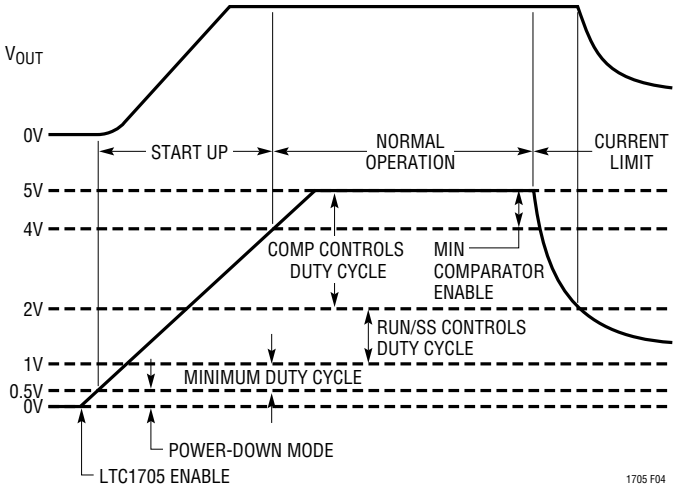

Figure 4. Soft-Start Operation in Start Up and Current Limit

Current Limit

The LTC1705 includes an onboard current limit circuit that limits the maximum output current to a user-programmed level. It works by sensing the voltage drop across QB during the time that QB is on and comparing that voltage to a user-programmed voltage at I_{MAX}. Since QB looks like a low value resistor during its on-time, the voltage drop across it is proportional to the current flowing in it. In a buck converter, the average current in the inductor is equal to the output current. This current also flows through QB during its on-time. Thus, by watching the voltage across QB, the LTC1705 can monitor the output current.

Any time QB is on and the current flowing to the output is reasonably large, the SW node at the drain of QB will be somewhat negative with respect to PGND. The LTC1705 senses this voltage, inverts it and compares the sensed voltage with a positive voltage at the I_{MAX} pin. The I_{MAX} pin includes a trimmed 10µA pull-up, enabling the user to set the voltage at I_{MAX} with a single resistor, R_{IMAX}, to ground. The LTC1705 compares the two inputs and begins limiting the output current when the magnitude of the negative voltage at the SW pin is greater than the voltage at I_{MAX}. When the load current increases abruptly, the voltage feedback loop forces the duty cycle to increase rapidly and the on-time of QB will be small momentarily. The $R_{DS(ON)}$ of QB must be low enough to ensure that the SW node is pulled low within the QB on-time for proper current sensing.

The current limit detector is connected to an internal gm amplifier that pulls a current from the RUN/SS pin proportional to the difference in voltage magnitudes between the SW and I_{MAX} pins. The maximum value of this current is 250µA (typically). It begins to discharge the soft-start capacitor at RUN/SS, reducing the duty cycle and controlling the output voltage until the current drops below the limit. The soft-start capacitor needs to move a fair amount before it has any effect on the duty cycle, adding a delay until the current limit takes effect (Figure 4). This allows the LTC1705 to experience brief overload conditions without affecting the output voltage regulation. The delay also acts as a pole in the current limit loop to enhance loop stability. While the soft-start capacitor is being discharged, the top MOSFET must withstand the high power dissipation due to the high current especially if the regulator is powered by a high current supply. Larger overloads cause the soft-start capacitor to pull down quickly, protecting the output components from damage. The current limit gm amplifier includes a clamp to prevent it from pulling RUN/SS below 0.5V and shutting off the LTC1705.

Power MOSFET $R_{DS(ON)}$ varies from MOSFET to MOSFET, limiting the accuracy obtainable from the LTC1705 current limit loop. Additionally, ringing on the SW node due to parasitics can add to the apparent current, causing the loop to engage early. The LTC1705 current limit is designed primarily as a disaster prevention, “no blow up” circuit and is not useful as a precision current regulator. It should typically be set around 50% above the maximum expected normal output current to prevent component tolerances from encroaching on the normal current range. See the Current Limit Programming section for advice on choosing a valve for R_{IMAX}.

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EXTERNAL COMPONENT SELECTION

Power MOSFETs

Getting peak efficiency out of the LTC1705 depends strongly on the external MOSFETs used. The LTC1705 requires at least two external MOSFETs per side—more if one or more of the MOSFETs are paralleled to lower on-resistance. To work efficiently, these MOSFETs must exhibit low $R_{DS(ON)}$ at 5V V_{GS} to minimize resistive power loss while they are conducting current. They must also have low gate charge to minimize transition losses during switching. On the other hand, voltage breakdown requirements in a typical LTC1705 circuit are pretty tame: the 6V maximum input voltage limits the V_{DS} and V_{GS} the MOSFETs can see to safe levels for most devices.

Low $R_{DS(ON)}$

$R_{DS(ON)}$ calculations are pretty straightforward. $R_{DS(ON)}$ is the resistance from the drain to the source of the MOSFETwhen the gate is fully on. Many MOSFETs have $R_{DS(ON)}$ specified at 4.5V gate drive—this is the right number to use in LTC1705 circuits running from a 5V supply. As current flows through this resistance while the MOSFET is on, it generates I^2R watts of heat, where I is the current flowing (usually equal to the output current) and R is the MOSFET $R_{DS(ON)}$. This heat is only generated when the MOSFET is on. When it is off, the current is zero and the power lost is also zero (and the other MOSFET is busy losing power).

This lost power does two things: it subtracts from the power available at the output, costing efficiency, and it makes the MOSFET hotter—both bad things. The effect is worst at maximum load when the current in the MOSFETs and thus the power lost are at a maximum. Lowering $R_{DS(ON)}$ improves heavy load efficiency at the expense of additional gate charge (usually) and more cost (usually). Proper choice of MOSFET $R_{DS(ON)}$ becomes a trade-off between tolerable efficiency loss, power dissipation and cost. Note that while the lost power has a significant effect on system efficiency, it only adds up to a watt or two in a typical LTC1705 circuit, allowing the use of small, surface mount MOSFETs without heat sinks.

Gate Charge

Gate charge is amount of charge (essentially, the number of electrons) that the LTC1705 needs to put into the gate of an external MOSFET to turn it on. The easiest way to visualize gate charge is to think of it as a capacitance from the gate pin of the MOSFET to SW (for QT) or to PGND (for QB). This capacitance is composed of MOSFET channel charge, actual parasitic drain-source capacitance and Miller-multiplied gate-drain capacitance, but can be approximated as a single capacitance from gate to source. Regardless of where the charge is going, the fact remains that it all has to come out of PV_{CC} to turn the MOSFET gate on and when the MOSFET is turned back off, that charge all ends up at ground. In the meanwhile, it travels through the LTC1705's gate drivers, heating them up. More power lost!

In this case, the power is lost in little bite-sized chunks, one chunk per switch per cycle, with the size of the chunk set by the gate charge of the MOSFET. Every time the MOSFET switches, another chunk is lost. Clearly, the faster the clock runs, the more important gate charge becomes as a loss term. Old-fashioned switchers that ran at 20kHz could pretty much ignore gate charge as a loss term; in the 550kHz LTC1705, gate charge loss can be a significant efficiency penalty. Gate charge loss can be the dominant loss term at medium load currents, especially with large MOSFETs. Gate charge loss is also the primary cause of power dissipation in the LTC1705 itself.

TG Charge Pump

There's another nuance of MOSFET drive that the LTC1705 needs to get around. The LTC1705 is designed to use N-channel MOSFETs for both QT and QB, primarily because N-channel MOSFETs generally cost less and have lower $R_{DS(ON)}$ than similar P-channel MOSFETs. Turning QB on is simple since the source of QB is attached to PGND; the LTC1705 just switches the BG pin between PGND and PV_{CC} . Driving QT is another matter. The source of QT is connected to SW which rises to PV_{CC} when QT is on. To keep QT on, the LTC1705 must get TG one MOSFET $V_{GS(ON)}$ above PV_{CC} . It does this by utilizing a floating driver with the negative lead of the driver attached to SW (the source of QT) and the PV_{CC} lead of the driver coming

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out separately at BOOST. An external 1µF capacitor (CCP) connected between SW and BOOST (Figure 2) supplies power to BOOST when SW is high and recharges itself through DCP when SW is low. This simple charge pump keeps the TG driver alive even as it swings well above PV_{CC}. The value of the bootstrap capacitor CCP needs to be at least 100 times that of the total "effective" gate capacitance of the topside MOSFET(s). For very large external MOSFETs (or multiple MOSFETs in parallel), CCP may need to be increased beyond the 1µF value.

Input Supply

The BiCMOS process that allows the LTC1705 to include large MOSFET drivers on-chip also limits the maximum input voltage to 6V. This limits the practical maximum input supply to a loosely regulated 5V rail. The LTC1705 operates properly with input supplies down to about 3.3V, so a typical 3.3V supply can also be used if the external MOSFETs are appropriately chosen (see the Power MOSFETs section).

At the same time, the input supply needs to supply several amps of current without excessive voltage drop. The input supply must have regulation adequate to prevent sudden load changes from causing the LTC1705 input voltage to dip. In typical applications where the LTC1705 is generating a secondary low voltage logic supply, all of these input conditions are met by the main system logic supply when fortified with an input bypass capacitor.

Input Bypass Capacitor

A typical LTC1705 circuit running from a 5V logic supply might provide 1.6V at 15A at its core output. 5V to 1.6V implies a duty cycle of 32%, which means QTC is on 32% of each switching cycle. During QTC's on-time, the current drawn from the input equals the load current and during the rest of the cycle, the current drawn from the input is near zero. This 0A to 15A, 32% duty cycle pulse train adds up to $7A_{RMS}$ at the input. At 550kHz, switching cycles last about 1.8µs—most system logic supplies have no hope of regulating output current with that kind of speed. A local input bypass capacitor is required to make up the difference and prevent the input supply from dropping drastically when QTC kicks on. This capacitor is usually chosen for RMS ripple current capability and ESR as well as value. The LTC1705 I/O channel typically operates at a much smaller output current, hence the input bypass capacitor in an LTC1705 circuit should be chosen primarily to meet the core output requirement.

Consider our 15A example. The input bypass capacitor gets exercised in three ways: its ESR must be low enough to keep the initial drop as QT turns on within a reasonable value (100mV or so); its RMS current capability must be adequate to withstand the $7A_{RMS}$ ripple current at the input and the capacitance must be large enough to maintain the input voltage until the input supply can make up the difference. Generally, a capacitor that meets the first two parameters will have far more capacitance than is required to keep capacitance-based droop under control. In our example, we need 0.006Ω ESR to keep the input drop under 100mV with a 15A current step and $7A_{RMS}$ ripple current capacity to avoid overheating the capacitor. These requirements can be met with multiple low ESR tantalum or electrolytic capacitors in parallel or with a large monolithic ceramic capacitor.

Tantalum capacitors are a popular choice as input capacitors for LTC1705 applications, but they deserve a special caution here. Generic tantalum capacitors have a destructive failure mechanism if they are subjected to large RMS currents (like those seen at the input of a LTC1705). At some random time after they are turned on, they can blow up for no apparent reason. The capacitor manufacturers are aware of this and sell special "surge tested" tantalum capacitors specifically designed for use with switching regulators. When choosing a tantalum input capacitor, make sure that it is rated to carry the RMS current that the LTC1705 will draw. If the data sheet doesn't give an RMS current rating, chances are the capacitor isn't surge tested. Don't use it!

Output Bypass Capacitor

The output bypass capacitor has quite different requirements from the input capacitor. The ripple current at the output of a buck regulator like the LTC1705 is much lower than at the input, due to the fact that the inductor current is constantly flowing at the output. The primary concern at the output is capacitor ESR. Fast load current transitions at the output appear as voltage across the ESR of the

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output bypass capacitor until the feedback loop in the LTC1705 can change the inductor current to match the new load current value. This ESR step at the output is often the single largest budget item in the load regulation calculation. As an example, our hypothetical 1.6V, 15A switcher with a 0.006Ω ESR output capacitor would experience a 90mV step at the output with a 0A to 15A load step—a 5.6% output change!

Usually the solution is to parallel several capacitors at the output. For example, to keep the transient response in side of 3.5% with the previous design, we'd need an output ESR better than 0.004Ω. This can be met with six 0.025Ω, 180µF special polymer capacitors in parallel.

Inductor

The inductor in a typical LTC1705 circuit is chosen primarily for value and saturation current. The inductor value sets the ripple current, which is commonly chosen between 20% to 40% of the anticipated full load current. Ripple current is set by:

$$I_{RIPPLE} = \frac{t_{ON(QB)}(V_{OUT})}{L}$$

In our 1.6V, 15A example, we'd set the ripple to 20% of 15A or 3A and the inductor value would be:

$$L = \frac{t_{ON(QB)}(V_{OUT})}{I_{RIPPLE}} = \frac{(1.2\mu s)(1.6V)}{3A} = 0.67\mu H$$

$$\text{with} \quad t_{ON(QB)} = \left(1 - \frac{1.6V}{5V}\right) / 550kHz = 1.2\mu s$$

The inductor must not saturate at the expected peak current. In this case, if the current limit was set to 22.5A, the inductor should be rated to withstand 22.5A + (0.5 • I_{RIPPLE}) or 24A without saturating.

FEEDBACK LOOP/COMPENSATION

Feedback Loop Types

In a typical LTC1705 circuit, the feedback loop consists of the modulator, the external inductor, the output capacitor and the feedback amplifier with its compensation network. All of these components affect loop behavior and must be accounted for in the loop compensation. The modulator consists of the internal PWM generator, the output MOSFET drivers and the external MOSFETs themselves. From a feedback loop point of view, it looks like a linear voltage transfer function from COMP to SW and has a gain roughly equal to the input voltage. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a second order LC roll off at the output, with the attendant 180° phase shift. This rolloff is what filters the PWM waveform, resulting in the desired DC output voltage, but the phase shift complicates the loop compensation if the gain is still higher than unity at the pole frequency. Eventually (usually well above the LC pole frequency), the reactance of the output capacitor will approach its ESR and the rolloff due to the capacitor will stop, leaving 6dB/octave and 90° of phase shift (Figure 5).

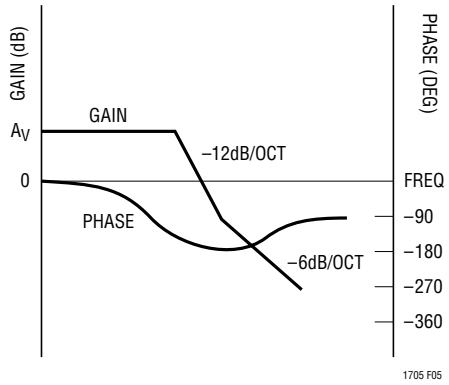

Figure 5. Transfer Function of Buck Modulator

So far, the AC response of the loop is pretty well out of the user's control. The modulator is a fundamental piece of the LTC1705 design and the external L and C are usually chosen based on the regulation and load current requirements without considering the AC loop response. The feedback amplifier, on the other hand, gives us a handle with which to adjust the AC response. The goal is to have 180° phase shift at DC (so the loop regulates) and something less than 360° phase shift at the point that the loop

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gain falls to 0dB. The simplest strategy is to set up the feedback amplifier as an inverting integrator, with the 0dB frequency lower than the LC pole (Figure 6). This "Type 1" configuration is stable but transient response is less than exceptional if the LC pole is at a low frequency.

Figure 7 shows an improved "Type 2" circuit that uses an additional pole-zero pair to temporarily remove 90° of phase shift. This allows the loop to remain stable with 90° more phase shift in the LC section, provided the loop reaches 0dB gain near the center of the phase "bump." Type 2 loops work well in systems where the ESR zero in the LC roll-off happens close to the LC pole, limiting the total phase shift due to the LC. The additional phase compensation in the feedback amplifier allows the 0dB point to be at or above the LC pole frequency, improving loop bandwidth substantially over a simple Type 1 loop. It has limited ability to compensate for LC combinations where low capacitor ESR keeps the phase shift near 180° for an extended frequency range. LTC1705 circuits using conventional switching grade electrolytic output capacitors can often get acceptable phase margin with Type 2 compensation.

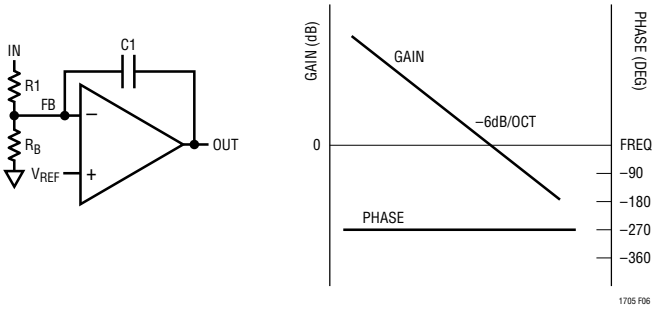

Figure 6. Type 1 Schematic and Transfer Function

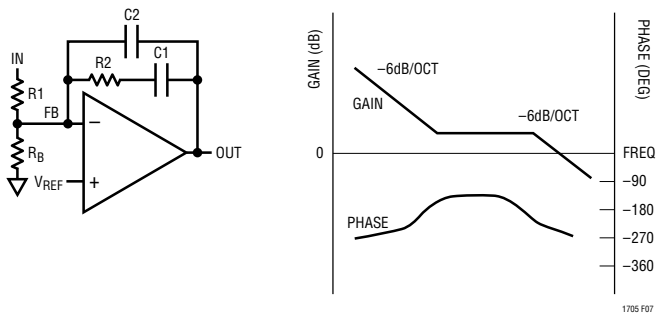

Figure 7. Type 2 Schematic and Transfer Function

"Type 3" loops (Figure 8) use two poles and two zeros to obtain a 180° phase boost in the middle of the frequency band. A properly designed Type 3 circuit can maintain acceptable loop stability even when low output capacitor ESR causes the LC section to approach 180° phase shift well above the initial LC roll-off. As with a Type 2 circuit, the loop should cross through 0dB in the middle of the phase bump to maximize phase margin. Many LTC1705 circuits using low ESR tantalum or OS-CON output capacitors need Type 3 compensation to obtain acceptable phase margin with a high bandwidth feedback loop.

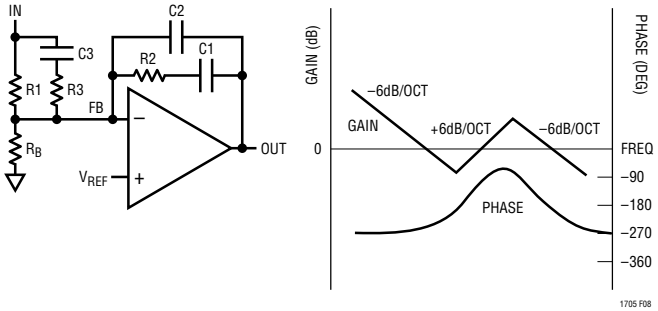

Figure 8. Type 3 Schematic and Transfer Function

Feedback Component Selection

Selecting the R and C values for a typical Type 2 or Type 3 loop is a nontrivial task. The applications shown in this data sheet show typical values, optimized for the power components shown. They should give acceptable performance with similar power components, but can be way off if even one major power component is changed significantly. Applications that require optimized transient response will need to recalculate the compensation values specifically for the circuit in question. The underlying mathematics are complex, but the component values can be calculated in a straightforward manner if we know the gain and phase of the modulator at the crossover frequency.

Modulator gain and phase can be measured directly from a breadboard or can be simulated if the appropriate parasitic values are known. Measurement will give more accurate results, but simulation can often get close enough to give a working system. To measure the modulator gain and phase directly, wire up a breadboard with an LTC1705

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and the actual MOSFETs, inductor and input and output capacitors that the final design will use. This breadboard should use appropriate construction techniques for high speed analog circuitry: bypass capacitors located close to the LTC1705, no long wires connecting components, appropriately sized ground returns, etc. Wire the feedback amplifier as a simple Type 1 loop, with a 10k resistor from V_{OUT} to FB and a 0.1µF feedback capacitor from COMP to FB. Choose the bias resistor (R_B) as required to set the desired output voltage. Disconnect R_B from ground and connect it to a signal generator or to the source output of a network analyzer (Figure 9) to inject a test signal into the loop. Measure the gain and phase from the COMP pin to the output node at the positive terminal of the output capacitor. Make sure the analyzer's input is AC coupled so that the DC voltages present at both the COMP and V_{OUT} nodes don't corrupt the measurements or damage the analyzer.

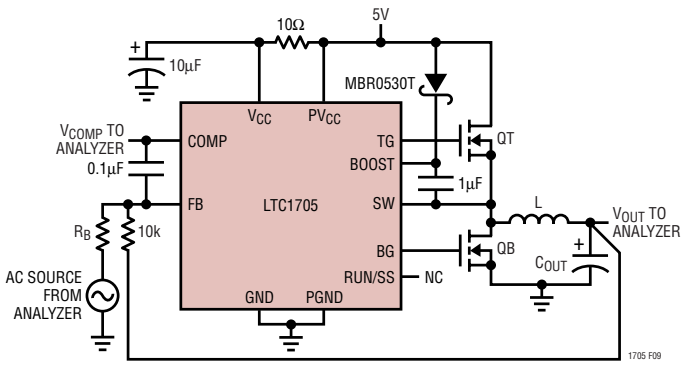

Figure 9. Modulator Gain/Phase Measurement Set Up

If breadboard measurement is not practical, a SPICE simulation can be used to generate approximate gain/phase curves. Plug the expected capacitor, inductor and MOSFET values into the following SPICE deck and generate an AC plot of V(V_{OUT})/V(COMP) in dB and phase of V_{OUT} in degrees. Refer to your SPICE manual for details of how to generate this plot.

```
*1705 modulator gain/phase
*2000 Linear Technology
*this file written to run with PSpice 8.0
*may require modifications for other
SPICE simulators

*MOSFETs
rfet mod sw 0.02      ;MOSFET rdson

*inductor
lext sw out1 1u       ;inductor value
rl out1 out 0.005     ;inductor series R

*output cap
cout out out2 1000u   ;capacitor value
resr out2 0 0.01      ;capacitor ESR

*1705 internals
emod mod 0 comp 0 5   ;3.3 for 3.3V supply
vstim comp 0 0 ac 1   ;ac stimulus
.ac dec 100 1k 1meg
.probe
.end
```

With the gain/phase plot in hand, a loop crossover frequency can be chosen. Usually the curves look something like Figure 5. Choose the crossover frequency in the rising or flat parts of the phase curve, beyond the external LC poles. Frequencies between 10kHz and 50kHz usually work well. Note the gain (GAIN, in dB) and phase (PHASE, in degrees) at this point. The desired feedback amplifier gain will be -GAIN to make the loop gain at 0dB at this frequency. Now calculate the needed phase boost, assuming 60° as a target phase margin:

$$BOOST = -(PHASE + 30°)$$

If the required BOOST is less than 60°, a Type 2 loop can be used successfully, saving two external components. BOOST values greater than 60° usually require Type 3 loops for satisfactory performance.

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Finally, choose a convenient resistor value for R1 (10k is usually a good value). Now calculate the remaining values:

(K is a constant used in the calculations)

f = chosen crossover frequency

$G = 10^{(GAIN/20)}$ (this converts GAIN in dB to G in absolute gain)

TYPE 2 Loop:

$$K = Tan\left(\frac{BOOST}{2} + 45^\circ\right)$$

$$C2 = \frac{1}{2\pi fGKR1}$$

$$C1 = C2\left(K^2 - 1\right)$$

$$R2 = \frac{K}{2\pi fC1}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

TYPE 3 Loop:

$$K = Tan^2\left(\frac{BOOST}{4} + 45^\circ\right)$$

$$C2 = \frac{1}{2\pi fGR1}$$

$$C1 = C2\left(K - 1\right)$$

$$R2 = \frac{\sqrt{K}}{2\pi fC1}$$

$$R3 = \frac{R1}{K - 1}$$

$$C3 = \frac{1}{2\pi f\sqrt{K}R3}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

CURRENT LIMIT PROGRAMMING

Programming current limit on the LTC1705 is straightforward. The I_{MAX} pin sets the current limit by setting the maximum allowable voltage drop across QB (the bottom MOSFET) before the current limit circuit engages. The voltage across QB is set by its on-resistance and the current flowing in the inductor, which is the same as the output current. The LTC1705 current limit circuit inverts the negative voltage across QB before comparing it with the voltage at I_{MAX}, allowing the current limit to be set with a positive voltage.

To set the current limit, calculate the expected voltage drop across QB at the maximum desired current:

$$V_{PROG} = (I_{LIMIT})\ (R_{DS(ON)})$$

I_{LIMIT} should be chosen to be quite a bit higher than the expected operating current, to allow for MOSFET $R_{DS(ON)}$ changes with temperature. Setting I_{LIMIT} to 150% of the maximum normal operating current is usually safe and will adequately protect the power components if they are chosen properly. Note that the ringing on the switch node can cause error for the current limit threshold. This factor will change depending on the layout and the components used. V_{PROG} is then programmed at the I_{MAX} pin using the internal 10µA pull-up and an external resistor:

$$R_{IMAX} = V_{PROG}/10\mu A$$

The resulting value of R_{IMAX} should be checked in an actual circuit to ensure that the current circuit kicks in as expected. MOSFET $R_{DS(ON)}$ specs are like horsepower ratings in automobiles and should be taken with a grain of salt. Circuits that use very low values for R_{IMAX} (<10k) should be checked carefully, since small changes in R_{IMAX} can cause large I_{LIMIT} changes when the switch node ringing makes up a large percentage of the total V_{PROG} value. If V_{PROG} is set too low, the LTC1705 may fail to start up.

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Accuracy Trade-Offs

The V_{DS} sensing scheme used in the LTC1705 is not particularly accurate, primarily due to uncertainty in the $R_{DS(ON)}$ from MOSFET to MOSFET. A second error term arises from the ringing present at the SW pin, which causes the V_{DS} to look larger than $(I_{LOAD})(R_{DS(ON)})$ at the beginning of QB's on-time. These inaccuracies do not prevent the LTC1705 current limit circuit from protecting itself and the load from damaging overcurrent conditions, but they do prevent the user from setting the current limit to a tight tolerance if more than one copy of the circuit is being built. The 50% factor in the current setting equation above reflects the margin necessary to ensure that the circuit will stay out of current limit at the maximum normal load, even with a hot MOSFET that is running quite a bit higher than its $R_{DS(ON)}$ spec.

V_{CLK} LINEAR REGULATOR

The LTC1705 monolithic LDO linear regulator is easy to use. Input and output supply bypass capacitors are the only two external components required for this LDO. The V_{INCLK} pin powers up the regulator and an internal P-channel MOS transistor sources at least 150mA of current at a fixed output voltage of 2.5V. This device is short-circuit protected and includes thermal shutdown to turn off all three regulator outputs should the junction temperature exceed about 155°C.

The circuit design in the LTC1705 requires the use of an output capacitor as part of the frequency compensation. A minimum output capacitor of 2.2µF and ESR larger than 100mΩ is recommended to prevent oscillations. Larger values of output capacitance decrease the peak deviations and provide improved transient response for large load current changes. Many different types of capacitors are available and have widely varying characteristics. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, equivalent series inductance and capacitance temperature coefficient. In a typical operating condition, a 10µF solid tantalum at the V_{OUTCLK} pin ensures stability. The AVX TPSD106M035R0300 or equivalent works well in this application.

OPTIMIZING PERFORMANCE

2-Step Conversion

The LTC1705 is ideally suited for use in 2-step conversion systems. 2-step systems use a primary regulator to convert the input power source (batteries or AC line voltage) to an intermediate supply voltage, often 5V. The LTC1705 then converts the intermediate voltage to the lower voltage, high current supplies required by the system. Compared to a 1-step converter that converts a high input voltage directly to a very low output voltage, the 2-step converter exhibits superior transient response, smaller component size and equivalent efficiency. Thermal management and layout complexity are also improved with a 2-step approach.

A typical notebook computer supply might use a 4-cell Li-Ion battery pack as an input supply with a 15V nominal terminal voltage. The logic circuits require 5V/3A and 3.3V/5A to power system board logic and 2.5V/0.15A, 1.5V/2A and 1.3V/15A to power the CPU. A typical 2-step conversion system would use a step-down switcher (perhaps an LTC1628 or two LTC1625s) to convert 15V to 5V and another to convert 15V to 3.3V (Figure 10). The 3.3V input supply can power the 1.3V output at the LTC1705 core channel and the 2.5V LDO. The 5V input supply can power the 1.5V I/O channel. The corresponding 1-step system would use four similar step-down switchers plus an LDO, each switcher using 15V as the input supply and generating one of the four output voltages.

Clearly, the 5V and 3.3V sections of the two schemes are equivalent. The 2-step system draws additional power from the 5V and 3.3V outputs, but the regulation techniques and trade-offs at these outputs are similar. The difference lies in the way the 1.5V and 1.3V supplies are generated. For example, the 2-step system converts 3.3V to 1.3V with a 39% duty cycle. During the QT on-time, the voltage across the inductor is 2V and during the QB on-time, the voltage is 1.3V, giving roughly symmetrical transient response to positive and negative load steps. The 2V maximum voltage across the inductor allows the use of a small 0.47µH inductor while keeping ripple current to 3A (20% of the 15A maximum load). By contrast, the 1-step

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converter is converting 15V to 1.3V, requiring just a 9% duty cycle. Inductor voltages are now 13.7V when QT is on and 1.3V when QB is on, giving vastly different di/dt values and correspondingly skewed transient response with positive and negative current steps. The narrow 9% duty cycle usually requires a lower switching frequency, which in turn requires a higher value inductor and larger output capacitor. Parasitic losses due to the large voltage swing at the source of QT cost efficiency, eliminating any advantage the 1-step conversion might have had.

Note that power dissipation in the LTC1705 portion of a 2-step circuit is lower than it would be in a typical 1-step converter, even in cases where the 1-step converter has higher total efficiency than the 2-step system. In a typical microprocessor core supply regulator, for example, the regulator is usually located right next to the CPU. In a 1-step design, all of the power dissipated by the core regulator is right there next to the hot CPU, aggravating thermal management. In a 2-step LTC1705 design, a significant percentage of the power lost in the core regulation system happens in the 5V or 3.3V supply, which is usually away from the CPU. The power lost to heat in the LTC1705 section of the system is relatively low, minimizing the heat near the CPU.

Additionally, with a 1-step converter, the high input battery voltage requires the MOSFET to operate at high voltage levels. This imposes stringent requirements on the MOSFETs selection. Most of the MOSFETs that meet the high voltage and high current requirements are expensive and bulky. This makes for an awkward power supply design, especially in portable applications. The high input voltage also necessitates higher gate drive, which aggravate switching losses.

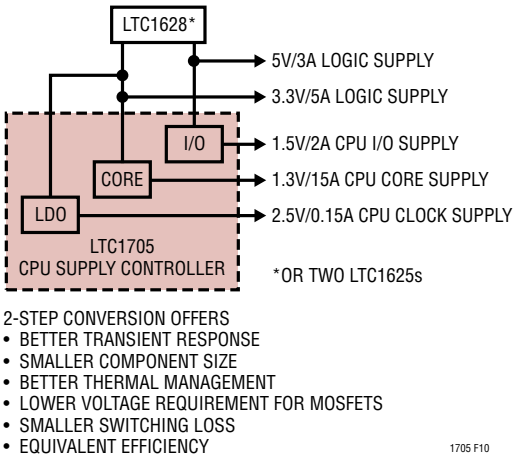

Figure 10. 2-Step Conversion Block Diagram

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2-Step Efficiency Calculation

Calculating the efficiency of a 2-step converter system involves some subtleties. Simply multiplying the efficiency of the primary 5V or 3.3V supply by the efficiency of the 1.5V or 1.3V supply under estimates the actual efficiency, since a significant fraction of the total power is drawn from the 3.3V and 5V rails in a typical system. The correct way to calculate system efficiency is to calculate the power lost in each stage of the converter and divide the total output power from all outputs by the sum of the output power plus the power lost:

$$\text{Efficiency} = \frac{\text{Total Output Power}}{\text{Total Output Power} + \text{Total Output Lost}}(100\%)$$

In our example 2-step system, the total output power is:

Total Output Power =

15W + 16.5W + 0.375W + 3W + 19.5W = 54.375W

(corresponding to 5V, 3.3V, 2.5V, 1.5V and 1.3V output voltages)

Assuming the LTC1705 provides 90% efficiency at the core and I/O channels, and 75% efficiency at the LDO, the additional loads on the 5V and 3.3V supplies are:

1.3V: 19.5W/90% =21.67W ⇒ 6.6A from 3.3V

1.5V: 3W/90% =3.3W ⇒ 0.66A from 5V

2.5V: 0.375W/75% =0.5W ⇒ 0.152A from 3.3V

If the 5V and 3.3V supplies are each 94% efficient, the power lost in each supply is:

1.3V: 21.67W – 19.5W = 2.17W

1.5V: 3.3W – 3W = 0.3W

2.5V: 0.5W – 0.375W = 0.125W

3.3V: 16.5W + 3.3V(6.6A + 0.152A) = 38.78W Load
(38.78W/94%) – 38.78W = 2.48W Lost

5V: 15W + 5V(0.66A) = 18.3W Load
(18.3W/94%) – 18.3W = 1.17W Lost

Total Loss = 6.25W

Total System Efficiency =
54.375W/(54.375W + 6.25W) = 89.7%

Maximizing High Load Current Efficiency

Efficiency at high load currents is primarily controlled by the resistance of the components in the power path (QT, QB, L_{EXT}) and power lost in the gate drive circuits due to MOSFET gate charge. Maximizing efficiency in this region of operation is as simple as minimizing these terms.

The behavior of the load over time affects the efficiency strategy. Parasitic resistances in the MOSFETs and the inductor set the maximum output current the circuit can supply without burning up. A typical efficiency curve shows that peak efficiency occurs near 30% of this maximum current. If the load current will vary around the efficiency peak and will spend relatively little time at the maximum load, choosing components so that the average load is at the efficiency peak is a good idea. This puts the maximum load well beyond the efficiency peak, but usually gives the greatest system efficiency over time, which translates to the longest run time in a battery-powered system. If the load is expected to be relatively constant at the maximum level, the components should be chosen so that this load lands at the peak efficiency point, well below the maximum possible output of the converter.

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REGULATION OVER COMPONENT TOLERANCE/ TEMPERATURE

DC Regulation Accuracy

The LTC1705 initial DC output accuracy depends mainly on internal reference accuracy, op amp offset and internal or external resistor accuracy. Two LTC1705 specs come into play: V_{SENSEC} voltage and feedback voltage line regulation. The V_{SENSEC} voltage spec is within ±1.25% for all VID codes over the full temperature range, which encompasses reference accuracy, error amplifier offset and the input resistor divider mismatch. The feedback voltage line regulation spec adds an additional 0.1%/V term that accounts for change in reference output with change in input supply voltage. With a 5V supply, the errors contributed by the LTC1705 itself add up to less than 1.5% DC error at the output.

At the I/O side, the output voltage setting resistors (R1 and R_B in Figure 3) are the other major contributor to DC error. At a typical 1.xV output voltage, the resistors are of roughly the same value, which tends to halve their error terms, improving accuracy. Still, using 1% resistors for R1 and R_B will add 1% to the total output error budget. Using 0.1% resistors in just those two positions can nearly halve the DC output error for very little additional cost.

Load Regulation

Load regulation is affected by feedback amplifier gain and external ground drops in the feedback path. A full-range load step might require a 10% duty cycle change to keep the output constant, requiring the COMP pin to move about 100mV. With amplifier gain at 85dB, this adds up to only a 10µV shift at FB, negligible compared to the reference accuracy terms.

External ground drops aren't so negligible. The LTC1705 can sense the positive end of the output voltage by attaching the feedback resistor directly at the load, but it cannot do the same with the ground lead. Just 0.001Ω of resistance in the ground lead at 15A load will cause a 15mV error in the output voltage—as much as all the other DC errors put together. Proper layout becomes essential to achieving optimum load regulation from the LTC1705. A properly laid out LTC1705 circuit should move not more than one to two millivolts at the output from zero to full load.

Transient Response

Transient response is the other half of the regulation equation. The LTC1705 can keep the DC output voltage constant to within 1% when averaged over hundreds of cycles. Over just a few cycles, however, the external components conspire to limit the speed that the output can move. Consider our typical 5V to 1.5V circuit, subjected to a 1A to 5A load transient. Initially, the loop is in regulation and the DC current in the output capacitor is zero. Suddenly, an extra 4A start flowing out of the output capacitor while the inductor is still supplying only 1A. This sudden change will generate a (4A)(R_{ESR})voltage step at the output; with a typical 0.015Ω output capacitor ESR, this is a 60mV or 4% (for a 1.5V output voltage) step at the output!

Very quickly, the feedback loop will realize that something has changed and will move at the bandwidth allowed by the external compensation network towards a new duty cycle. If the bandwidth is set to 50kHz, the COMP pin will get to 60% of the way to 90% duty cycle in 3µs. Now the inductor is seeing 3.5V across itself for a large portion of the cycle and its current will increase from 1A at a rate set by di/dt = V/L. If the inductor value is 0.5µH, the peak di/dt will be 3.5V/0.5µH or 7A/µs. Sometime in the next few micro-seconds after the switch cycle begins, the inductor current will have risen to the 5A level of the load current and the output voltage will stop dropping. At this point, the inductor current will rise somewhat above the level of the output current to replenish the charge lost from the output capacitor during the load transient. During the next couple of cycles, the MIN comparator may trip on and off, preventing the output from falling below its -5% threshold until the time constant of the compensation loop runs out and the main feedback amplifier regains control. With a properly compensated loop, the entire recovery time will be inside of 10µs.

TYPICAL APPLICATIONS

Most loads care only about the maximum deviation from ideal, which occurs somewhere in the first two cycles after the load step hits. During this time, the output capacitor does all the work until the inductor and control loop regain control. The initial drop (or rise if the load steps down) is entirely controlled by the ESR of the capacitor and amounts to most of the total voltage drop. To minimize this drop, reduce the ESR as much as possible by choosing low ESR capacitors and/or paralleling multiple capacitors at the output. The capacitance value accounts for the rest of the voltage drop until the inductor current rises. With most output capacitors, several devices paralleled to get the ESR down will have so much capacitance that this drop term is negligible. Ceramic capacitors are an exception; a small ceramic capacitor can have suitably low ESR with relatively small values of capacitance, making this second drop term significant.

Optimizing Loop Compensation

Loop compensation has a fundamental impact on transient recovery time, the time it takes the LTC1705 to recover after the output voltage has dropped due to output capacitor ESR. Optimizing loop compensation entails maintaining the highest possible loop bandwidth while ensuring loop stability. The feedback component selection section describes in detail the techniques used to design an optimized Type 3 feedback loop, appropriate for most LTC1705 systems.

Measurement Techniques

Measuring transient response presents a challenge in two respects: obtaining an accurate measurement and generating a suitable transient to use to test the circuit. Output measurements should be taken with a scope probe directly across the output capacitor. Proper high frequency probing techniques should be used. In particular, don't use the 6" ground lead that comes with the probe! Use an adapter that fits on the tip of the probe and has a short ground clip to ensure that inductance in the ground path doesn't cause a bigger spike than the transient signal being measured. Conveniently, the typical probe tip ground clip is spaced just right to span the leads of a typical output capacitor.

Now that we know how to measure the signal, we need to have something to measure. The ideal situation is to use the actual load for the test and switch it on and off while watching the output. If this isn't convenient, a current step generator is needed. This generator needs to be able to turn on and off in nanoseconds to simulate a typical switching logic load, so stray inductance and long clip leads between the LTC1705 and the transient generator must be minimized.

Figure 11 shows an example of a simple transient generator. Be sure to use a noninductive resistor as the load element—many power resistors use an inductive spiral pattern and are not suitable for use here. A simple solution is to take ten 1/4W film resistors and wire them in parallel to get the desired value. This gives a noninductive resistive load which can dissipate 2.5W continuously or 50W if pulsed with a 5% duty cycle, enough for most LTC1705 circuits. Solder the MOSFET and the resistor(s) as close to the output of the LTC1705 circuit as possible and set up the signal generator to pulse at a 100Hz rate with a 5% duty cycle. This pulses the LTC1705 with 500µs transients10ms apart, adequate for viewing the entire transient recovery time for both positive and negative transitions while keeping the load resistor cool.

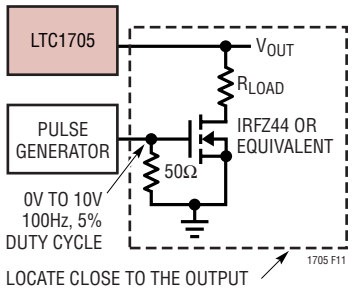
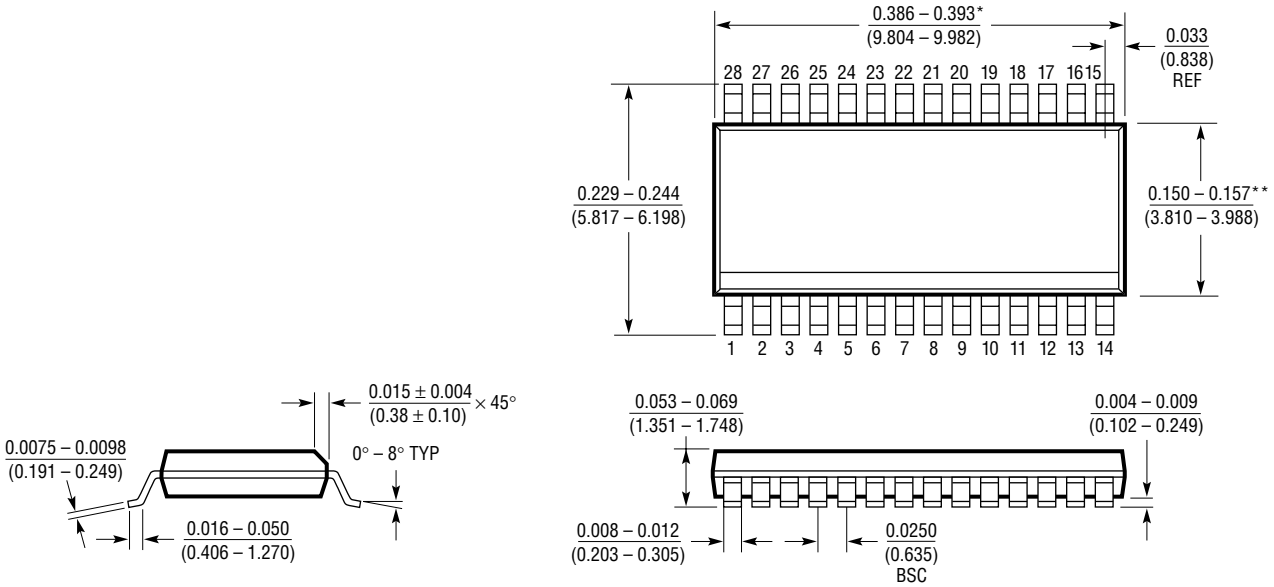


Figure 11. Transient Load Generator

PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



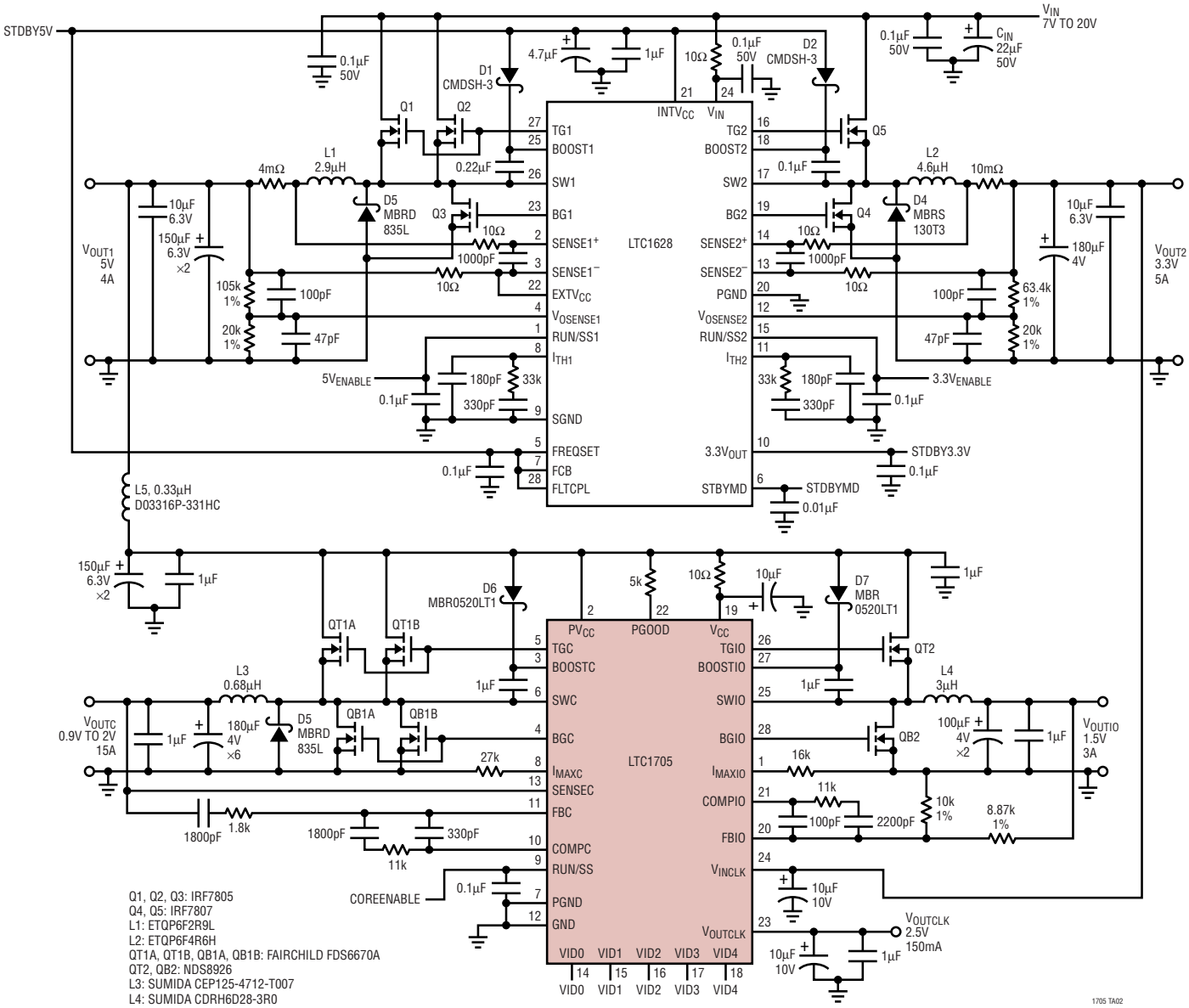
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN28 (SSOP) 1098

TYPICAL APPLICATION

Complete 2-Step Notebook Power Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC1628-PG	Dual High Efficiency 2-Phase Synchronous Step-Down Controller	Constant Frequency, Standby 5V and 3.3V LDOs, $3.5V \le V_{IN} \le 36V$
LTC1703	Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with VID	Mobile VID Control with 25MHz GBW Voltage Mode, $V_{IN} \le 7V$
LTC1708	Dual, 2-Phase Synchronous Step-Down Controller with 5-Bit VID	Mobile CPU VID, Dual Output $3.5V \le V_{IN} \le 36V$, Minimum C_{IN} and C_{OUT}
LTC1736	Synchronous Step-Down Controller with 5-Bit VID Control	Output Fault Protection, Power Good Output, 3.5V to 36V Input

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