0.5-20GHz Driver

GaAs Monolithic Microwave IC

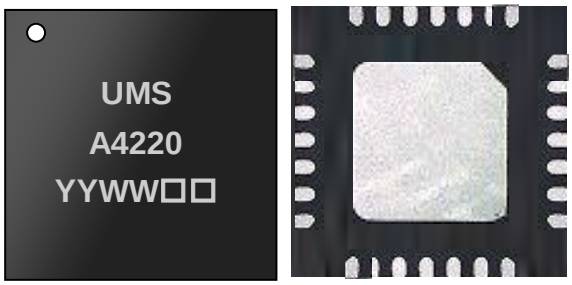
Description

The CHA4220-QGG is a distributed Driver Amplifier that operates between 0.5 and 20GHz.

It is designed for a wide range of applications, such as electronic warfare, X and Ku Point to Point Radio, and test instrumentation.

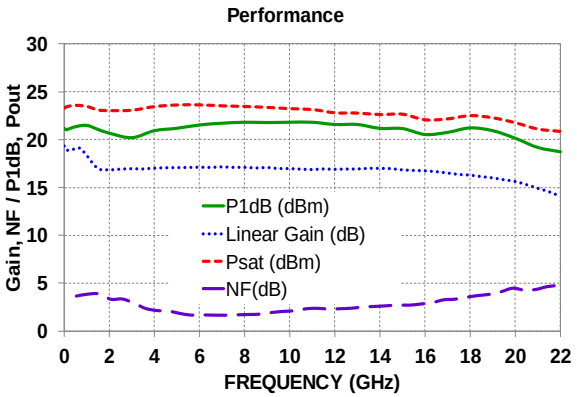
The circuit is manufactured using a 0.25µm gate length power pHEMT process, with via holes through the substrate, air bridges and optical gate lithography.

The part is supplied as 5x5 QFN package with input and output RF accesses matched to 50 ohms.



Main Features

- Broadband performances: 0.5-20GHz
- Typical Linear Gain: 17dB
- P1dB: 20dBm
- Psat: 23dBm
- OIP3: 28dBm
- Typical Noise Figure: 3dB
- DC bias: Idq=120mA @ Vd=6.5V
  With Vg1#-0.3V and Vg2=1.5V.
- 28L QFN 5x5
- MSL3



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	0.5		20	GHz
Gain	Linear Gain		17		dB
NF	Noise Figure		3		dB
Pout	Output Power @1dB comp.		20		dBm

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Electrical Characteristics

Tamb.= +25°C,Vg1 to be set in order to have Idq=120mA, Vg2=1.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	0.5		20	GHz
Gain	Linear Gain		17		dB
NF	Noise Figure		3		dB
IRL	Input Return Loss		15		dB
ORL	Output Return Loss		18		dB
P1dB	Output power for 1dB Gain Compression		20		dBm
Psat	Saturated output power		23		dBm
OIP3	Output Third Order Intercept		28		dBm
Idq	Quiescent current on Vd		120		mA
Vd	Supply voltage on Vd	6	6.5	7	V
Id	Drain current @3dB gain compression		140		mA

The values are representative of typical “test fixture” measurements as defined on the drawing in paragraph “Proposed Evaluation Board”.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pin	Parameter	Values	Unit
Vg1	12	Gate control1 for the amplifier	-0.3	V
Vg2	1	Gate control2 for the amplifier	1.5	V
Vd	19	Drain Voltage (see application circuit p10)	6.5	V

The associated drain current with no RF input power is Idq=120mA

This typical bias is recommended in order to get the best compromise between output power, linearity and Noise Figure performance vs. Temperature.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8V	V
Idq	Drain bias current	170	mA
Vg1	Gate bias voltage Vg1	-2 to 0	V
Vg2	Gate bias voltage Vg2	1 to 2	V
Pin	Maximum CW input power overdrive	17	dBm
Ta	Operating temperature range (chip backside)	-40 to 85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage: these maximum ratings parameters could not be cumulated.

These are stress ratings only, and functional operation of the device at these conditions is not implied.

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Device thermal performance

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

A derating must be applied on the dissipated power if the Tcase temperature cannot be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

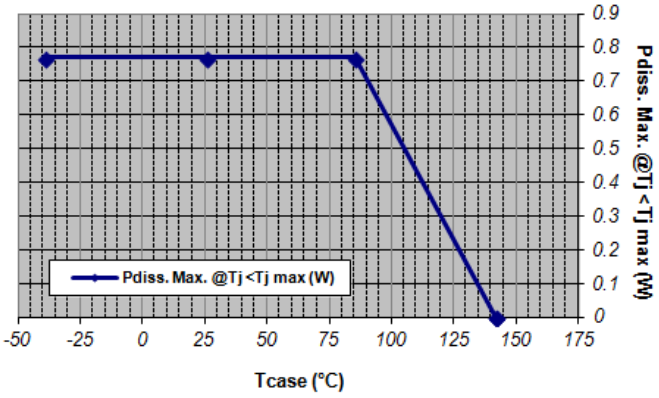
The provided thermal information in the next chart is for the worst biasing point: Idq=110mA and Vd=7V, without RF drive @Tcase=85°C.

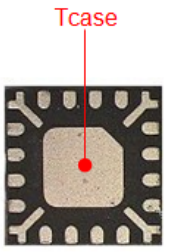
DEVICE THERMAL SPECIFICATION : CHA4220-QGG		
Recommended max. junction temperature (Tj max)	:	142 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power (Pdiss. Max.)	:	0.8 W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	14 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	73.5 °C/W
Minimum Tcase operating temperature(3)	:	-40 °C
Maximum Tcase operating temperature(3)	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.5

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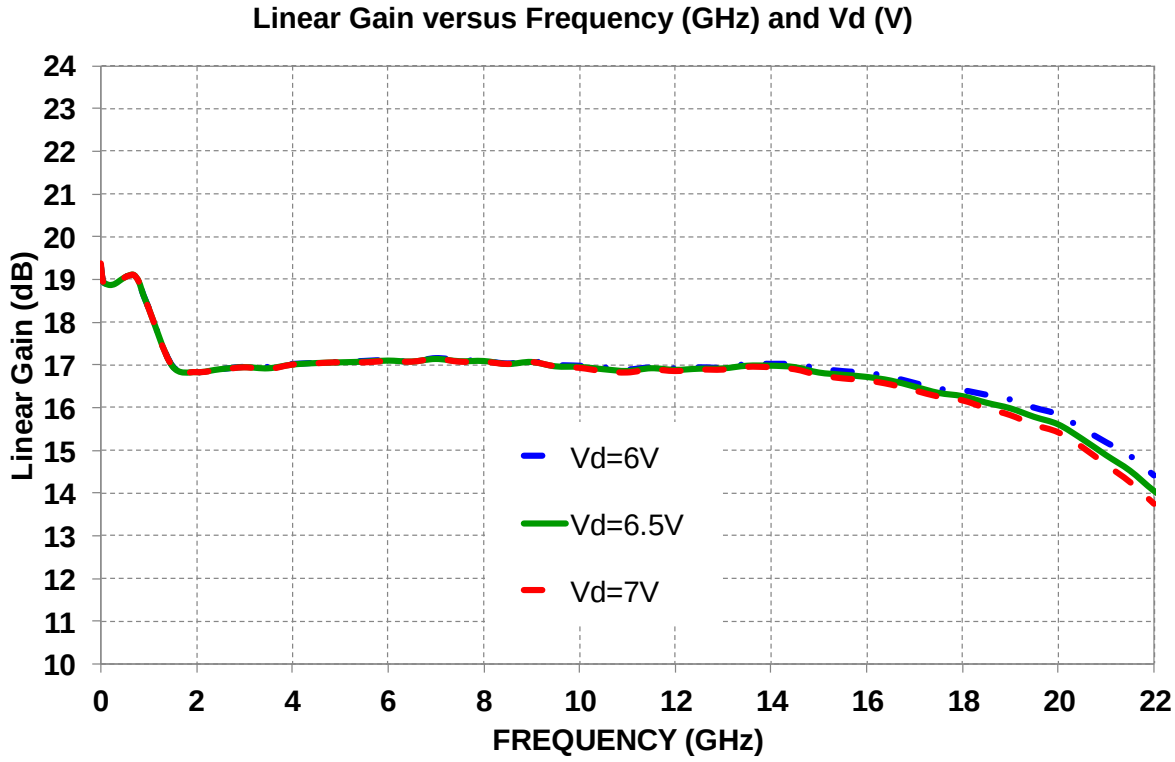
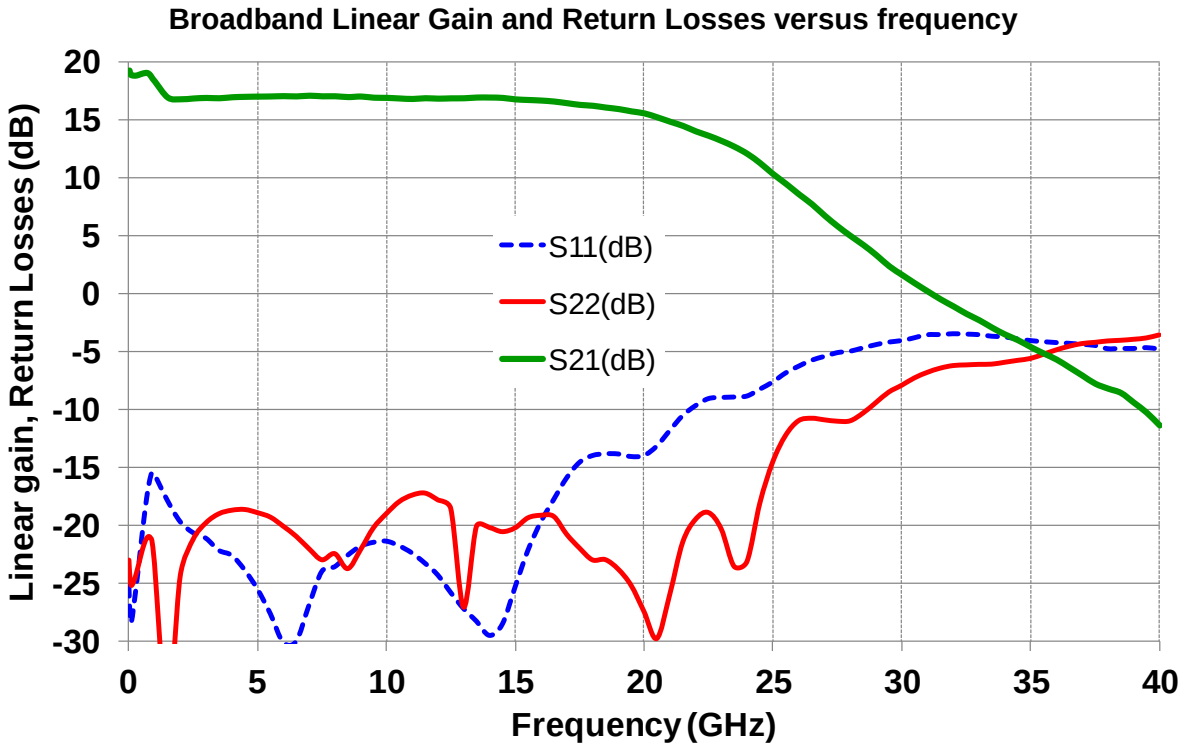
Typical Board Measurements

Tamb.= +25°C, Vd=6.5V, Vg1 set in order to get Idq =120mA, Vg2=1.5V





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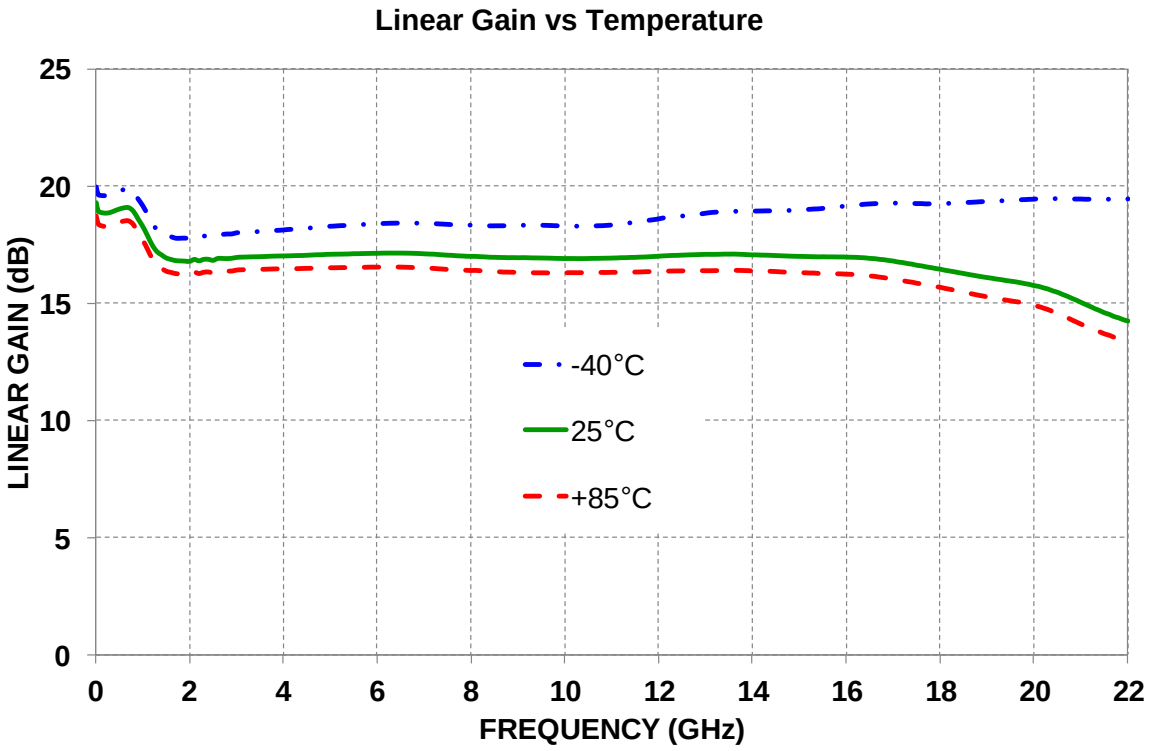
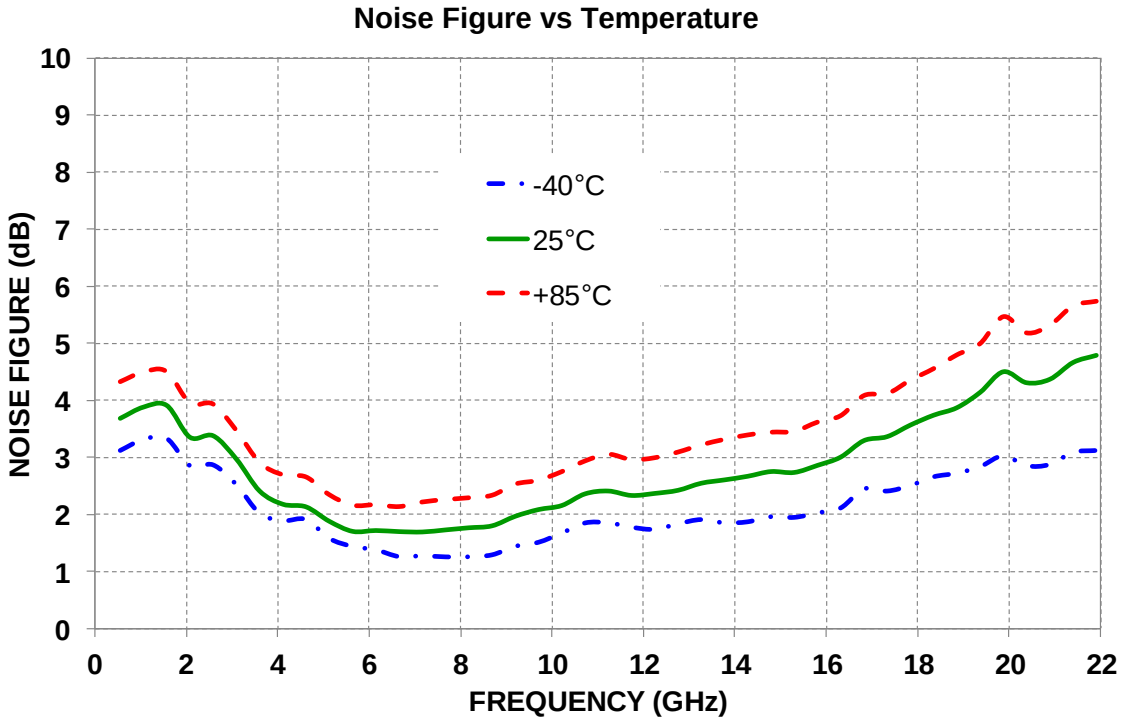
Typical Board Measurements

Vd =6.5V, Vg1 set in order to get Idq =120mA @ Tamb=+25°C with Vg2=1.5V
Vg1 and Vg2 remain constant versus temperature (Tamb.= +25°C, +85°C,-40°C)





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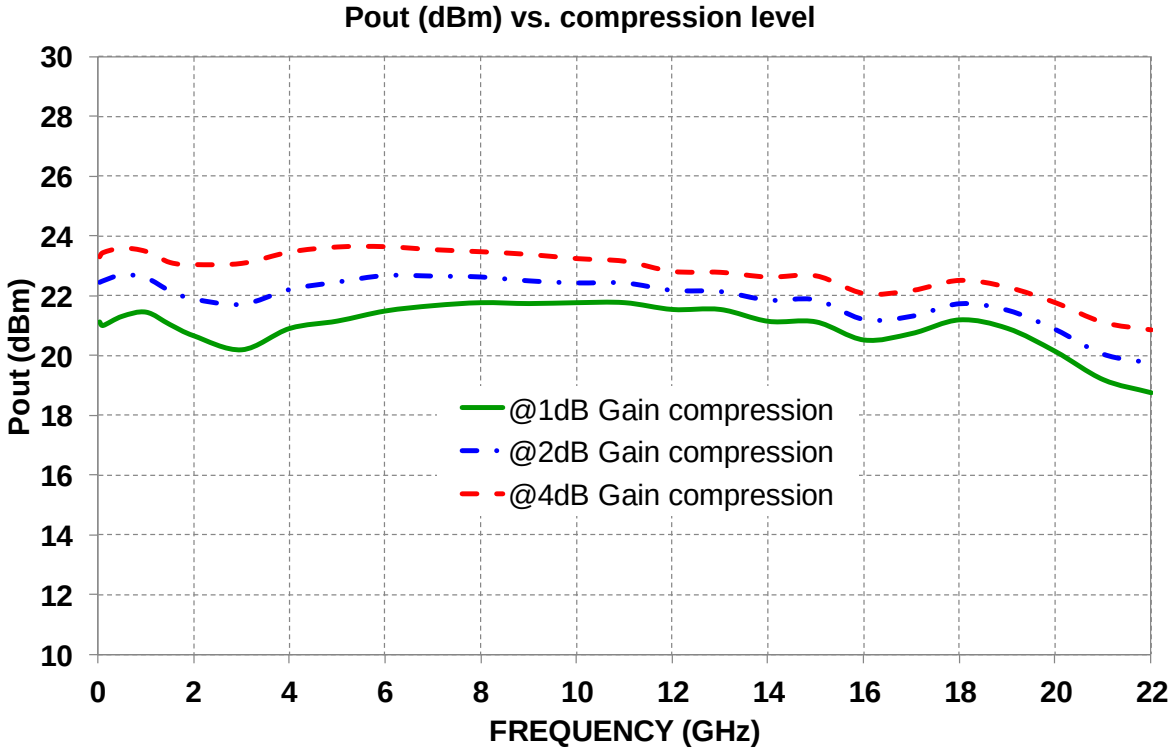
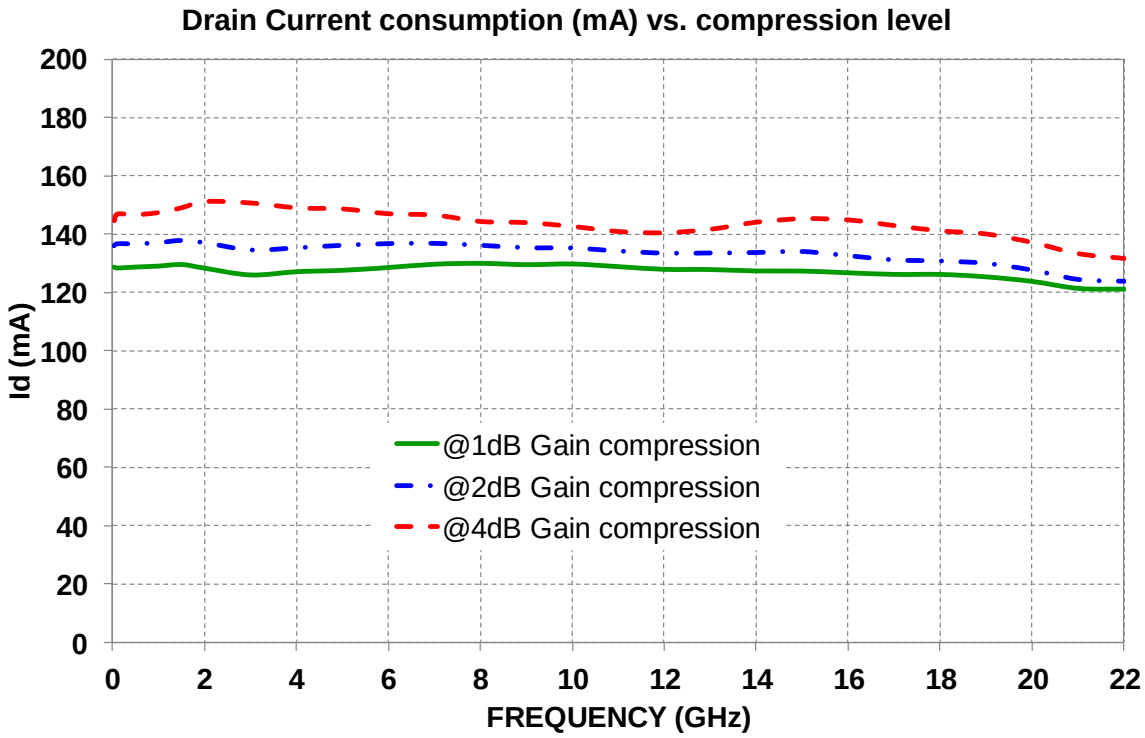
Typical Board Measurements

Tamb.= +25°C, Vd =6.5V, Vg1 set in order to get Idq =120 mA , Vg2=1.5V





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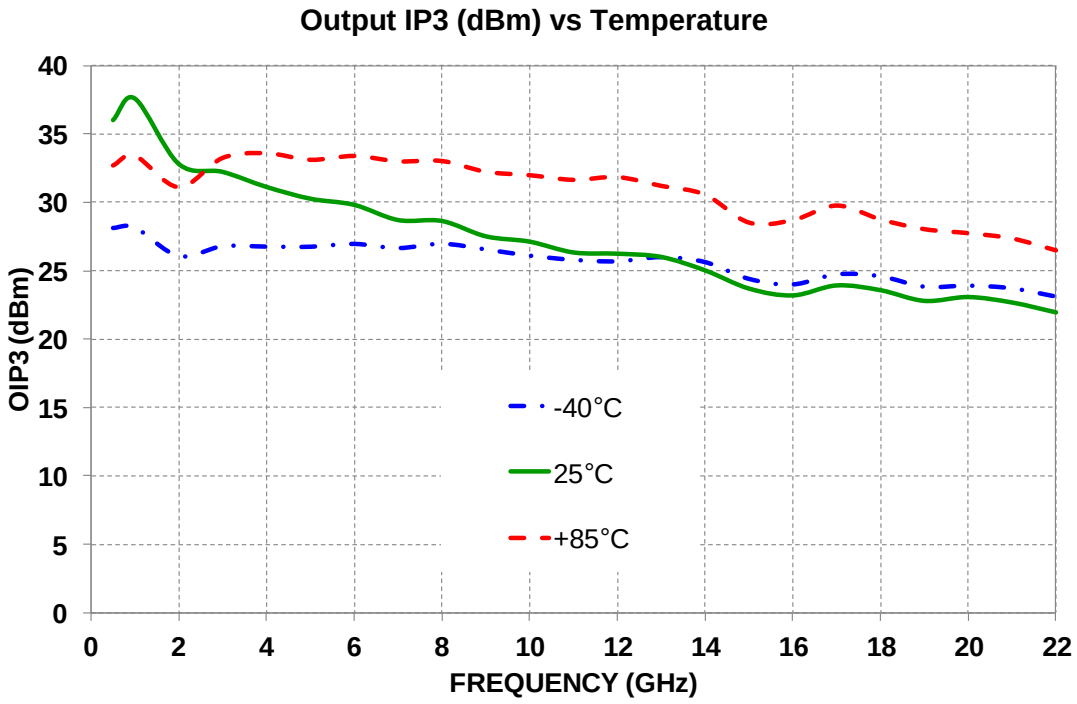
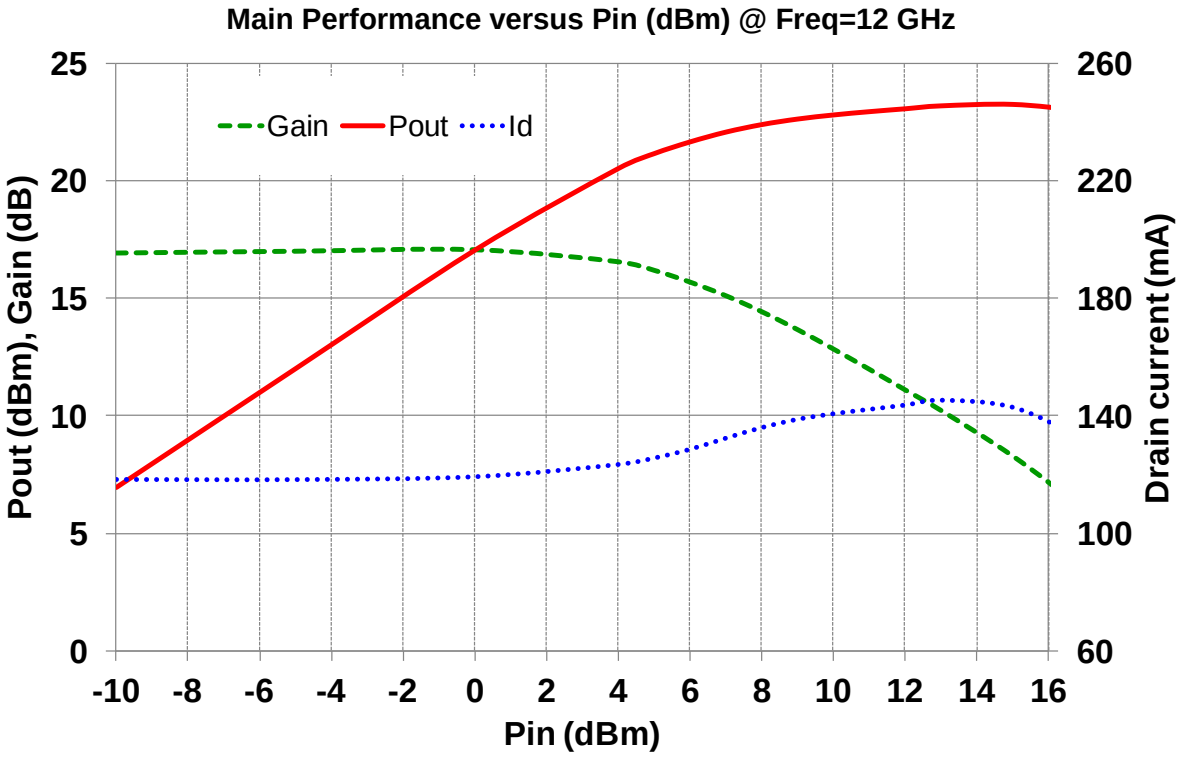
Typical Board Measurements

Vd =6.5V, Vg1 set in order to get Idq =120mA @ Tamb=+25°C with Vg2=1.5V
Vg1 and Vg2 remain constant versus temperature (Tamb.= +25°C, +85°C,-40°C)



Tamb.= +25°C, Vd =6.5V, Vg1 set in order to get Idq =120mA, Vg2=1.5V



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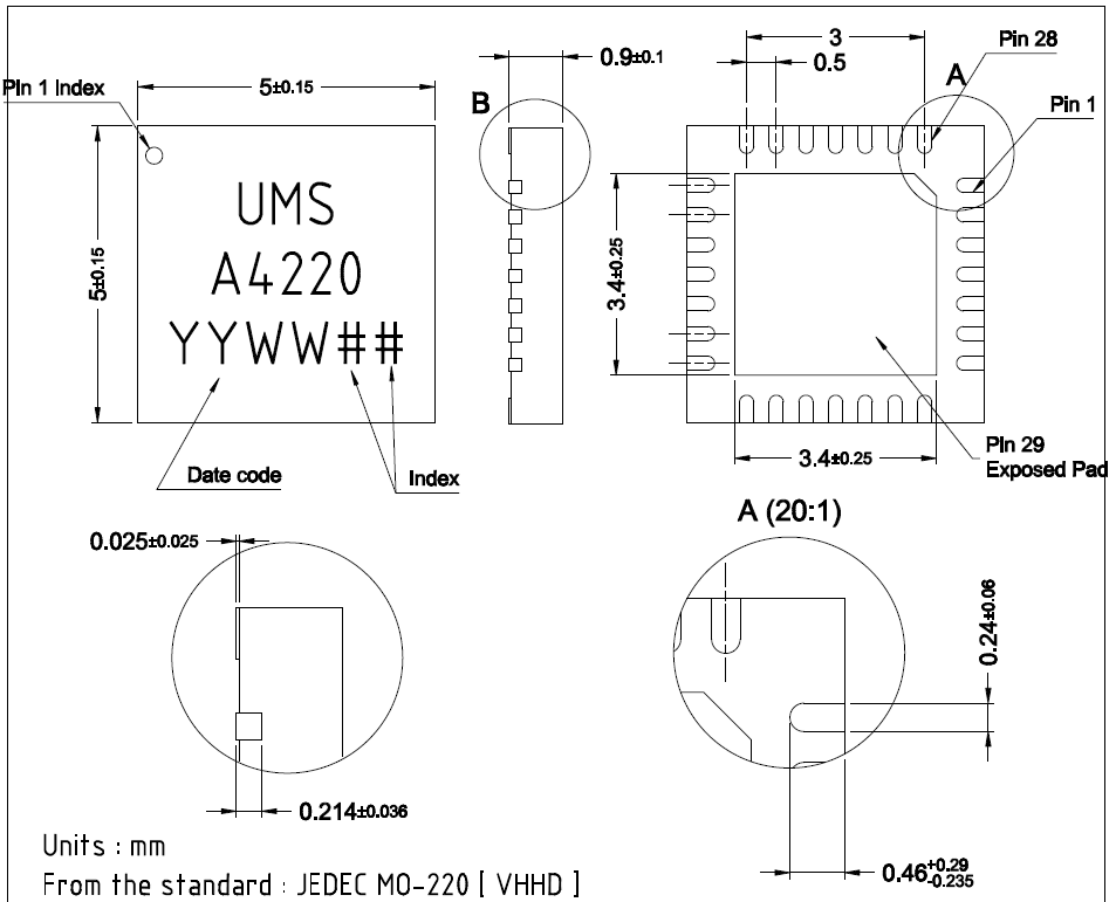
Package outline: 28 Leads 5x5 QFN (1)



Matte tin, Lead Free	(Green)	1- VG2	11- GND(2)	21- Nc
Units :	mm	2- Nc	12- VG1	22- Nc
From the standard :	JEDEC MO-220 (VHHD)	3- Nc	13- ACG4	23- Nc
		4- RF in	14- ACG3	24- Nc
29-	GND	5- GND(2)	15- Nc	25- Nc
		6- Nc	16- Nc	26- ACG2
		7- Nc	17- Nc	27- ACG1
		8- Nc	18- GND(2)	28- Nc
		9- Nc	19- RF out +VD	
		10- Nc	20- Nc	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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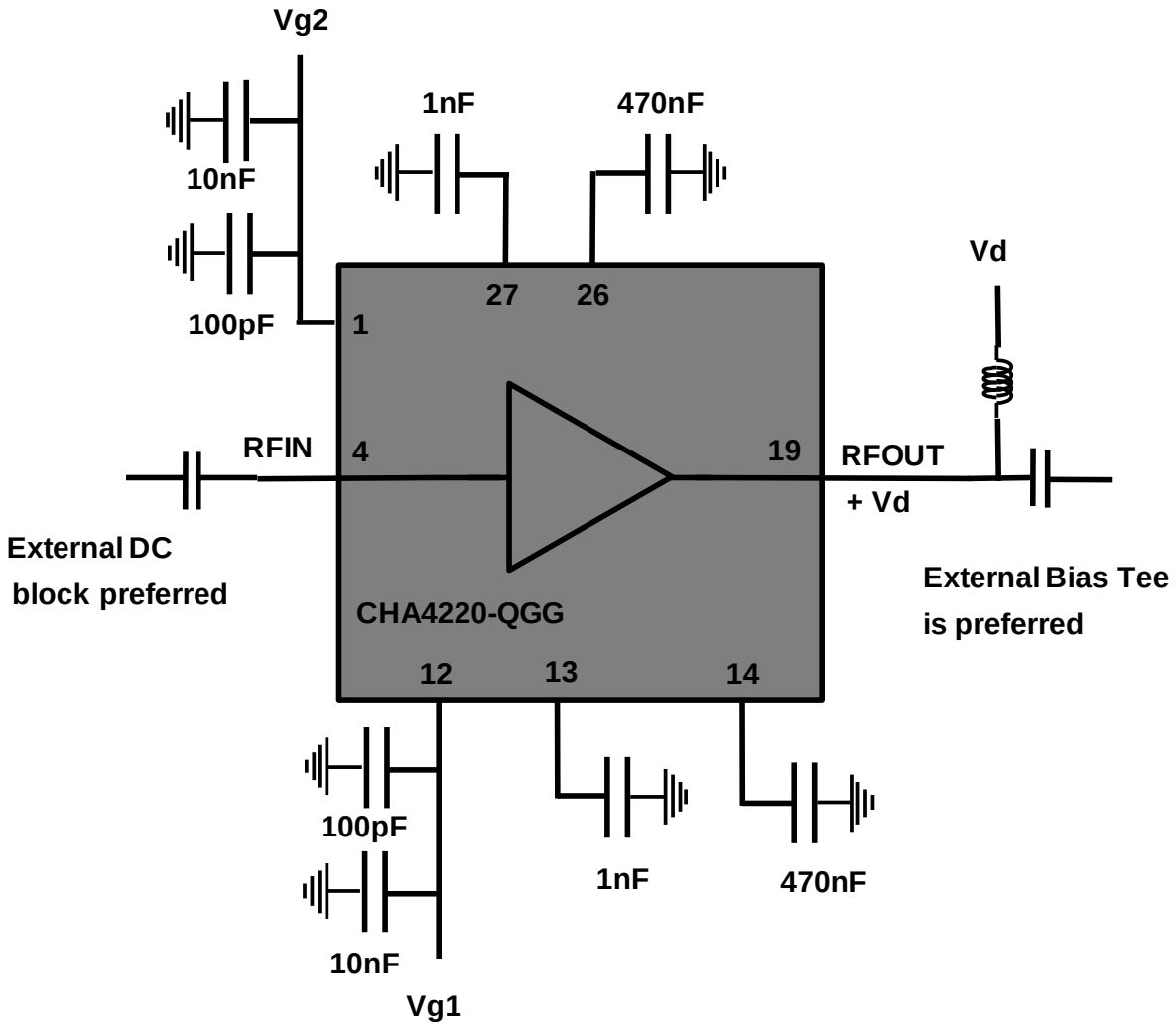
Application Circuit:



Note: external components are requested in order to use the part properly: on RF input access a DC block is requested, on RF output access a Bias Tee is requested.
Depending on the board, additional capacitors such as 1µF may be added on Vg1 or Vg2 access if necessary, for better low frequency decoupling.
Smaller capacitors than 470nF could be use if the part is not use in low frequency range (< 1 GHz): 10nF.

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Pin Description:

Pin	Symbol	Description
5,18, 29 (exposed PAD)	GND	Must be grounded properly, internal connections to ground are made
2,3,6,7,8,9,10,15, 16,17,20,21,22,23,24,25,28	NC	No internal connections
4	RF IN	RF input, DC coupled to Vg1
12	VG1	Gate voltage, bias network required
1	VG2	Gate voltage bias network required
19	RF OUT + VD	RF output + Vd bias (see application circuit)
13	AGC4	Low frequency termination4 on Vg1
14	AGC3	Low frequency termination3 on Vg1
26	AGC2	Low frequency termination2 on Vd
27	AGC1	Low frequency termination1 on Vd

UMS recommends also to ground Pin 2, 3, 6, 7, 11, 15, 16, 17, 20, 21 (see proposed footprint p14).

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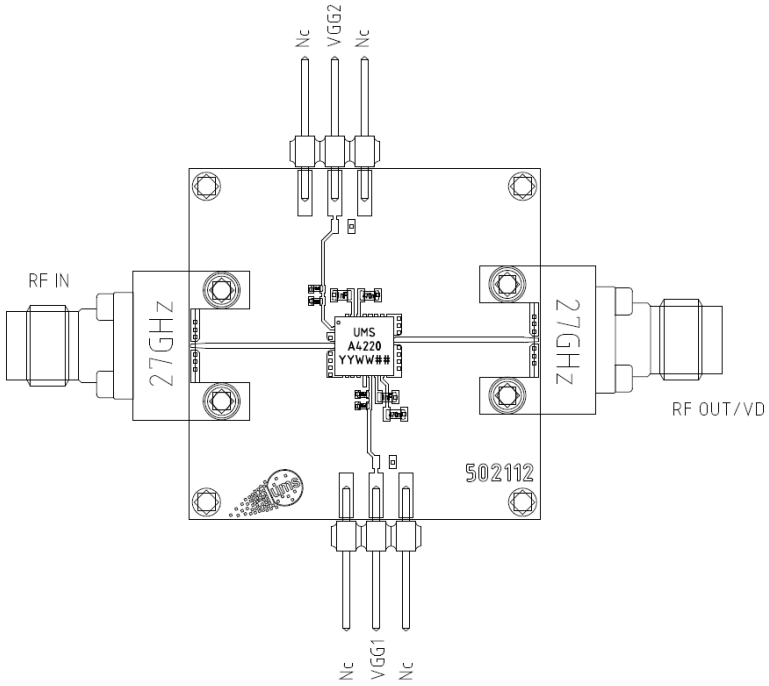
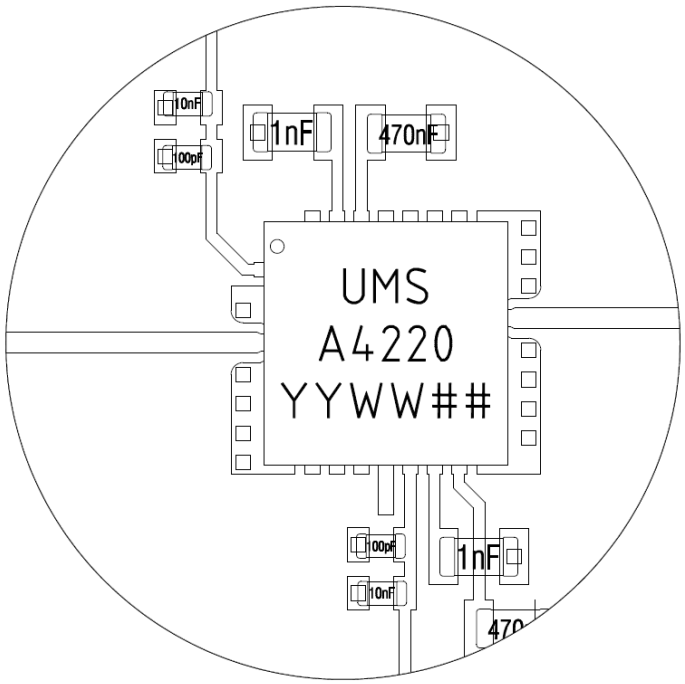
Proposed Evaluation Board

Compatible with the proposed footprint on page p14.
Top dielectric material is Rogers 4003 / 8mils or equivalent substrate.
Decoupling capacitors at first level are 100pF on Vg1 and Vg2.
Decoupling capacitors at second level are 10nF on Vg1 and Vg2.
Additional capacitors such as 1µF may also be added on each Vg accesses.
Low frequency terminations are closed on 1nF and 470nF (proposal)





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Device Operation

Device Power Up instructions:

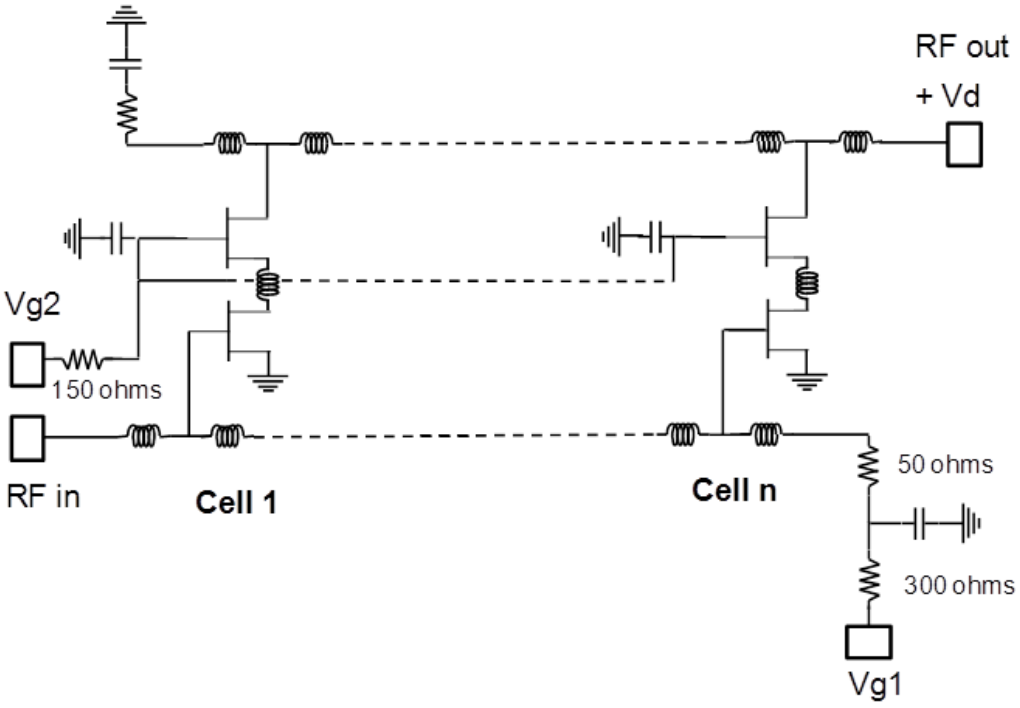
1) Ground the device.
2) Set Vg1 to -1.5V.
3) Set Vd to 6.5V (nominal value for Vd).
4) Set Vg2 to 1.5V (nominal value for Vg2).
5) Set Vg1 in the range of -0.3V for having Idq=120mA.
6) Apply RF input power and adjust Vg2 to obtain desired gain.

Device Power Down instructions:

1) Turn RF power supply off.
2) Set Vg1 to -1.5V in order to get Idq=0mA.
3) Set Vg2 to 0V.
4) Set Vd to 0V.
5) Set Vg1 to 0V.

DC Schematic

Vd=6.5V, Vg1=-0.3V, Vg2=1.5V, Idq=120mA



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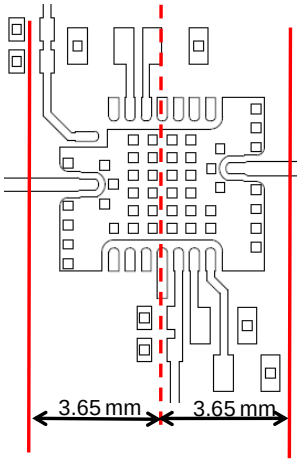
Package footprint and Definition of the measurements planes

The reference planes used for the provided measurements are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.65 mm offset (input wise and output wise respectively) from this axis.

From the edge of the QFN, the reference planes are 1.15mm apart.



Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

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Note

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 28L 5x5 package:	CHA4220-QGG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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