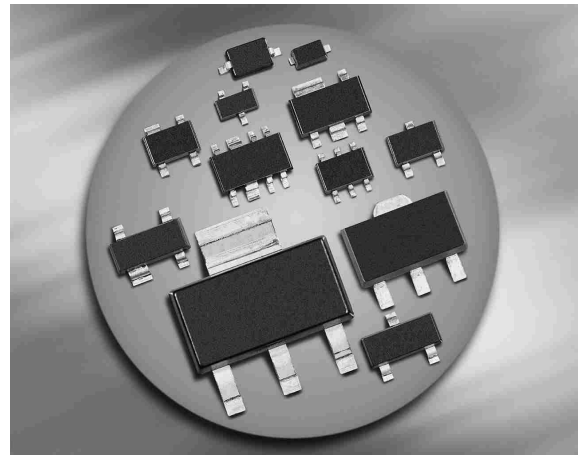
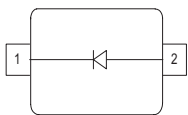


Silicon Schottky Diodes

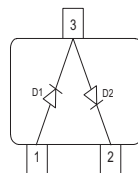
- Low barrier type for DBS mixer applications up to 12 GHz, phase detectors and modulators
- Low noise figure
- Pb-free (RoHS compliant) package



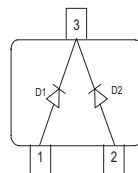
BAT15-02EL
BAT15-02ELS
BAT15-03W



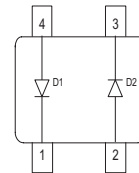
BAT15-04W



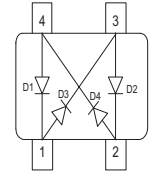
BAT15-05W



BAT15-099



BAT15-099R



ESD (Electrostatic discharge) sensitive device, observe handling precaution!

Type	Package	Configuration	L_S (nH)	Marking
BAT15-02EL	TSLP-2-19	single, leadless	0.4	NN
BAT15-02ELS	TSSLP-2-3	single, leadless	0.2	S underline
BAT15-03W	SOD323	single	1.8	white P
BAT15-04W	SOT323	series	1.4	S8s
BAT15-05W	SOT323	common cathode	1.4	S5s
BAT15-099	SOT143	anti-parallel pair	2	S5s
BAT15-099R	SOT143	cross-over ring	2	S6s

Maximum Ratings at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	4	V
Forward current	I_F	110	mA
Total power dissipation BAT15-02ELS, $T_S \leq 73\text{ °C}$ BAT15-02EL, $T_S \leq 76\text{ °C}$ BAT15-03W, $T_S \leq 70\text{ °C}$ BAT15-04W, $T_S \leq 68\text{ °C}$ BAT15-05W, $T_S \leq 65\text{ °C}$ BAT15-099, $T_S \leq 48\text{ °C}$ BAT15-099R, $T_S \leq 67\text{ °C}$	P_{tot}	100 100 100 100 100 100 100	
Junction temperature	T_j	150	°C
Operating temperature range	T_{op}	-55 ... 150	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾ BAT15-02ELS BAT15-02EL BAT15-03W BAT15-04W BAT15-05W BAT15-099 BAT15-099R	R_{thJS}	≤ 770 ≤ 780 ≤ 795 ≤ 820 ≤ 850 ≤ 1020 ≤ 830	

¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Breakdown voltage $I_{(BR)} = 100\text{ }\mu\text{A}$	$V_{(BR)}$	4	-	-	V
Reverse current $V_R = 1\text{ V}$	I_R	-	-	5	μA
Forward voltage $I_F = 1\text{ mA}$ $I_F = 10\text{ mA}$	V_F	0.16 0.25	0.23 0.32	0.32 0.41	V
Forward voltage matching ¹⁾ $I_F = 10\text{ mA}$	ΔV_F	-	-	20	mV

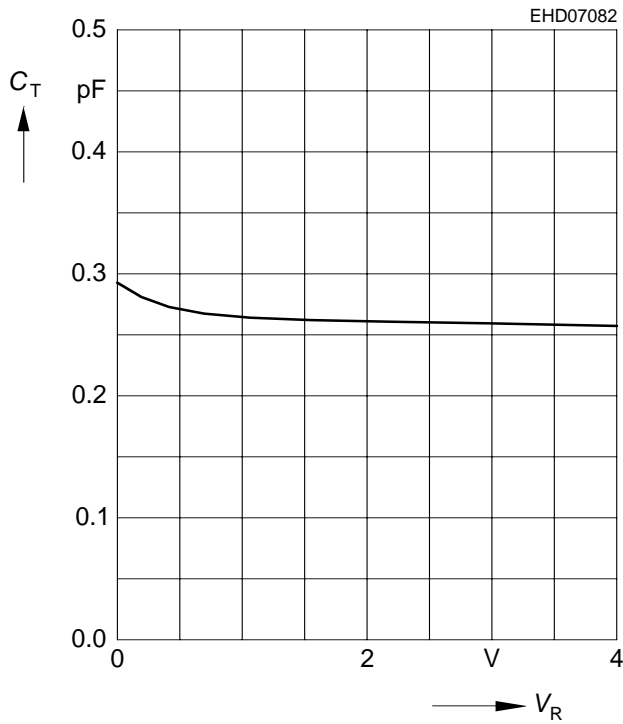
AC Characteristics

Diode capacitance $V_R = 0\text{ V}$, $f = 1\text{ MHz}$, BAT15-02ELS $V_R = 0\text{ V}$, $f = 1\text{ MHz}$, BAT15-099R $V_R = 0\text{ V}$, $f = 1\text{ MHz}$, all others types	C_T	- - -	- - -	0.23 0.5 0.35	pF
Differential forward resistance $I_F = 10\text{ mA} / 50\text{ mA}$	R_F	-	5.5	-	Ω

¹⁾ ΔV_F is the difference between lowest and highest V_F in a multiple diode component.

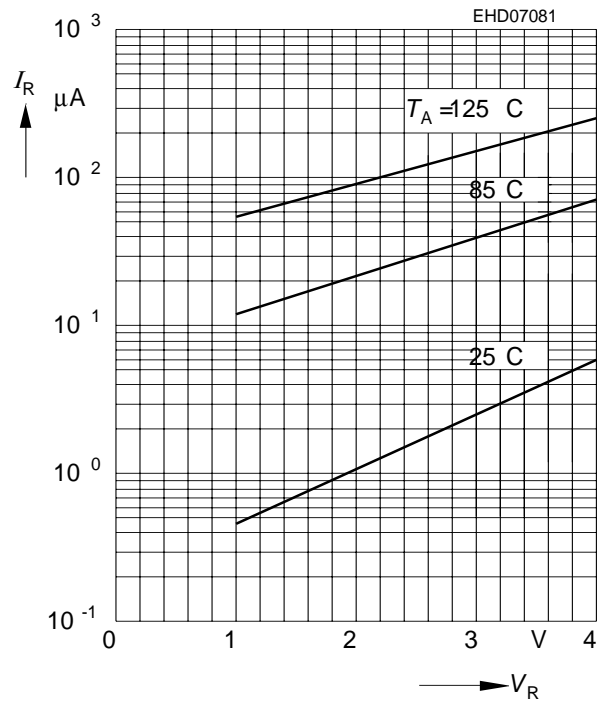
Diode capacitance $C_T = f(V_R)$

$f = 1\text{MHz}$



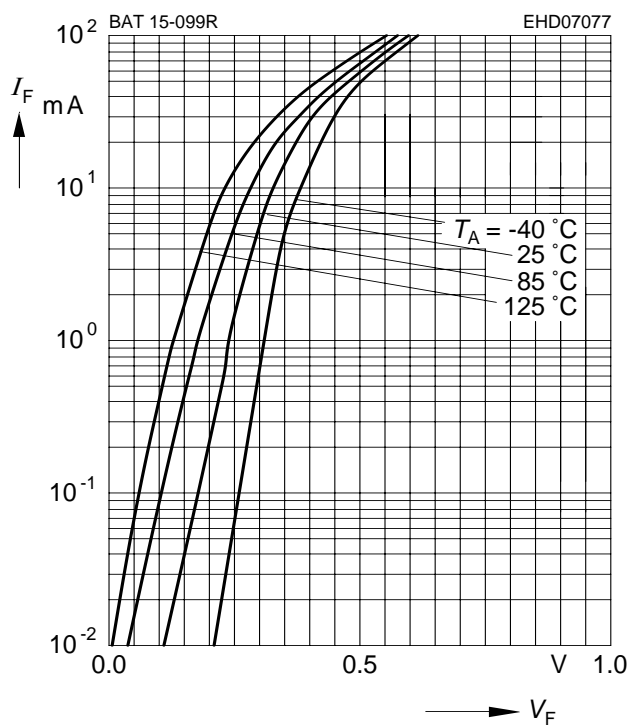
Reverse current $I_R = f(V_R)$

$T_A = \text{Parameter}$



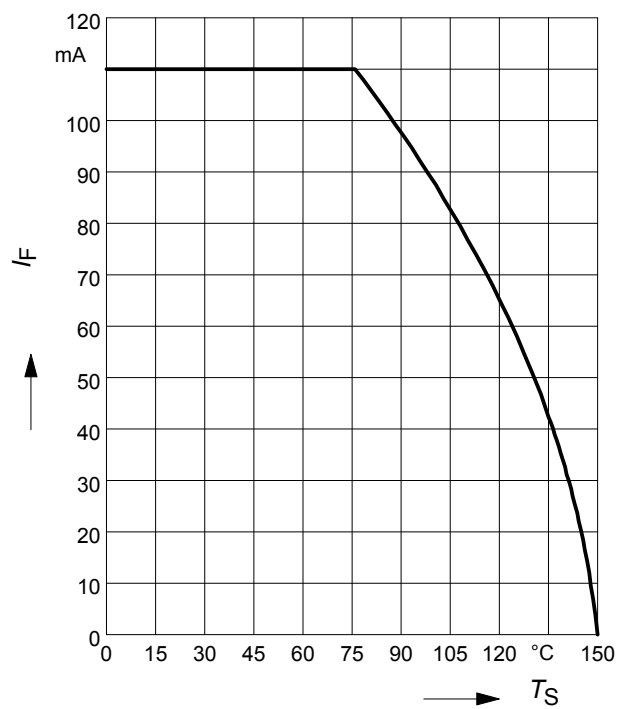
Forward current $I_F = f(V_F)$

$T_A = \text{Parameter}$



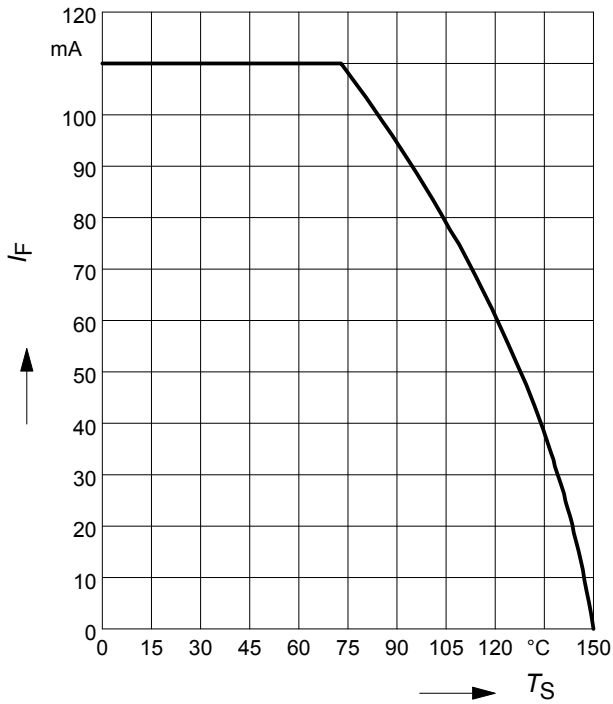
Forward current $I_F = f(T_S)$

BAT15-02EL



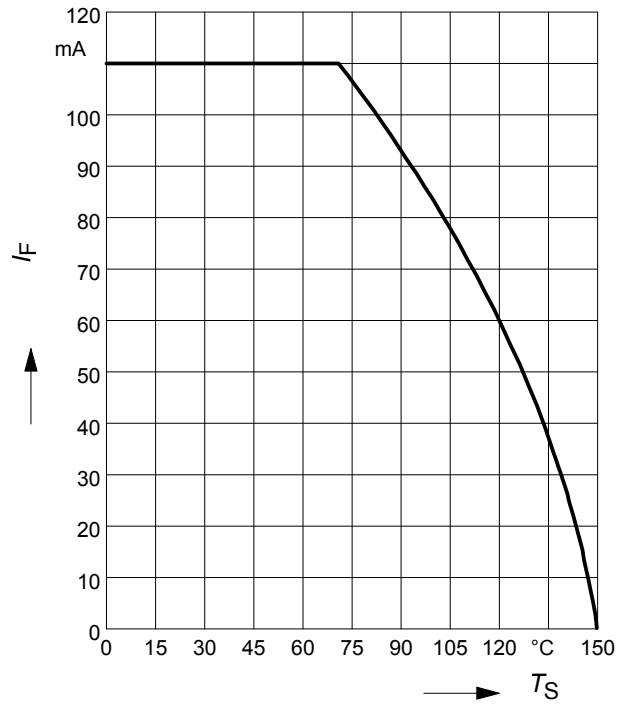
Forward current $I_F = f(T_S)$

BAT15-02ELS



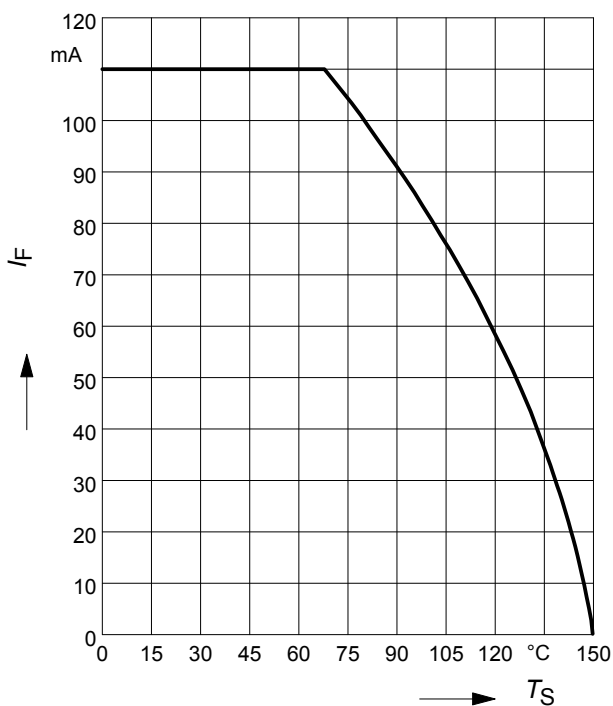
Forward current $I_F = f(T_S)$

BAT15-03W



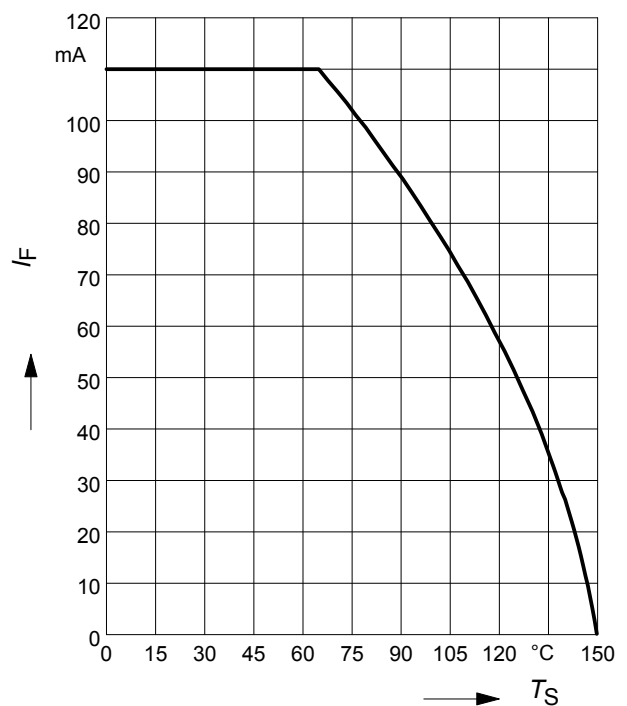
Forward current $I_F = f(T_S)$

BAT15-04W



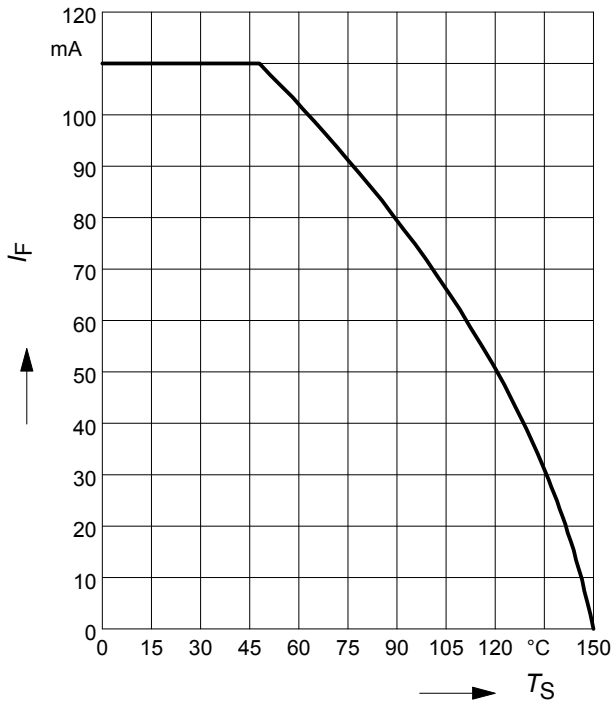
Forward current $I_F = f(T_S)$

BAT15-05W



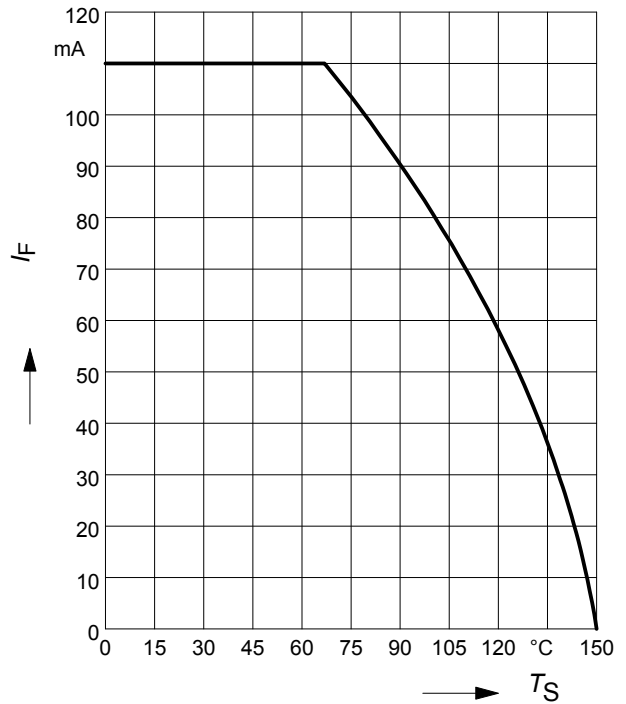
Forward current $I_F = f(T_S)$

BAT15-099



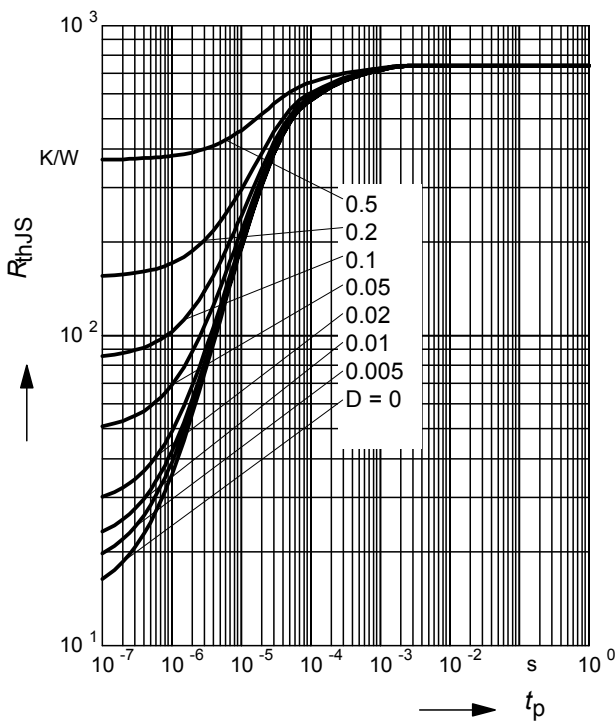
Forward current $I_F = f(T_S)$

BAT15-099R



Permissible Puls Load $R_{thJS} = f(t_p)$

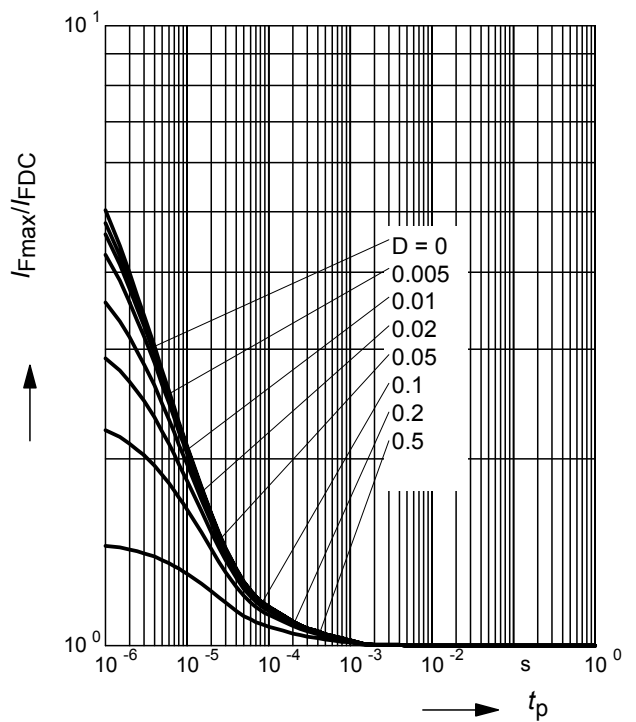
BAT15-02EL



Permissible Pulse Load

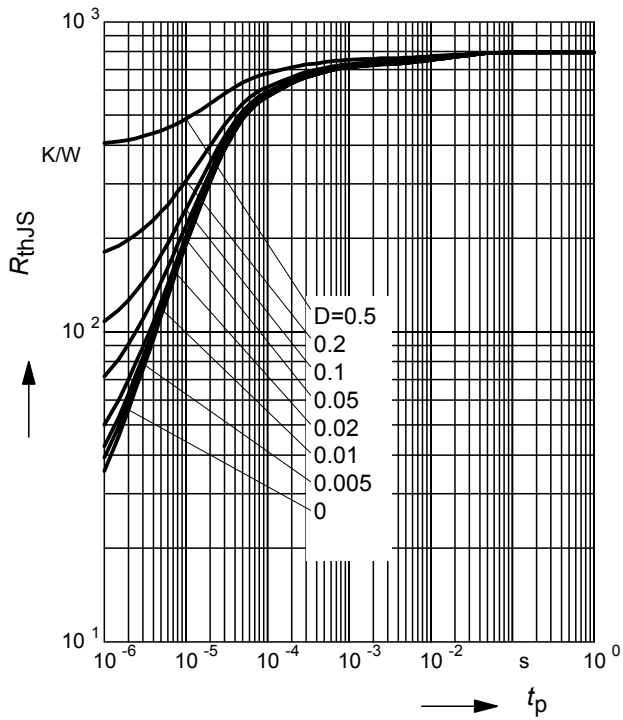
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT15-02EL



Permissible Puls Load $R_{thJS} = f(t_p)$

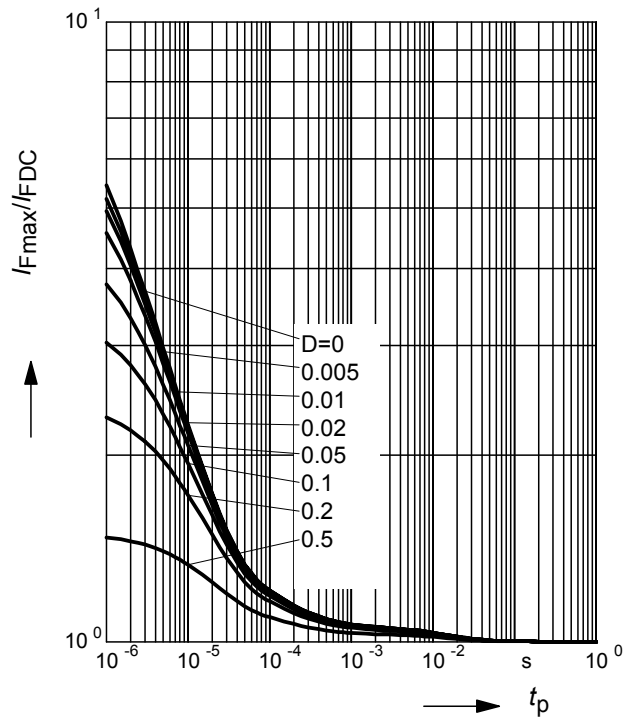
BAT15-03W



Permissible Pulse Load

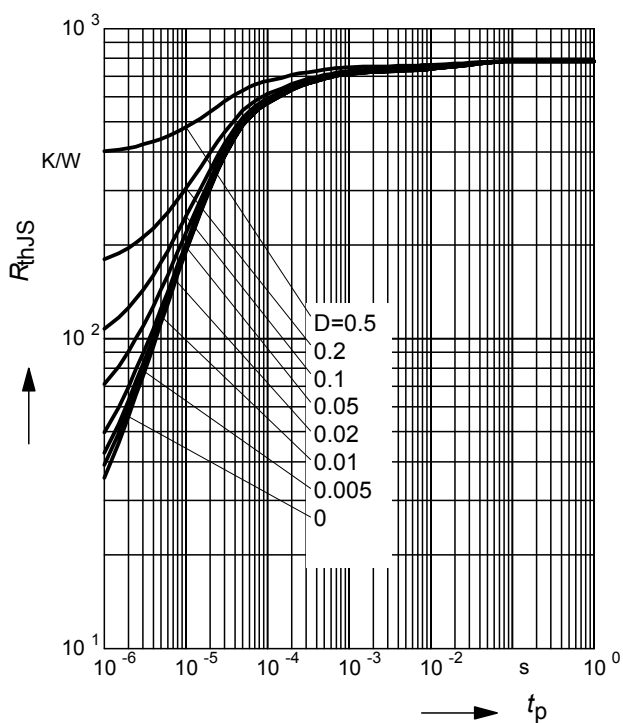
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT15-03W



Permissible Puls Load $R_{thJS} = f(t_p)$

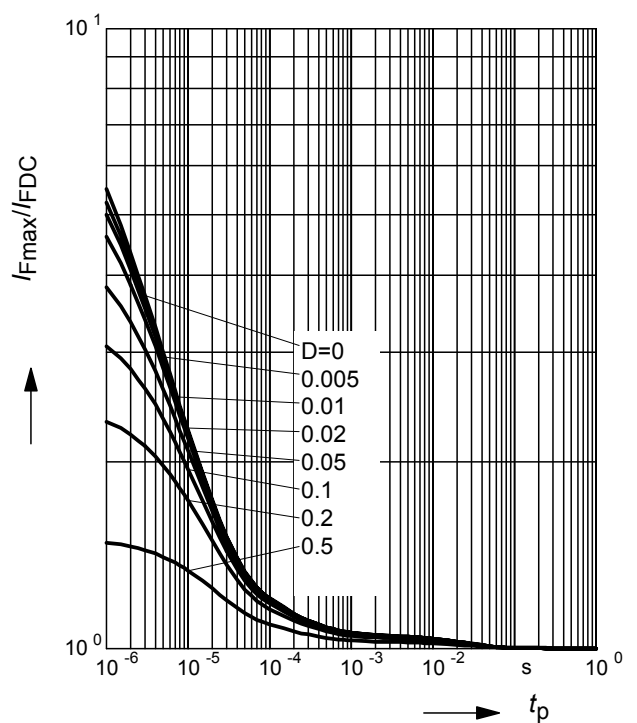
BAT15-04W



Permissible Pulse Load

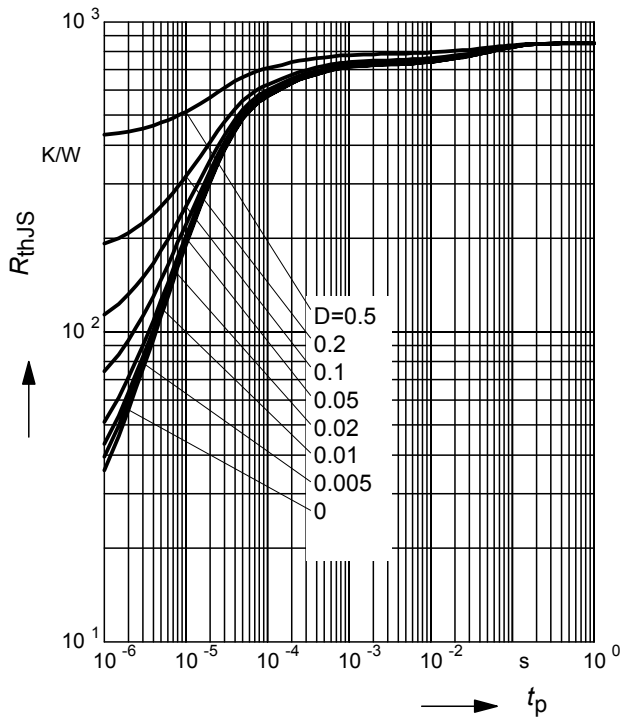
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT15-04W



Permissible Puls Load $R_{thJS} = f(t_p)$

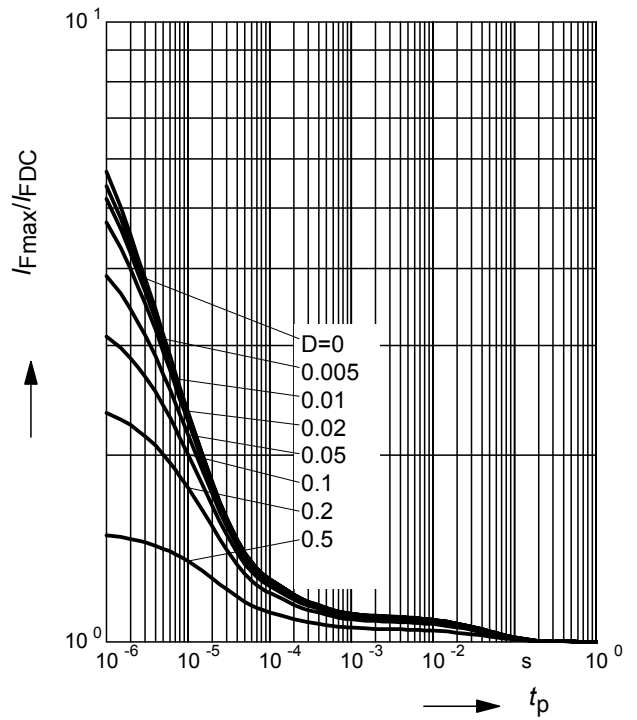
BAT15-05W



Permissible Pulse Load

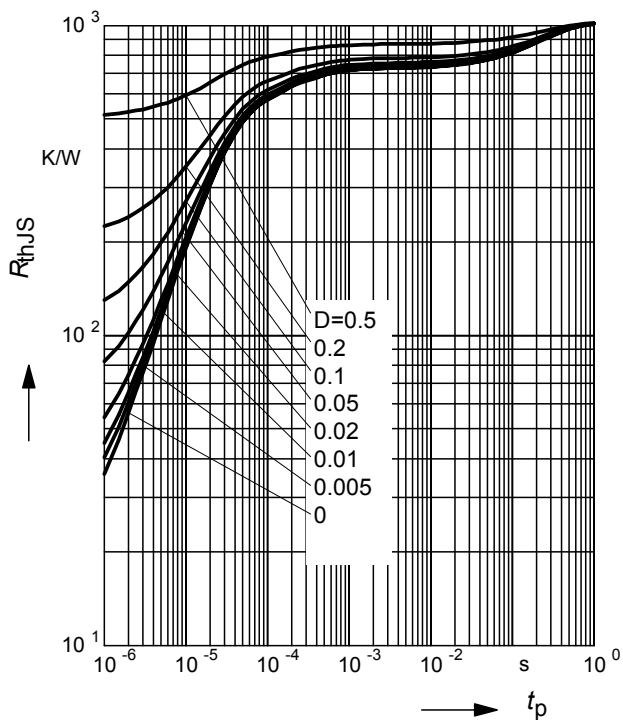
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT15-05W



Permissible Puls Load $R_{thJS} = f(t_p)$

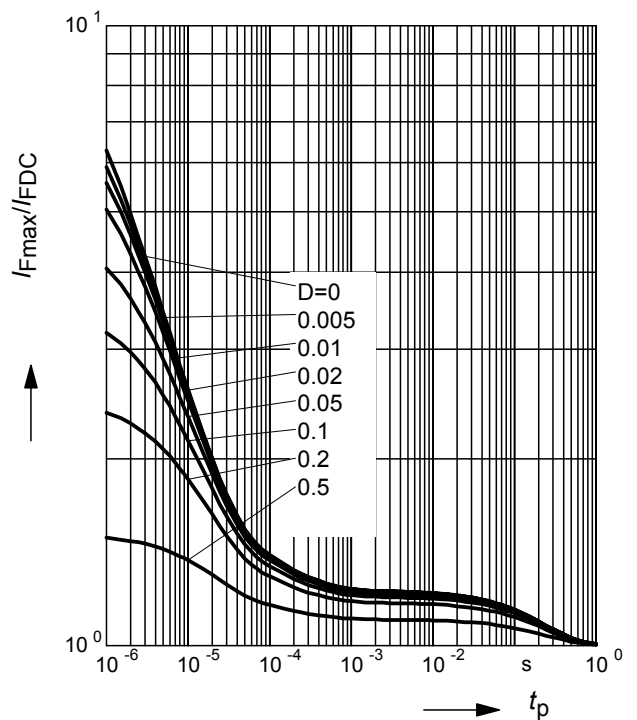
BAT15-099



Permissible Pulse Load

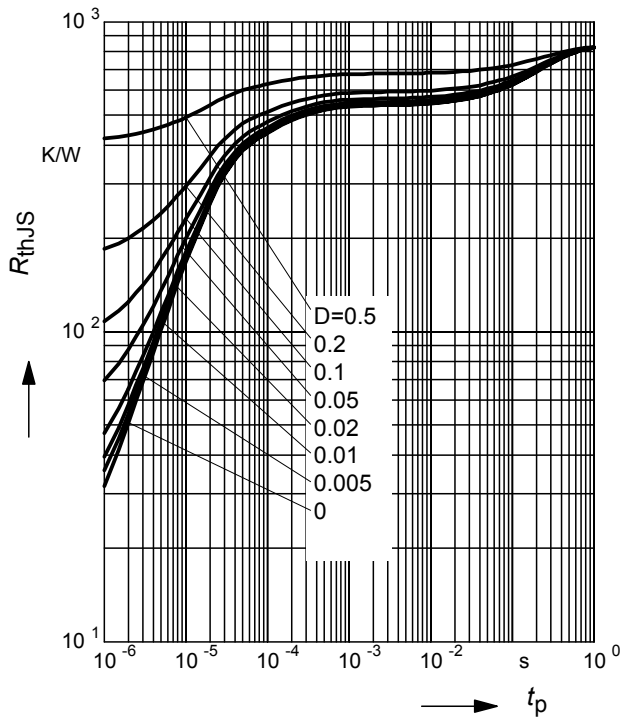
$I_{Fmax} / I_{FDC} = f(t_p)$

BAT15-099



Permissible Puls Load $R_{thJS} = f(t_p)$

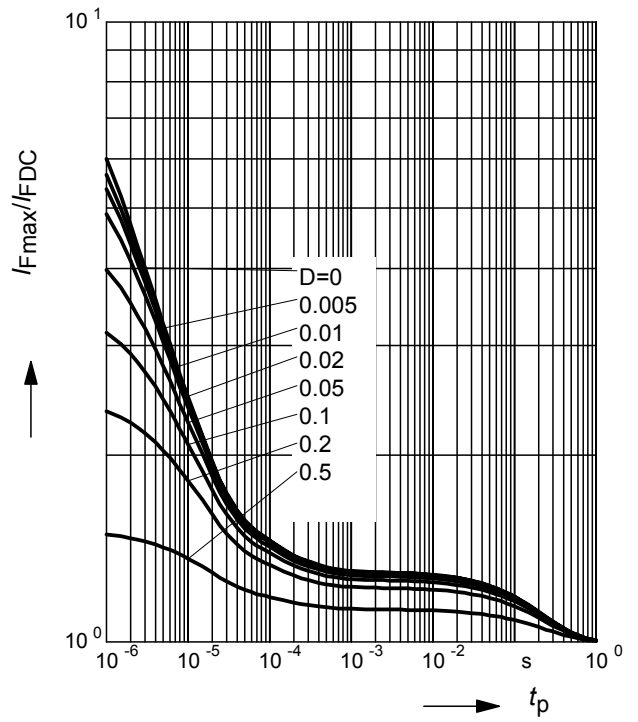
BAT15-099R



Permissible Pulse Load

$I_{Fmax} / I_{FDC} = f(t_p)$

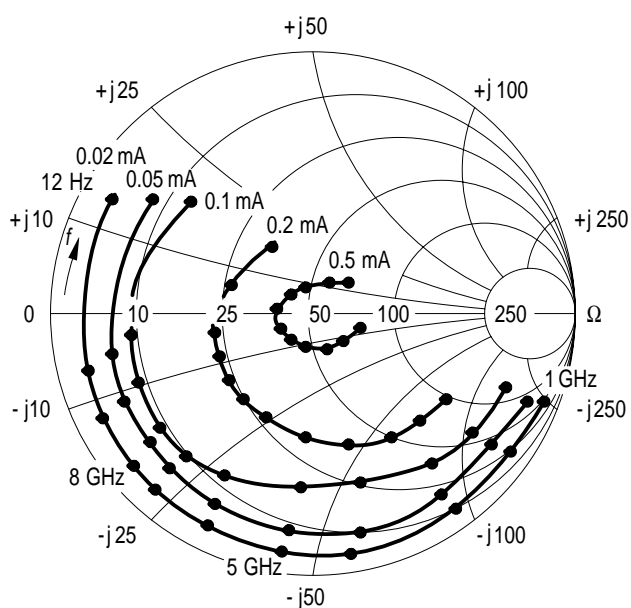
BAT15-099R



S₁₁-Parameters for BAT15-099

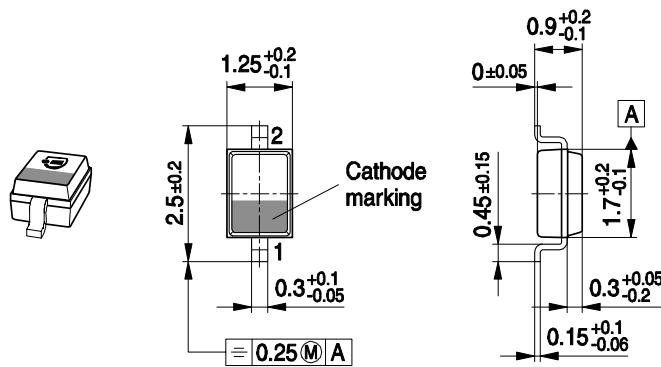
 Typical impedance characteristics (with external bias I and $Z_0 = 50\Omega$)

f	$I = 0.02 \text{ mA}$		$I = 0.05 \text{ mA}$		$I = 0.1 \text{ mA}$		$I = 0.2 \text{ mA}$		$I = 0.5 \text{ mA}$	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1	0.94	-16.4	0.84	-16.6	0.77	-16.4	0.59	-17.2	0.19	-16.7
2	0.93	-33.8	0.88	-33.8	0.77	-34.5	0.58	-35.2	0.15	-36.1
3	0.92	-53.8	0.86	-54.5	0.75	-54.1	0.58	-56.1	0.13	-64.8
4	0.91	-74.3	0.84	-75.3	0.72	-76.4	0.51	-78.4	0.11	-104.8
5	0.91	-96.6	0.84	-97.6	0.72	-99.1	0.53	-102.3	0.15	-135.7
6	0.91	-115.4	0.84	-116.7	0.73	-118.7	0.53	-122.9	0.18	-160.9
7	0.91	-131	0.84	-132.3	0.73	-134.1	0.54	-138.1	0.2	-168.8
8	0.91	-143	0.84	-144.5	0.73	-146.8	0.55	-150.5	0.81	179.4
9	0.91	-155.6	0.83	-150.2	0.71	-159.7	0.53	-163.9	0.18	179.4
10	0.9	-167.3	0.83	-169.7	0.71	-178.8	0.51	-175.8	0.14	151.2
11	0.89	175.5	0.8	172.6	0.7	170	0.45	164.9	0.09	105.5
12	0.88	175.5	0.76	146.5	0.62	142.8	0.39	134.2	0.14	43.6

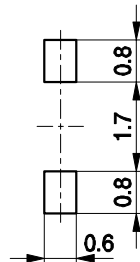
S₁₁ = (f, I) BAT15-099


EHD07083

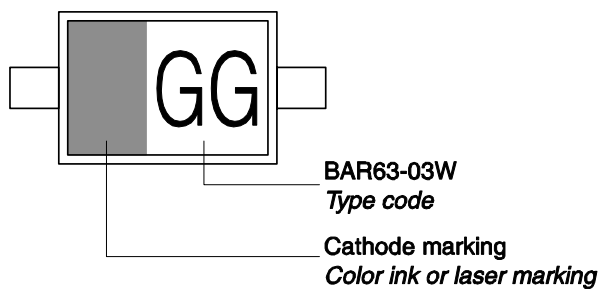
Package Outline



Foot Print

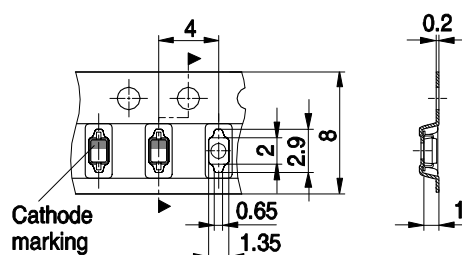


Marking Layout (Example)

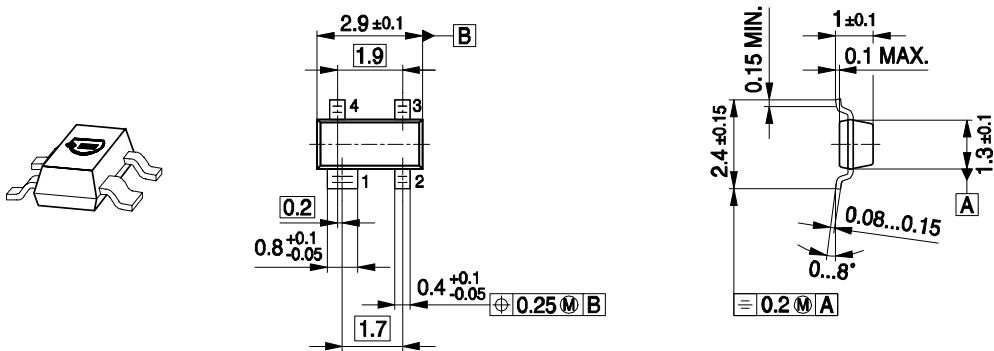


Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø330 mm = 10.000 Pieces/Reel



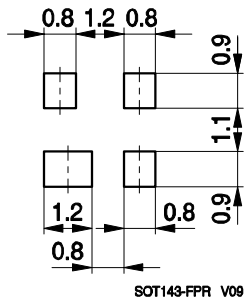
Package Outline



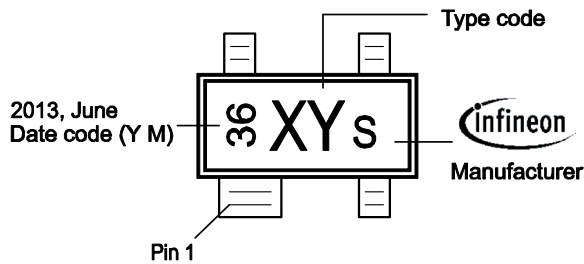
Note: Mold flash, protrusions or gate burrs of 0,2 mm max. per side are not included

SOT143-PO V09

Foot Print

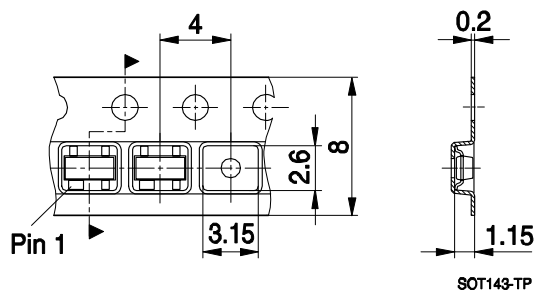


Marking Layout (Example)

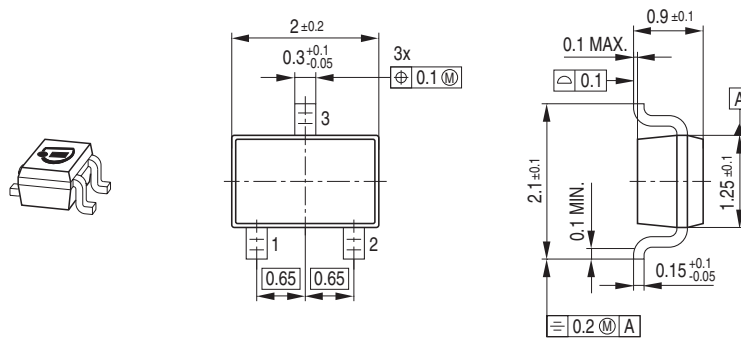


Standard Packing

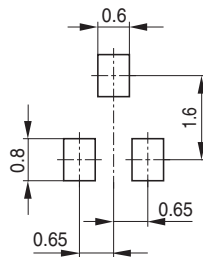
Reel ø180 mm = 3.000 Pieces/Reel
 Reel ø330 mm = 10.000 Pieces/Reel



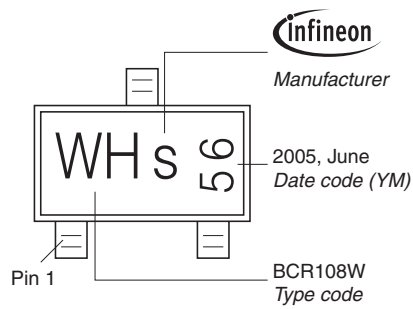
Package Outline



Foot Print

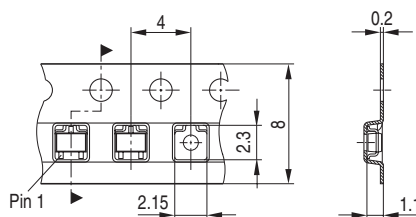


Marking Layout (Example)

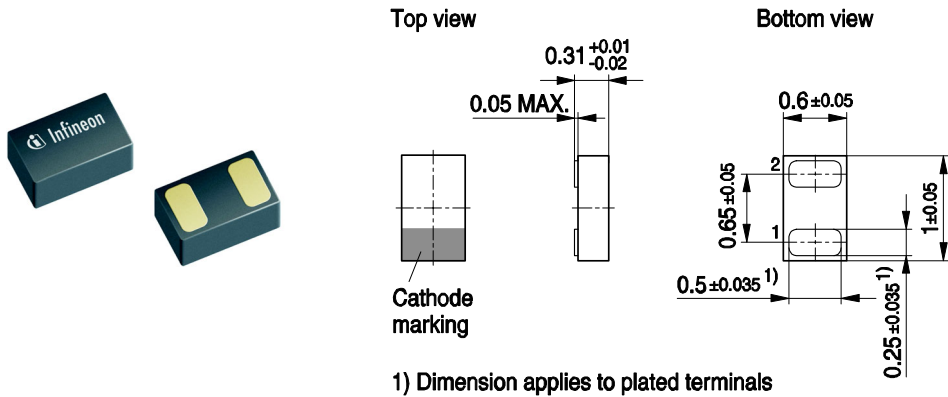


Standard Packing

Reel $\varnothing 180$ mm = 3.000 Pieces/Reel
 Reel $\varnothing 330$ mm = 10.000 Pieces/Reel



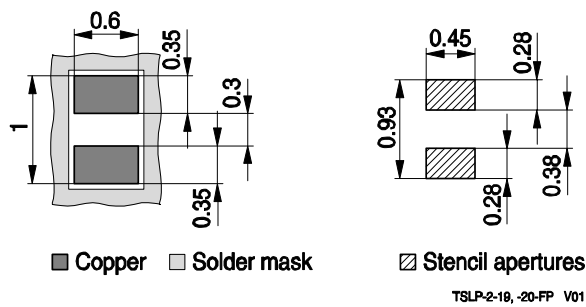
Package Outline



TSLP-2-19, -20-PO V01

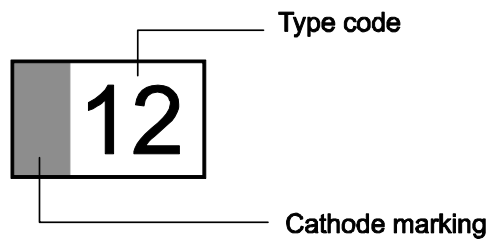
Foot Print

For board assembly information please refer to Infineon website „Packages“



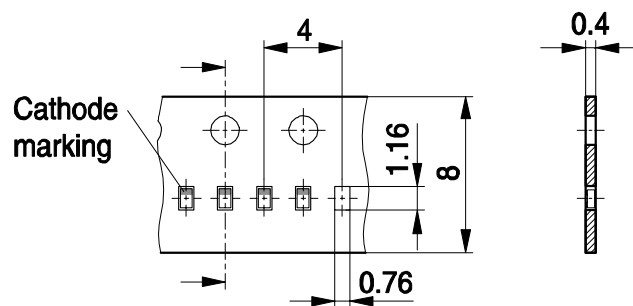
TSLP-2-19, -20-FP V01

Marking layout (Example)



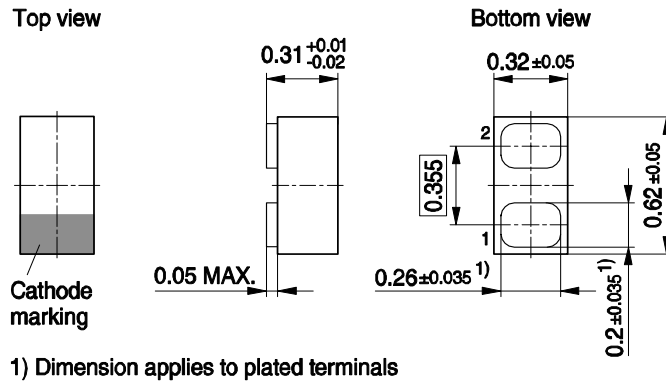
Standard Packing

Reel Ø 180 mm: 15.000 Pieces / Reel
Reels/Box: 1



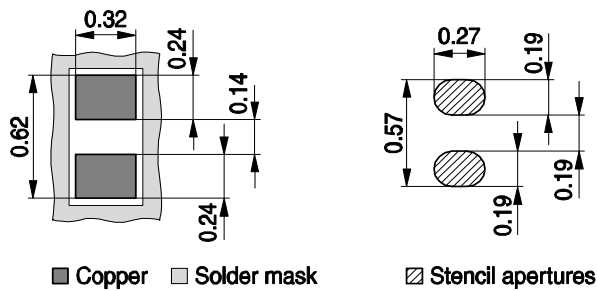
TSLP-2-19, -20-TP V02

Package Outline

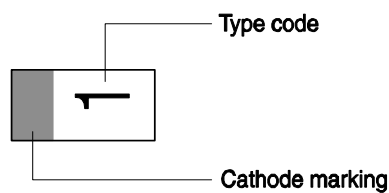


Foot Print

For board assembly information please refer to Infineon website "Packages"

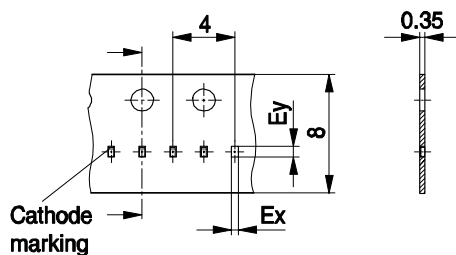


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



Tape type	Ex	Ey
Punched Tape	0.43	0.73
Embossed Tape	0.37	0.67

Deliveries can be both tape types (no selection possible).
Specification allows identical processing (pick & place) by users.

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