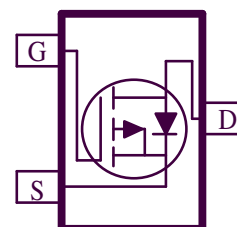
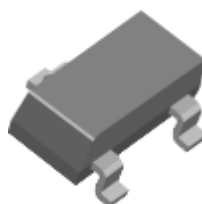


P-Channel 30-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SC70-3 saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
-30	0.112 @ $V_{GS} = -10V$	-1.5
	0.172 @ $V_{GS} = -4.5V$	-1.2



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^a	$T_A = 25^\circ C$	I_D	-1.5	A
	$T_A = 70^\circ C$		-1.2	
Pulsed Drain Current ^b		I_{DM}	-2.5	
Continuous Source Current (Diode Conduction) ^a		I_S	± 0.28	A
Power Dissipation ^a	$T_A = 25^\circ C$	P_D	0.34	W
	$T_A = 70^\circ C$		0.22	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{THJA}	375	$^\circ C/W$
	Steady-State		430	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

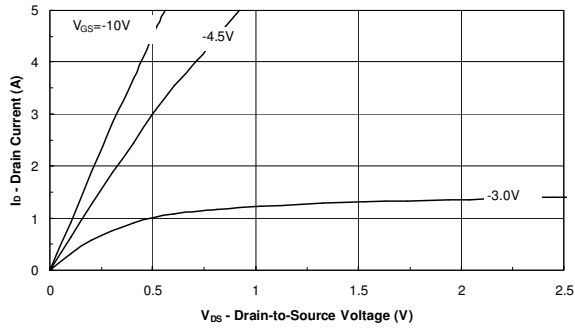
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-1			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -24 V, V _{GS} = 0 V, T _J = 55°C			-10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-5			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -10 V, I _D = -1.5 A			112	nΩ
		V _{GS} = -4.5 V, I _D = -1.2 A			172	
Forward Transconductance ^A	g _s	V _{DS} = -5 V, I _D = -1.5 A		9		S
Diode Forward Voltage	V _{SD}	I _S = -0.46 A, V _{GS} = 0 V		-0.65		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -5 V, I _D = -1.5 A		7.2		nC
Gate-Source Charge	Q _{gs}			1.7		
Gate-Drain Charge	Q _{gd}			1.5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, I _L = -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		10		ns
Rise Time	t _r			9		
Turn-Off Delay Time	t _{d(off)}			27		
Fall-Time	t _f			11		

Notes

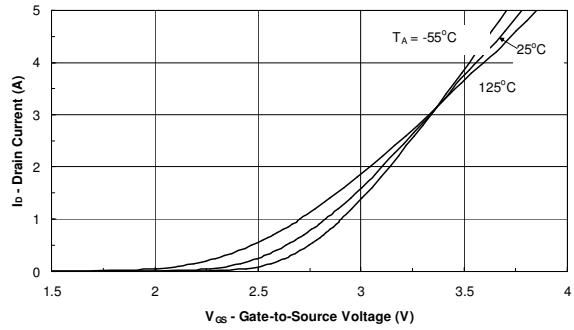
- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Repetitive rating, pulse width limited by junction temperature.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typical" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

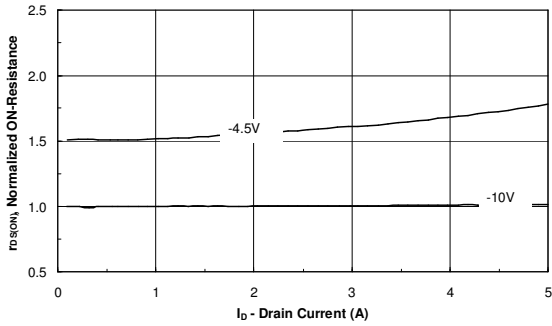
Typical Electrical Characteristics (P-Channel)



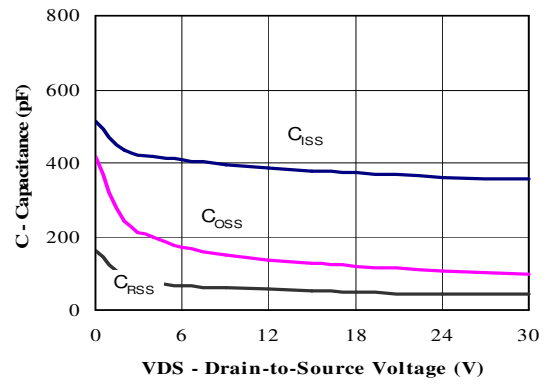
Output Characteristics



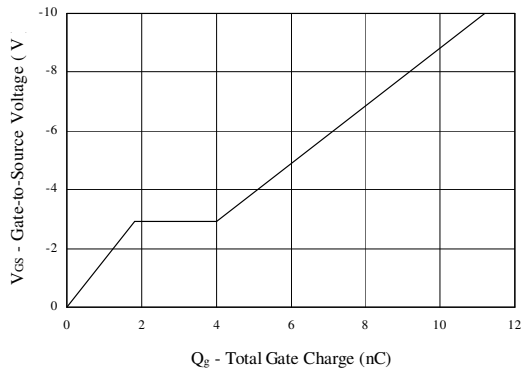
Transfer Characteristics



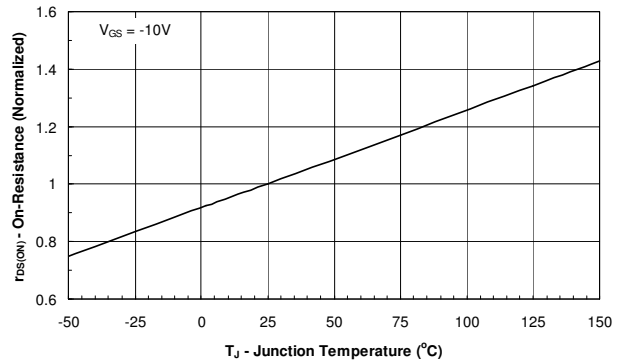
On-Resistance vs. Drain Current



Capacitance

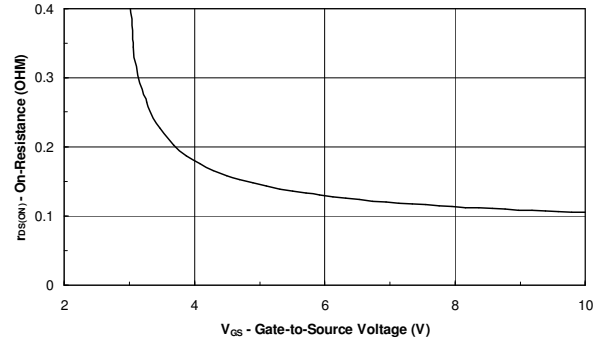
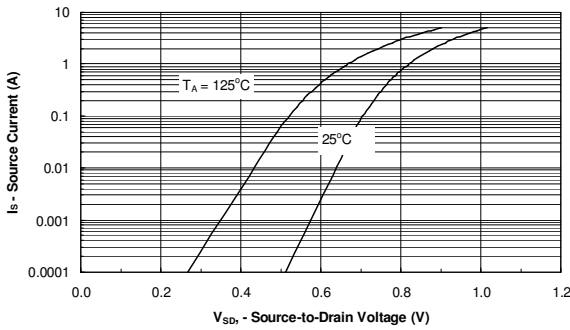


Gate Charge

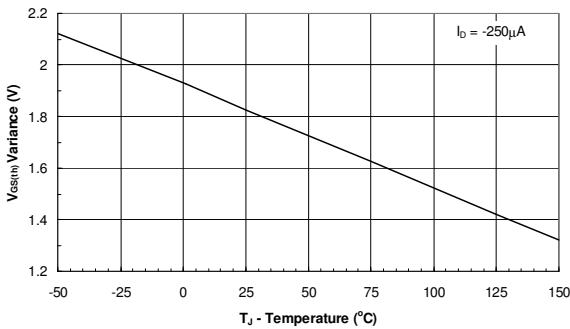


On-Resistance vs. Junction Temperature

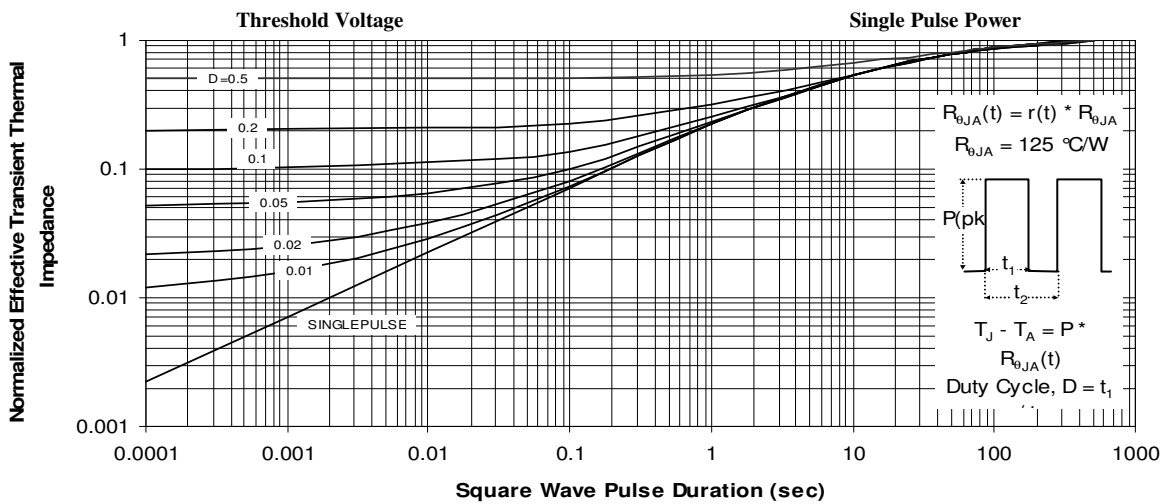
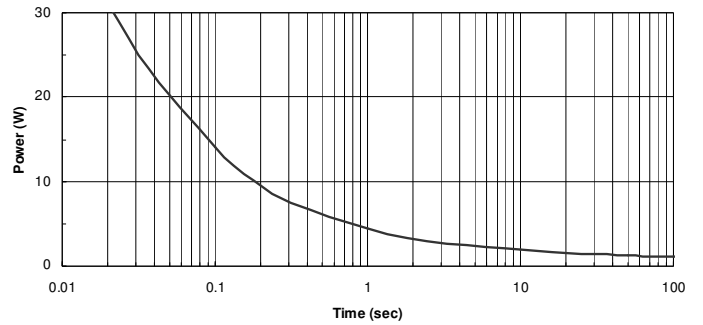
Typical Electrical Characteristics (P-Channel)



Source-Drain Diode Forward Voltage



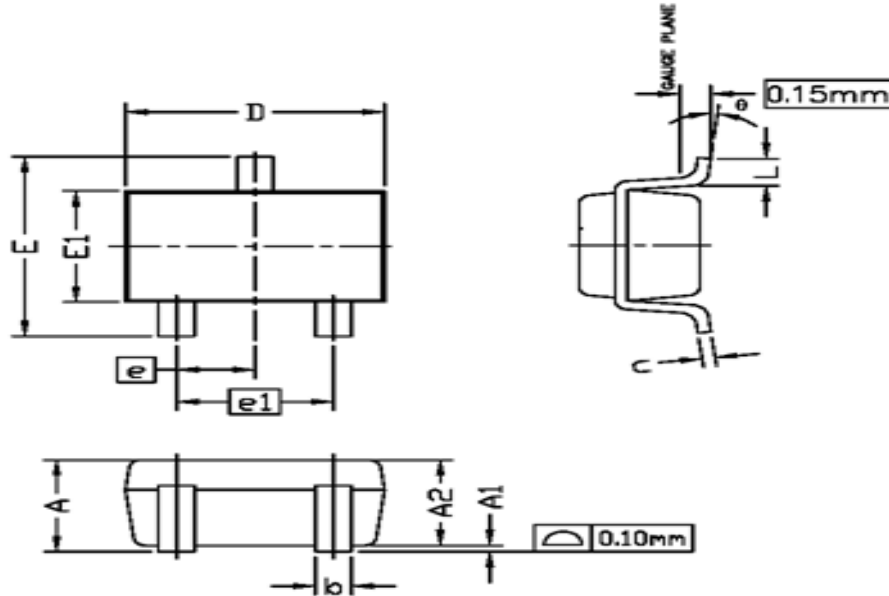
On-Resistance vs. Gate-to Source Voltage



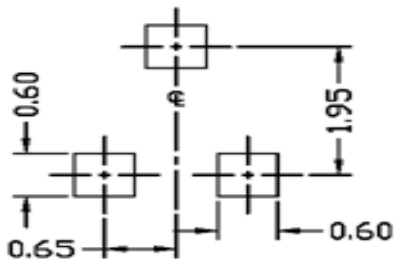
Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Information

SC70 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.10			0.043
A1	0.00		0.10	0.00		0.004
A2	0.7	0.9	1.00	0.028	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.08		0.22	0.003		0.009
D	1.85	2.10	2.15	0.073	0.083	0.085
E	1.80	2.30	2.40	0.071	0.091	0.094
e	0.65 BSC			0.026 BSC		
e1	1.30 BSC			0.051 BSC		
E1	1.1	1.30	1.4	0.043	0.051	0.055
L	0.26	0.36	0.46	0.010	0.014	0.018
θ	0°	4°	8°	0°	4°	8°

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 3 MILS EACH.
4. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM.
ie: REVERSE TRIM/FORM.
5. DIMENSION L IS MEASURED IN GAUGE PLANE.
6. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.