Rev: 102108

DS33M33 Demo Kit

General Description

The DS33M33 demo kit (DK) is an easy-to-use evaluation board for the DS33M33 and the DS33M33 Ethernet-over-SONET/SDH devices. The demo kit contains an option for either T3 or E3. The T3E3 links are complete with line interface, transformers, and network connections. Maxim's ChipView software is provided with the demo kit, giving point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal, queue overflow, Ethernet link, Tx/Rx, and interrupt status.

Windows is a registered trademark of Microsoft Corp.

Demo Kit Contents

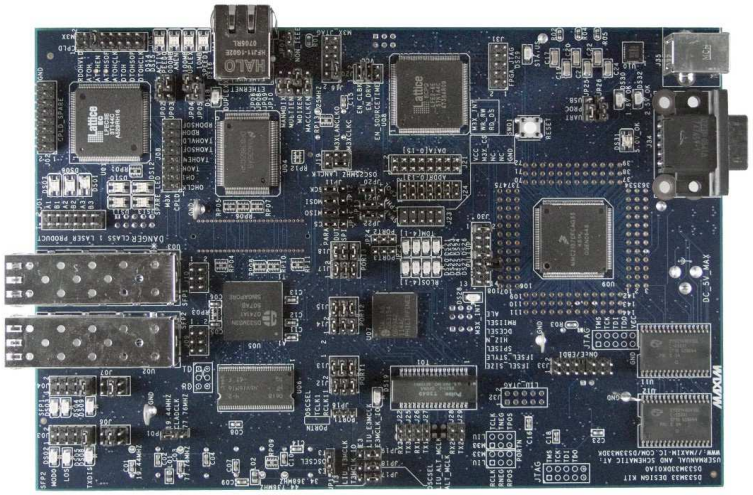
DS33M33DK Board
CD Including:
- ChipView Software
- DS33M33 Definition Files
- DS33M33DK Definition File
- DS33M33DK Data Sheet
- DS33M33 Data Sheet

Features

- **Demonstrates Key Functions of DS33M33 Ethernet Transport Chipset**
- **Includes Ethernet PHY Supporting 10/100 and Gigabit Modes**
- **Includes Optical SFP Module for SONET/SDH Interface**
- **Network Connectors, Transformers, and Termination Ease Connectivity**
- **Careful Layout Provides Signal Integrity**
- **On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS33M33 and DS3154 Register Set**
- **Software-Controlled (Register Mapped) Configuration Switches Facilitate Clock and Signal Routing**
- **All System Side and Overhead Pins are Easily Accessible for External Data Source/Sink**
- **LEDs Programmed Through GPIO Pins Provide Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

Ordering Information

PART	TYPE
DS33M33DK	Demo Kit for DS33M33



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Downloaded from: http://www.datasheetcatalog.com/

Table of Contents

1. BOARD FLOORPLAN 3
2. PC BOARD ERRATA 3
3. FILE LOCATIONS 4
4. BASIC OPERATION 5
   - 4.1 POWERING UP THE DEMO KIT 5
     - *4.1.1 General 5*
   - 4.2 BASIC DS33M33 INITIALIZATION 5
     - *4.2.1 Additional configuration for DS33M33 ..... 5*
   - 4.3 MONITOR AND CAPTURE ETHERNET TRAFFIC 5
5. JUMPERS AND CONNECTORS 6
6. LINE-SIDE CONNECTIONS 9
7. SYSTEM CONNECTORS 9
8. MICROCONTROLLER 9
9. POWER-SUPPLY CONNECTORS 9
10. CONNECTING TO A COMPUTER 9
11. INSTALLING AND RUNNING THE SOFTWARE 10
12. ADDRESS MAP 11
    - 12.1 OVERHEAD CPLD REGISTER MAP 11
    - 12.2 CONTROL AND STATUS REGISTERS 12
13. ADDITIONAL INFORMATION/RESOURCES 16
    - 13.1 DS33M33 INFORMATION 16
    - 13.2 DS33M33DK INFORMATION 16
    - 13.3 TECHNICAL SUPPORT 16
14. COMPONENT LIST 16
15. SCHEMATICS 21

List of Figures

Figure 1-1. DS33M33DK Board Floorplan 3
Figure 15-1. DS33M33 PCB Layout and Schematic Hierarchy Block Page Listing 21

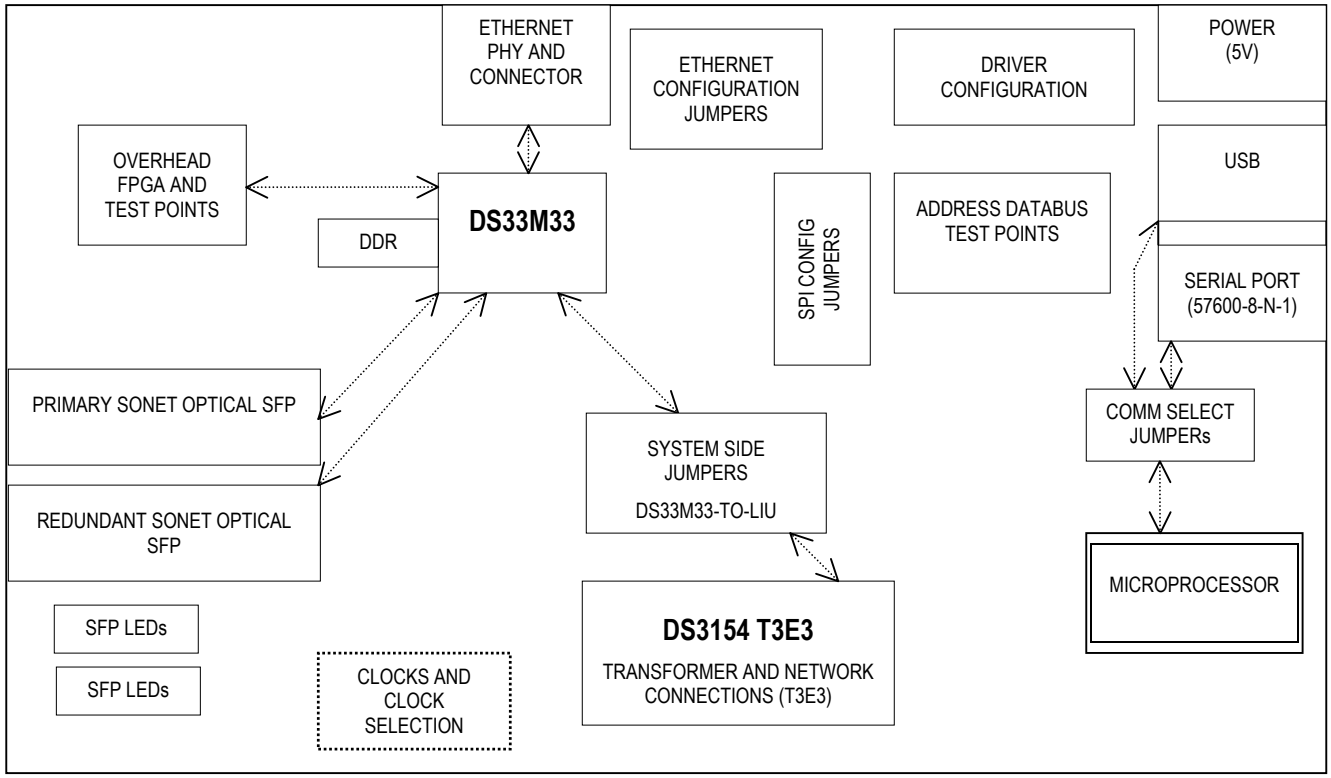
List of Tables

Table 3-1. Definition and Configuration Files 4
Table 5-1. Jumpers and Connectors 6
Table 12-1. Address Map 11
Table 12-2. Register Map for Overhead CPLD (Reference Designator U01) 11

Downloaded from: http://www.datasheetcatalog.com/

1. Board Floorplan

Figure 1-1. DS33M33DK Board Floorplan



2. PCB Errata

There are no errata for the DS33M33DK02A0.

Downloaded from: http://www.datasheetcatalog.com/

3. File Locations

This demo kit relies upon several supporting files, which are provided on the CD and are available as a zip file from the Maxim website www.maxim-ic.com/DS33M33DK. All locations are given relative to the directory in the CD/zip file called "DS33M33_def_ini_". Table 3-1 shows the DS33M33, DS3154, and FPGA register definition files and configuration files.

Table 3-1. Definition and Configuration Files

FILE NAME	FILE USAGE
. \parallel_mode\ _DS33M_GlobalSonet.def	Top level definition file to select in ChipView's register mode. This file will autoload the remaining definition files for the DS33M33 when parallel mode is used. (Note the wan files still need to be loaded (either DS)).
.\parallel_mode\DS3154DC.def .\parallel_mode\ds33M_BufferMan.def .\parallel_mode\ds33M_EncapDecap.def .\parallel_mode\ds33M_GlobalEth.def .\parallel_mode\ds33M_group.def .\parallel_mode\ds33M_LanSubscriber.def .\parallel_mode\DS33M_port1.def .\parallel_mode\DS33M_port2.def .\parallel_mode\DS33M_port3.def .\parallel_mode\DS33M_serial_1234.def .\parallel_mode\DS33M_TEST.def .\parallel_mode\ds33M_Vcat.def .\parallel_mode\Overhead_FPGA.def	DS33M33 dependent files. These are called by _DS33M_GlobalSonet.def file, which is listed above.
.\parallel_mode\m33_eos_vcg0_port2_port3_mii.mfg	File for manually configuring the DS33M33 for EoS VC3 with two ports assigned to VCG1.
.\parallel_mode\m33_eos_vc3_mii100.mfg	File for manually configuring the DS33M33 for EoS VC3 mode.
.\parallel_mode\m33_eopos_ds3.mfg	File for manually configuring the DS33M33 for EoPoS DS3 mode.
.\parallel_mode\enc_dec_lb.mfg	Encap/decap loopback/
.\parallel_mode\m30_rx_tx.mfg	M30 mode Rx and Tx configuration. This file configures the MAC for GMII mode and requires a Gigabit Ethernet link.
.\parallel_mode\norm_ds3154_dlb.mfg .\parallel_mode\m33_pos_au3_liu.mfg	Two files for configuring the LIU in M33 mMode and configuring the DS33M33 in PoS AU3 mode.
.\ spi_mode.zip	Configuration mode files for SPI™ 3-wire bus mode. The default mode for this demo kit is parallel mode. To avoid accidental use the SPI mode files have been provided in a zip format.
.\ ParitalConfig_DS33M_100mBit.mfg .\ ParitalConfig_DS33M_GigaBit.mfg	Files to change Ethernet speed in the MAC and Global Ethernet section.

SPI is a trademark of Motorola, Inc.

Downloaded from: http://www.datasheetcatalog.com/

4. Basic Operation

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

4.1 Powering Up the Demo Kit

- Connect PCB power jack to the wall adapter.
- Connect RS232 serial cable, or USB cable between the host PC and demo kit.
- Verify that the jumpers are configured as described in Table 5-1.

4.1.1 General

- Upon power-up the power LEDs (DS30, DS31, DS32 green) will be lit. Note that with DS33M3301A0 board revision, the LED DS31 will be red when power conditions are correct.
- PHY LINK LED should be lit if an Ethernet cable is connected.

Following are several basic system initializations.

4.2 Basic DS33M33 Initialization

This section covers two basic methods for configuring the DS33M33.

1. Device Driver-Based Configuration: (Note: The DS33M3302A0 board revision does not come loaded with device drivers). If the pins J20.1+J20.2 are Jumpered the device driver will auto configure the DS33M33 upon power-up. This enables traffic to pass from the Ethernet port to the serial port. Consult the device driver documentation for further details. To load the GUI interface for the device drivers, go to the ChipView register mode **Tools** menu and select **Tools→Plugins→DS33M30/M33 Device Driver Demo**.
2. Register-Based Configuration: EoS VC3 with two ports assigned to VCG1.
    a. Remove jumper J20.1+J20.2 to disable device drivers, and reset the board.
    b. Launch ChipView.exe and select **Register View**.
    c. When prompted for a definition file, pick the file named **_DS33M33_GlobalMicroport.def**. Several additional definition files will load.
    d. Go to the **File** menu and select **File→Memory Config File→Load .MFG file**. When prompted, select the file named **m33_eos_vcg0_port2_port3_mii.mfg**.

4.2.1 Additional Configuration for DS33M33

- Using either a patch or crossover cable, connect the Ethernet connector to an ordinary PC or network test equipment. This should cause the link LED to turn on.
- Place a loopback connector at the SONET network side; the optical LOS LEDs should go out.
- At this point any packets sent to the DS33M33 are echoed back. Incoming packets (i.e., ping) should cause the Activity LED to blink.
- Note that ChipView.exe display settings can be changed using the **Options→Settings** menu.

4.3 Monitor and Capture Ethernet Traffic

- Although ping is mentioned, it is **not** the recommended frame source for testing. The ping command goes through the computer's TCPIP stack, and sometimes is not sent out the PC's network connector (i.e., if the PC's ARP cache is out of date). Additionally, ping requires two PCs, as a Windows PC with only one adapter cannot ping itself (i.e., a local ping gets sent to local host instead of out the connector). With that said, ping is still a valuable test once the prototyping stage is complete.
- Generation and capture of arbitrary (raw) packets can be accomplished using CommView. A time-limited demo is available at www.tamos.com/products/commview.
- Wireshark (formerly Ethereal) is a free packet capture utility. Download is available at www.wireshark.org.
- Adding additional Ethernet ports to a PC is rather simple when a USB-to-Ethernet adapter is used. This allows for end-to-end testing using a single PC. When using two adapters, the PC has a different IP address for each adapter. Test equipment allows selection of either adapter. Operating system-based

Downloaded from: http://www.datasheetcatalog.com/

network traffic is sent out the default adapter, which usually is the adapter that has recently had connection to a live network.

5. Jumpers and Connectors

Jumpers and connectors are listed in Table 5-1. They are listed in order of appearance on the PCB from left to right, top to bottom (as viewed with SONET connectors port on the left side of the board).

Table 5-1. Jumpers and Connectors

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J05	Overhead Test Points	J05.5+J05.6 Jumpered	2	Jumpers to connect overhead CPLD to DS33M33. Connector is marked to show that the odd numbered pins belong to the CPLD.
J02	Spare Connector	Not used	23	Spare pins connected to overhead CPLD.
J08	Overhead Test Points	—	2	Jumpers to connect overhead CPLD to DS33M33. Connector is marked to show that the odd numbered pins belong to the CPLD.
JB01 (bottom of PCB)	JTAG	—	24	CPLD JTAG header.
JP05 + JP02	Bias PHY Speed1 + Speed0	Jumper P2+1 (low) P2+1 (low)	26	If auto negotiation is enabled, this setting advertises capability for 10/100/1000 speeds. If auto negotiation is disabled, then this setting forces 10Mb mode.
		Jumper P2+3 (high) P2+3 (high)	26	If auto negotiation is enabled this setting advertises capability for 10/100 speeds. If auto negotiation is disabled, this setting is not legal.
		Jumper P2+3(high) P2+1 (low)	26	If auto negotiation is enabled, this setting advertises capability for 1000 speeds. If auto negotiation is disabled, this setting forces 1000Mb mode.
Note: In Gigabit mode the DS33M33 Mac must be configured with indirect Mac register MACCR bit 15 set.				
JP03	Bias PHY ANEN	Jumper P2+3 (high)	26	Jumper P2+3 to enable auto negotiation.
JP04	Bias PHY Duplex	Jumper P2+3 (high)	26	Jumper P2+3 to enable full duplex; jumper P1.2 to force half duplex.
JP06	Bias PHY ManMDIX	Jumper P2+1 (high)	26	Default MDIX setting P2+3 PHY is set to straight mode; P2+1 PHY is in crossover mode.
JP07	Bias PHY NonIEEE	Jumper P2+3 (high)	26	Jumper P2+3 to enable IEEE compliant operation.
JP08	Bias PHY MultiEn	Jumper P2+1 (high)	26	PHY advertisement setting. P2+3 selects multiple node priority (switch or hub); P1+2 selects single node priority (NIC).
JP09	Bias PHY MdixEn	Jumper P2+1 (high)	26	P2+3 disables pair swap mode, P2+1 enables pair swap mode

Downloaded from: http://www.datasheetcatalog.com/

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
JP10	Bias PHY MacClkEn	Jumper P2+3 (low)	26	P2+3 PHY clock to mac output is disabled, P1+2 PHY clock to mac output is enabled. Mac clock only needs to be enabled in Gigabit mode.
DS14	LED activity	—	26	Flashes for PHY Tx-Rx activity.
DS15 DS16 DS17	LED link speed	1 of the 3 should be lit (when linked)	26	LED to indicate link speed–1000, 100, or 10Mbps. Only one of the three LEDs should be lit. See JP05 + JP02 description for setting in GMII vs. MII mode.
DS18	LED duplex	—	25	LED is on in full-duplex mode.
JB03 JB02	PHY Test Points	—	19	PHY test points. The connector pinout is compatible with existing PHY cards, but cannot be used with U04 on the board.
J16	JTAG	Jumper J16.1+J16.3	8	DS33M33 JTAG.
J20	Runtime options	NA	1	Currently the device drivers do not fit in flash, and are not loaded to the DK.
J31	JTAG	—	31	FPGA JTAG.
JP25 JP26	Comm Port	Jumper P1+2 P1+2	15	Jumper pins 1+2 to select the RS232 transceiver. Jumper pins 2+3 to select the USB to serial converter.
SW01	Reset	—	11	System reset button.
J21	Test Points	—	8	Databus test points, pins D0–D15
J24	Test Points	—	8	Address bus test points pins A0–A13.
J23	Test Points	—	8	Test points for DS33M33 CS, WR RD, and INT.
JP22 JP21 JP20	SPI Bias SWAP CPHA CPOL	Jumper P1+2	8	Jumper pins 2+1 to connect to processor parallel databus. Leave jumper off to pull pin low, jumper pins 2+3 to pull pin high.
JP14 JP13 JP12 JP11	SPI connection CS MISO MOSI SCK	Jumper P1+2	8	Jumper Pins 2+1 to connect to parallel databus. Jumper pins 2+3 to connect to SPI port.
J30	Pin Bias IFSEL_SIZE IFSEL_STYLE SPISEL HIZ DCESEL RMIISEL ALE	Jumper IFSEL_STYLE HIZ_N (parallel mode)	8	Jumper to pull high, leave jumper off to pull low.
J19	Clock select	Jumper P2+4	6	Clock selection for PHY and Ethernet side of DS33M33.
JP01	Clock select	Jumper P1+2	6	Clad clock selection, jumper P1+2 to drive with 19.44MHz. Jumper P2+3 to drive with 77.76MHz clock.

Downloaded from: http://www.datasheetcatalog.com/

SILKSCREEN REFERENCE	FUNCTION	BASIC SETTING	SCHEMATIC PAGE	DESCRIPTION
J09 J10	SerDes analog test points	—	3, 4	Test points to view analog +- differential SerDes signals. To loopback DS33M33 Tx→Rx remove the SFP and jumper P3+5 and P2+6.
J03 J04	SFP test points	Jumper P9+10	3	Test points for SFP module.
DS02 DS03	SFP MOD0	—	3	Lit when a SFP module is installed.
DS08 DS09	SFP TXDISABLE	—	3	Lit when Tx is enabled.
DS05 DS04	SFP LOS	—	3	Lit when fiber optic cable is removed.
J06 J07	SFP LOS / M33 LOS	Jumper P2+3	3, 4	Jumper P2+3 to connect SFP LOS to DS33M33 LOS. Jumper P2+4 to pull DS33M33 high. Jumper P2+6 to pull DS33M33 low.
U03	SFP	Installed	3, 4	Primary SFP module.
U02	SFP	Not Installed	3, 4	Redundant SFP module.
J33	Software Debug	—	15	ONcE EBDI.
J32	JTAG	—	20	LIU JTAG.
J13 J15 J18	RCLK RNEG RPOS	Jumpered	9	LIU-to-DS33M33 connections.
J13 J15 J18	TCLK TNEG TPOS	Jumpered	9	LIU-to-DS33M33 connections.
JP16 JP23 JP24	LIU Port Clocks	Not used	9	Jumper 1+2 to drive TCLKn with OscSel. Jumper 2+3 to drive TCLKn with RCLKn.
J22 J25 J26 J27 JB05 JB06 J28 J29	RX3 TX3 RX1 TX1 RX4 (bottom of PCB) TX4 (bottom of PCB) RX2 TX2	—	8	Rx Tx jumpers.
JP17	LIU_T3MCLK	Jumper P2+3	20	Jumper P2+3 to drive with T3 Osc. Jumper P1+2 to drive with T3_MCLK_IO.
JP18	LIU_ALT_MCLK	Jumper P2+3	20	Jumper P2+3 to drive with Osc Sel. Jumper P1+2 to drive with Alternate MCLK.
JP19	LIU_E3MCLK	Jumper P2+3	20	Jumper P2+3 to drive with E3 Osc. Jumper P1+2 to drive with E3_MCLK_IO.
JP15	Osc Select	Jumper P2+3	20	Jumper P2+3 to drive with T3 Osc. Jumper P1+2 to drive with E3 Osc.

Downloaded from: http://www.datasheetcatalog.com/

6. Line-Side Connections

The DS33M33DK has two optical ports: one Ethernet port and three T3E3 ports.

7. System Connectors

System-side signals can be accessed from test point headers. The headers are clearly labeled with signal information.

8. Microcontroller

The microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS33M33 and the FPGAs.

9. Power-Supply Connectors

Connect a 5.0V wall adapter to the PCB power jack. LED DS1 provides indications that a 5.0V supply is connected properly. The board power supplies (3.3V, 2.5V, and 1.8V) are regulated to supply proper voltages to various circuits on the board.

10. Connecting to a Computer

Both USB and serial modes are supported.

To connect through a RS-232 serial port, set jumpers JP25 and JP26 jumpers to pins 1+2, identified in the silkscreen as UART,PROC. Connect a standard DB-9 serial cable between the serial port on the DS33M33DK and an available serial port on the host computer. The host computer must be a Windows-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

To connect through USB, set jumpers JP25 and JP26 jumpers to pins 3+2, identified in the silkscreen as USB,PROC. Connect a USB cable between the DS33M33DK USB connector and the PC. The host computer must be a Windows-based PC, which should automatically recognize the device as a virtual com port and assign the device drivers. If drivers are not automatically assigned, direct the **New Hardware** wizard to the driver files on the CD in the folder marked **USBdrivers_CP210x**.

Downloaded from: http://www.datasheetcatalog.com/

11. Installing and Running the Software

ChipView is a general-purpose program that supports a number of Maxim demo kits. To install the ChipView software, run Chipview.msi from the disk included in the DS33M33DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS33M33DK.

After installation, run the ChipView program with the DS33M33DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Maxim evaluation platforms. In the active subwindow, select the _DS33M_GlobalSonet.def definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS33M33's register map. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

Downloaded from: http://www.datasheetcatalog.com/

12. Address Map

Address space begins at 0x81000000. All offsets given in the following tables are relative to 0x81000000. Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named **Overhead_FPGA.def**.

Table 12-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X6000	FPGA	Overhead CPLD and Clock/Signal Routing
0X4000	DS3154	DS3154 Line Interface Unit
0X0000	DS33M33	DS33M33 Registers

12.1 Overhead CPLD Register Map

Table 12-2. Register Map for Overhead CPLD (Reference Designator U01)

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0001	ATOH_CFG	Control	ATOH Configuration
0X0002	ATOHEN_CFG	Control	ATOHEN Configuration
0X0003	GPIOAwr	Control	GPIO A Output Enable + Write Value
0X0004	GPIOBwr	Control	GPIO B Output Enable + Write Value
0X0005	DTOH_STAT	Read-Only	DTOH Status
0X0006	DTOH_SEL	Control	DTOH Configuration
0X0007	GPIOrd_STAT	Read-Only	GPIO Read Values
0X0008	RDOH_STAT	Read-Oonly	RDOH Status
0x000A	RDOH_SEL	Control	RDOH Select
0x000D	TAOH_CFG	Control	TAOH Configuration
0x000F	TAOHen_CFG	Control	TAOHen Configuration

Downloaded from: http://www.datasheetcatalog.com/

12.2 Control and Status Registers

Register Name: **ATOH_CFG**
Register Description: **ATOH Configuration**
Register Offset: **0x0001**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	0	0	0	0	0	0	0	0

This register sets the overhead transport data byte value, which is positioned by the following register, ATOHEN_CFG.

Register Name: **ATOHEN_CFG**
Register Description: **ATOHEN Configuration**
Register Offset: **0x0002**

Bit #	7	6	5	4	3	2	1	0
Name								
Default	0	0	0	0	0	0	0	0

Byte enable for overhead transport byte, the data value in **ATOH_CFG** is positioned in the overhead as specified by **ATOHEN_CFG**. Examples follow:

ATOHEN_CFG	ATOH_CFG	RESULT
0	NA	Data is not written onto the overhead when **ATOHEN_CFG** = 0.
0x01	0x54	Data value 0x54 is written onto the first byte of the transport overhead.
0x81	0x54	Data value 0x54 is written onto the last byte of the transport overhead.
0x##	0xNN	Data value 0xNN is written to the 0x## byte of the transport overhead.

Downloaded from: http://www.datasheetcatalog.com/

Register Name: **GPIOAwr**
Register Description: **GPIO A Output Enable + Write Value**
Register Offset: **0x0003**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	GPIOa3 Output En	GPIOa3 Value	GPIOa2 Output En	GPIOa2 Value	GPIOa1 Output En	GPIOa1 Value
Default	0	0	0	0	0	0	0	0

Bits 5 and 4: DS33M33 GPIOA_3 Three-State and Level
0x = FPGA three-states GPIOA_3 pin
00 = FPGA drives GPIOA_3 pin with 0.0V
01 = FPGA drives GPIOA_3 pin with 3.3V

Bits 3 and 2: DS33M33 GPIOA_2 Three-State and Level
0x = FPGA three-states GPIOA_2 pin
00 = FPGA drives GPIOA_2 pin with 0.0V
01 = FPGA drives GPIOA_2 pin with 3.3V

Bits 1 and 0: DS33M33 GPIOA_1 Three-State and Level
0x = FPGA three-states GPIOA_1 pin
00 = FPGA drives GPIOA_1 pin with 0.0V
01 = FPGA drives GPIOA_1 pin with 3.3V

Register Name: **GPIOBwr**
Register Description: **GPIO B Output Enable + Write Value**
Register Offset: **0x0004**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	GPIOb3 Output En	GPIOb3 Value	GPIOb2 Output En	GPIOb2 Value	GPIOb1 Output En	GPIOb1 Value
Default	0	0	0	0	0	0	0	0

Bits 5 and 4: DS33M33 GPIOB_3 Three-State and Level control
0x = FPGA three-states GPIOB_3 pin
00 = FPGA drives GPIOB_3 pin with 0.0V
01 = FPGA drives GPIOB_3 pin with 3.3V

Bits 3 and 2: DS33M33 GPIOB_2 Three-State and Level control
0x = FPGA three-states GPIOB_2 pin
00 = FPGA drives GPIOB_2 pin with 0.0V
01 = FPGA drives GPIOB_2 pin with 3.3V

Bits 1 and 0: DS33M33 GPIOB_1 Three-State and Level control
0x = FPGA three-states GPIOB_1 pin
00 = FPGA drives GPIOB_1 pin with 0.0V
01 = FPGA drives GPIOB_1 pin with 3.3V

Downloaded from: http://www.datasheetcatalog.com/

Register Name: **DTOH_STAT**
Register Description: **DTOH Status**
Register Offset: **0x0005**

Bit #	7	6	5	4	3	2	1	0
Name	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0
Default	0	0	0	0	0	0	0	0

Read value of 1 of 81 bytes selected by DTOH_SEL.

Register Name: **DTOH_SEL**
Register Description: **DTOH Configuration**
Register Offset: **0x0006**

Bit #	7	6	5	4	3	2	1	0
Name	SEL7	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	SEL0
Default	0	0	0	0	0	0	0	0

Byte select for overhead transport byte, the overhead byte specified by **DTOH_CFG** is written to **DTOH_STAT**.

Examples:

DTOH_SEL	DTOH_STAT	RESULT
0	First byte	The first byte of the transport overhead is written to DTOH_STAT.
0x80	Last byte	The last byte of the transport overhead is written to DTOH_STAT.

Register Name: **GPIOrd_STAT**
Register Description: **GPIO Read Values**
Register Offset: **0x0007**

Bit #	7	6	5	4	3	2	1	0
Name	—	GPIOA3	GPIOA2	GPIOA1	—	GPIOB3	GPIOB2	GPIOB1
Default	0	0	0	0	0	0	0	0

Bit 6: DS33M33 GPIOA3 Pin Value
Reflects the value of DS33M33 GPIOA3 pin.

Bit 5: DS33M33 GPIOA3 Pin Value
Reflects the value of DS33M33 GPIOA2 pin.

Bit 4: DS33M33 GPIOA3 Pin Value
Reflects the value of DS33M33 GPIOA1 pin.

Bit 2: DS33M33 GPIOA3 Pin Value
Reflects the value of DS33M33 GPIOB3 pin.

Bit 1: DS33M33 GPIOA3 Pin Value
Reflects the value of DS33M33 GPIOB2 pin.

Bit 0: DS33M33 GPIOA3 Pin Value
Reflects the value of DS33M33 GPIOB1 pin.

Downloaded from: http://www.datasheetcatalog.com/

Register Name: **RDOH_STAT**
Register Description: **RDOH Status**
Register Offset: **0x0008**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Read value from the member and byte selected by RDOH_SEL[7:4] and RDOH_SEL[3:0]

Register Name: **RDOH_SEL**
Register Description: **RDOH Select**
Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	IF3	IF2	IF1	IF0	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Overhead interface Member Select. Writing IF[3:0] to a value of 0 disables. Writing 1 to 10 selects among the 10 members used in RDOH_STAT.

Bits 3 to 0: Byte Select. Writing B[3:0] to a value of 0-to-N selects the Nth byte in the member selected.

Register Name: **TAOH_CFG**
Register Description: **TAOH Configuration**
Register Offset: **0x000D**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Value to be written to the member and byte selected by TAOHen_CFG[7:4] and TAOHen_CFG [3:0]

Register Name: **TAOHen_CFG**
Register Description: **TAOH Enable Configuration**
Register Offset: **0x000F**

Bit #	7	6	5	4	3	2	1	0
Name	IF3	IF2	IF1	IF0	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Overhead interface Member Select. Writing IF[3:0] to a value of 0 disables. Writing 1 to 10 selects among the 10 members used in TAOH_STAT.

Bits 3 to 0: Byte Select. Writing B[3:0] to a value of 0-to-N selects the Nth byte in the member selected.

Downloaded from: http://www.datasheetcatalog.com/

13. Additional Information/Resources

13.1 DS33M33 Information

For more information about the DS33M33, refer to the DS33M33 data sheet at www.maxim-ic.com/DS33M33.

13.2 DS33M33DK Information

For more information about the DS33M33DK, refer to the DS33M33DK Quick View page at www.maxim-ic.com/DS33M33DK.

13.3 Technical Support

For additional technical support, submit your questions at www.maxim-ic.com/support.

Downloaded from: http://www.datasheetcatalog.com/

14. Component List

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C08, CB34, CB36, CB37, CB38, CB39, CB40, CB41, CB42, CB58, CB64, CB66, CB67, CB68, CB72, CB79, CB92, CB101, CB104, CB112, CB170	21	L_0603 CERAM .01uF 50V 10% X7R	AVX	06035C103KAT
See next row (begins with C02)	61	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
C02, C04, C05, C07, C10, C15, C18, CB05, CB06, CB09, CB10, CB11, CB12, CB16, CB21, CB22, CB23, CB25, CB28, CB33, CB43, CB44, CB45, CB47, CB53, CB54, CB63, CB65, CB69, CB77, CB83, CB85, CB88, CB89, CB94, CB95, CB97, CB98, CB113, CB115, CB116, CB118, CB122, CB126, CB128, CB134, CB135, CB137, CB138, CB140, CB142, CB143, CB144, CB146, CB148, CB156, CB160, CB168, CB177, CB186, CB187				
DB01	1	SCHOTTKY DIODE, 1 AMP 40 VOLT	International Rectifier	10BQ040
DS01, DS06, DS07, DS10, DS11, DS12, DS13, DS31	8	LED, RED/GREEN, SMD	LITEON	160-1172-1-ND
GND_TP01, GND_TP02, GND_TP03, GND_TP04, GND_TP11, GND_TPB01, GND_TPB02, GND_TPB03, GND_TPB06	9	STANDARD GROUND CLIP	KEYSTONE	4954
DS14, DS15, DS16, DS17	4	LED, GREEN/GREEN, SMD	LUMEX	67-1362-1-ND
J34	1	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
UB02, UB04, UB06	3	SPI SERIAL EEPROM 2M 8 PIN SOIC 2.7V to 3.6V	Atmel	AT25F2048N-10SU-2.7
RPB24, RPB26	2	RESISTOR, 4 PACK, 50 OHM 2PCT QUAD 0603	KOA	CN1J4TTD500G
U10	1	IC, SINGLE-CHIP USB TO UART BRIDGE, 28 PIN QFN	SIL	CP2101
J32	1	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT DO NOT POPULATE	DNP	DNP
U04	1	GIG PHYTER V, 10/100/1000 ETHERNET PHYSICAL LAYER, 128 PIN QFP	National Semiconductor	DP83865DVH
U07	1	QUAD DS3/E3/STS1 LIU 144P BGA	Maxim	DS3154
U05	1	IC, ETHERNET OVER SDH/SONET (EoS), -40C TO 85C, 256-PIN CSBGA	Maxim	DS33M33N
XB01	1	XTAL LOW PROFILE 8.0MHZ	ECL	EC1-8.000M
See next row (begins with C01)	79	0603 CERAM 4.7uF 6.3V MULTILAYER	Digi-Key	ECJ-1VB0J475M
C01, C03, C06, C09, C11, C12, C13, C14, C16, C23, CB03, CB04, CB07, CB14, CB15, CB17, CB18, CB19, CB20, CB24, CB26, CB27, CB29, CB30, CB31, CB32, CB46, CB49, CB55, CB60, CB62, CB70, CB73, CB74, CB75, CB76, CB78, CB82, CB84, CB86, CB90, CB91, CB93, CB96, CB100, CB102, CB103, CB106, CB107, CB109, CB110, CB114, CB117, CB119, CB120, CB121, CB123, CB127, CB129, CB131, CB132, CB133, CB136, CB139, CB141, CB147, CB150, CB153, CB154, CB162, CB163, CB165, CB167, CB173, CB175, CB181, CB182, CB183, CB190				
See next row (begins with CB50)	20	0603 CERAM .1uF 16V 10%	Panasonic	ECJ-1VB1C104K

Downloaded from: http://www.datasheetcatalog.com/

CB50, CB56, CB57, CB61, CB71, CB80, CB81, CB87, CB99, CB105, CB108, CB149, CB151, CB152, CB155, CB161, CB166, CB172, CB179, CB180				
See next row (begins with C17)	21	1206 CERAM 10uF 10V 20%	Panasonic	ECJ-3YB1A106M
C17, C19, C20, C21, C22, C24, CB188 , CB01, CB02, CB08, CB13, CB35, CB48, CB51, CB52, CB59, CB111, CB124, CB125, CB130, CB169				
CB164, CB184	2	L_1206 CERAM 1uF 16V 10%	Panasonic	ECJ-3YB1C105K
CB178	1	1206 CERAM 4.7uF 25V 10% X5R	Panasonic	ECJ-3YB1E475K
CB158, CB159, CB185, CB189	4	L_D CASE TANT 68uF 16V 20%	Panasonic	ECS-T1CD686R
RB09, RB10	2	RES 0603 100 Ohm 1/16W 1%	Panasonic	ERJ-3EKF1000V
RB12, RB13	2	RES 0603 1.00K Ohm 1/16W 1%	Panasonic	ERJ-3EKF1001V
RB17, RB19, RB20, RB21, RB22, RB23, RB24, RB25	8	RES 0603 332 Ohm 1/16W 1%	Panasonic	ERJ-3EKF3320V
RB16	1	RES 0603 9.76K Ohm 1/16W 1%	Panasonic	ERJ-3EKF9761V
R02, R04, R05, RB04, RB27	5	RES 0603 0.0 Ohm 1/16W 5%	Panasonic	ERJ-3GEY0R00V
RB01, RB02, RB29 , RB05	4	L_RES 0603 10K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ103V
R03	1	RES 0603 1.0M Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ105V
R01, RB06, RB11	3	RES 0603 2.0K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ202V
RB08	1	RES 0603 2.2K Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ222V
RB14, RB15	2	RES 0603 30 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ300V
RB07, RB26 , RB28, RB30	4	RES 0603 330 Ohm 1/16W 5%	Panasonic	ERJ-3GEYJ331V
RB03, RB18	2	RES 0805 10K Ohm 1/10W 1%	Panasonic	ERJ-6ENF1002V
SW01	1	SWITCH MOM 4PIN SINGLE POLE	Panasonic	EVQPAE04M
RPB18	1	RESISTOR, 4 PACK, 100 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V101JX
RPB01, RPB02, RPB05, RPB14, RPB20, RPB30, RPB36, RPB48, RPB52	9	RESISTOR, 4 PACK, 1K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V102JX
RPB03, RPB08, RPB10, RPB11, RPB12, RPB13, RPB29, RPB32, RPB33, RPB40, RPB41, RPB43, RPB45, RPB47, RPB49, RPB50, RPB51, RPB54, RPB55, RPB56, RPB57, RPB58, RPB60, RPB61, RPB62, RPB63, RPB64	27	RESISTOR, 4 PACK, 10K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V103JX
RPB19, RPB21, RPB28	3	RESISTOR, 4 PACK, 2.2K OHM 5PCT QUAD 0603	Panasonic	EXB-V8V222JX
RP02, RP03, RP04, RP05, RP06, RP07, RP08, RP09, RP10, RP11, RP12, RP13, RPB15, RPB16, RPB17, RPB23, RPB25, RPB27, RPB31, RPB34, RPB35, RPB37, RPB44	23	RESISTOR, 4 PACK, 30 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V300JX
RP01, RPB04, RPB06, RPB07, RPB09, RPB22, RPB38, RPB39, RPB42, RPB46, RPB53, RPB59	12	RESISTOR, 4 PACK, 330 OHM 5PCT QUAD 0603	Panasonic	EXB-V8V331JX
L01, L02, LB01, LB02, LB03, LB04	6	1uH ±10% 0805 Multilayer Ceramic 400 mA	TDK	GLF2012T1R0M

Downloaded from: http://www.datasheetcatalog.com/

J01, J30	2	HEADER, 14 PIN, DUAL ROW, VERT	Samtec	HDR-TSW-107-14-T-D
J11	1	CONNECTOR, SINGLE LEVEL, GIGABIT RJ-45, 10 PIN	Halo Electronics	HFJ11-1G02E
U08	1	IC, FPGA, 1.2V, 20X20 TQFP, 144 PIN	LAT	LFE2-6E-5TN144C
U01	1	IC, FPGA, 1.2V, 20X20 TQFP, 144 PIN	LAT	LFEC3E-3T144C
DS04, DS05, DS28 , DS19, DS20, DS21, DS22, DS23, DS24, DS25, DS26, DS27	12	L_LED, RED, SMD	Panasonic	LN1251C
DS02, DS03, DS08, DS09, DS29 , DS18, DS30, DS32	8	L_LED, GREEN, SMD	Panasonic	LN1351C
UB09	1	IC, LINEAR REG 1.5W, 1.8V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-18
UB08	1	IC, LINEAR REG 1.5W, 2.5V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-25
UB10, UB11, UB13	3	IC, LINEAR REG 1.5W, 3.3V or Adj, 1A, 16TSSOP-EP	Maxim	MAX1793EUE-33
UB01, UB03	2	IC, LDO REGULATOR WITH RESET,1.20V OUTPUT 300 MA, 6 PIN SOT23	Maxim	MAX1963EZT120-T
UB07	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	Maxim	MAX811TEUS-T
U09	1	MMC2107 PROCESSOR	Motorola	MMC2107
J03, J04, J23	3	TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Digi-Key	S2012-05-ND
J33	1	100 MIL 2*7 POS JUMPER	NA	NA
J35	1	TYPE B SINGLE RT ANGLE, BLACK	Digi-Key	WM17108-ND
JB08	1	100 MIL 2 POS JUMPER	NA	NA
See next row (begins with JP01)	27	100 MIL 3 POS JUMPER	NA	NA
JP01, JP02, JP03, JP04, JP05, JP06, JP07, JP08, JP09, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP25, JP26, JPB01				
TPB01, TPB02, TPB03	3	TEST POINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U06	1	DOUBLE DATA RATE (DDR) SDRAM 2-2-2 TIMING 256MBITX16 TSSOP	MICRON	MT46V16M16TG-75E
U11, U12	2	CYPRESS SRAM 4Mbit*8	CYPRESS	CY62148DV30L-70SXI
UB14	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	MAXIM	MAX3233E
JB02	1	TEST POINTS FOR SMD 50 PIN, 2 ROW VERTICAL	NA	NA_NOTPOPULATED
UB05 , UB12	2	HIGH SPEED INVERTER	FAIRCHILD	NC7SZ86
J24	1	NON POPULATED HEADER, 14 PIN, DUAL ROW, VERT	Samtec	NOPOP-HDR-TSW-107-14-T-D
JB05, JB06	2	DO NOT POPULATE L_2 PIN HEADER, .100 CENTERS, VERTICAL	Samtec	NOPOP-TSW-102-07-T-S
J09, J10	2	TERMINAL STRIP, 6 PIN, DUAL ROW, VERT NOT POPULATED	Samtec	NOPOP-TSW-103-07-T-D
J21	1	NOPOP TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	NOPOP-TSW-108-07-T-D
YB04	1	OSCILLATOR, CRYSTAL CLOCK, 5.0V - 34.368 MHZ	SaRonix	NTH089AA-34.368
YB05	1	SOCKETED OSCILLATOR, CRYSTAL CLOCK, 3.3V - 25.000 MHZ	SaRonix	NTH089AA3-25.000+SOCKET
YB03	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 44.736 MHZ	SaRonix	NTH089AA3-44.736

Downloaded from: http://www.datasheetcatalog.com/

JB09	1	CONN 2.1MM/5.5MM PWRJACK RT ANGLE PCB, closed frame, high current 24VDC@5A also requires 5V ACDC adapter INPUT 100-240VAC 50-60HZ 0.6A OUTPUT DC 5V 2.6A. PN DMS050260-P5P-SZ. MODEL 3Z-161WP05	CUI, INC	PJ-002AH
JB03	1	PLUG, SMD, 50 PIN, 2 ROW VERTICAL	Samtec	SFM-125-L2-S-D-LC
U02, U03	2	SFP host / receptacle	PARTS_KIT	SFP_HOST-TYCO
HB01, HB02, HB03, HB04, HB05	5	Rubber bumper 0.5 inch	NA	SJ5518-0
YB01	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 19.44 MHZ	SaRonix	SOCKET+NTH089A 3-19.44
YB02	1	OSCILLATOR, CRYSTAL CLOCK, 3.3V - 77.76 MHZ	SaRonix	SOCKET+NTH089A 3-77.7600
T01	1	XFMR, OCTAL T3/E3, 1 TO 2, SMT 32 PIN	Pulse	T3049
CB145, CB157, CB171, CB174, CB176	5	D CASE TANT 470uF 6.3V 20%	KEM	T491D477M006AS
J22, J25, J26, J27, J28, J29	6	L_2 PIN HEADER, .100 CENTERS, VERTICAL	Samtec	TSW-102-07-T-S
J06, J07, J12, J13, J14, J15, J17, J18, J19, J20, JB04, JB07	12	TERMINAL STRIP, 6 PIN, DUAL ROW, VERT	Samtec	TSW-103-07-T-D
J16, J31, JB01	3	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	Samtec	TSW-105-07-T-D
J02, J05, J08	3	TERMINAL STRIP, 16 PIN, DUAL ROW, VERT	Samtec	TSW-108-07-T-D

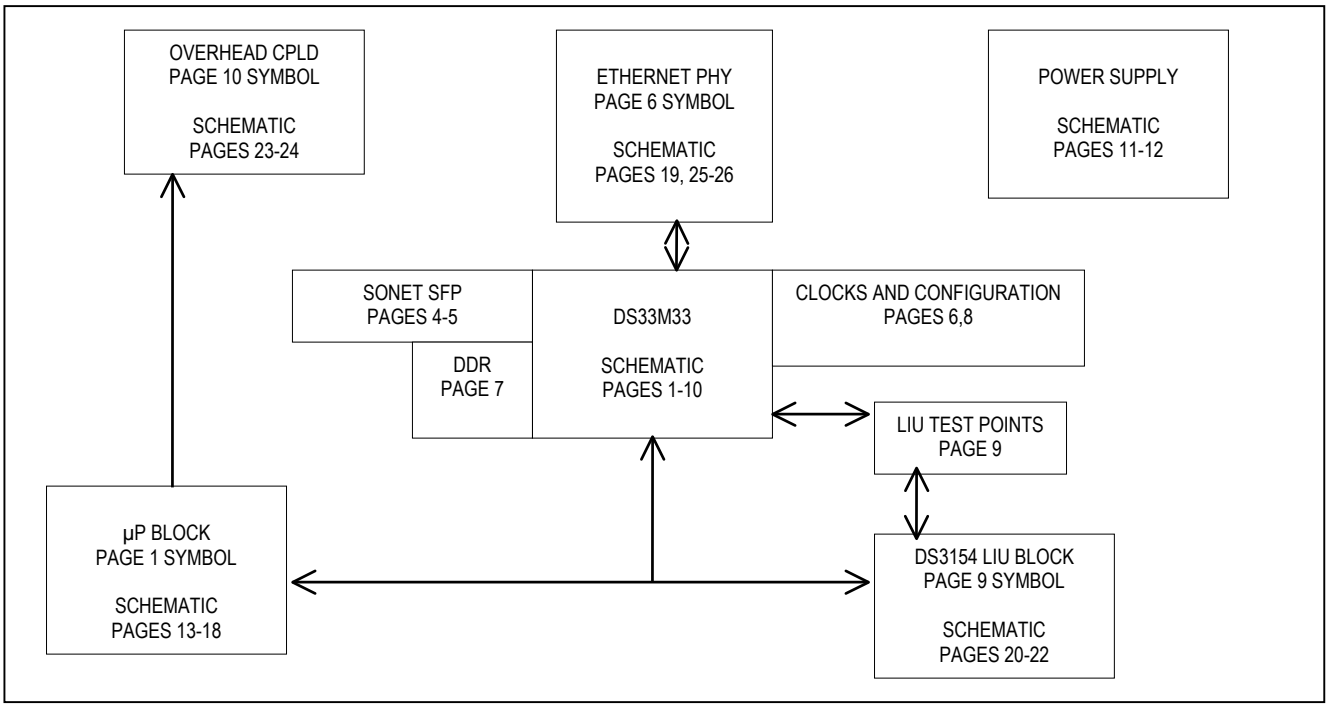
Downloaded from: http://www.datasheetcatalog.com/

15. Schematics

The DS33M33DK schematics are featured in the following pages. The schematic contains five hierarchal blocks: Microcontroller, DS3154, Ethernet PHY, Ethernet Test Points, and Overhead CPLD.

All signals inside a hierarchy block are local, with exception for V_{CC} and ground. In-port and out-port connectors are used to allow signals inside a hierarchy block to become accessible as pins on the hierarchy blocks symbol. From here blocks are wired together as if they were ordinary components. Figure 15-1 shows the system diagram in terms of hierarchal blocks with schematic page numbers given for each functional block.

Figure 15-1. DS33M33 PCB Layout and Schematic Hierarchy Block Page Listing



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

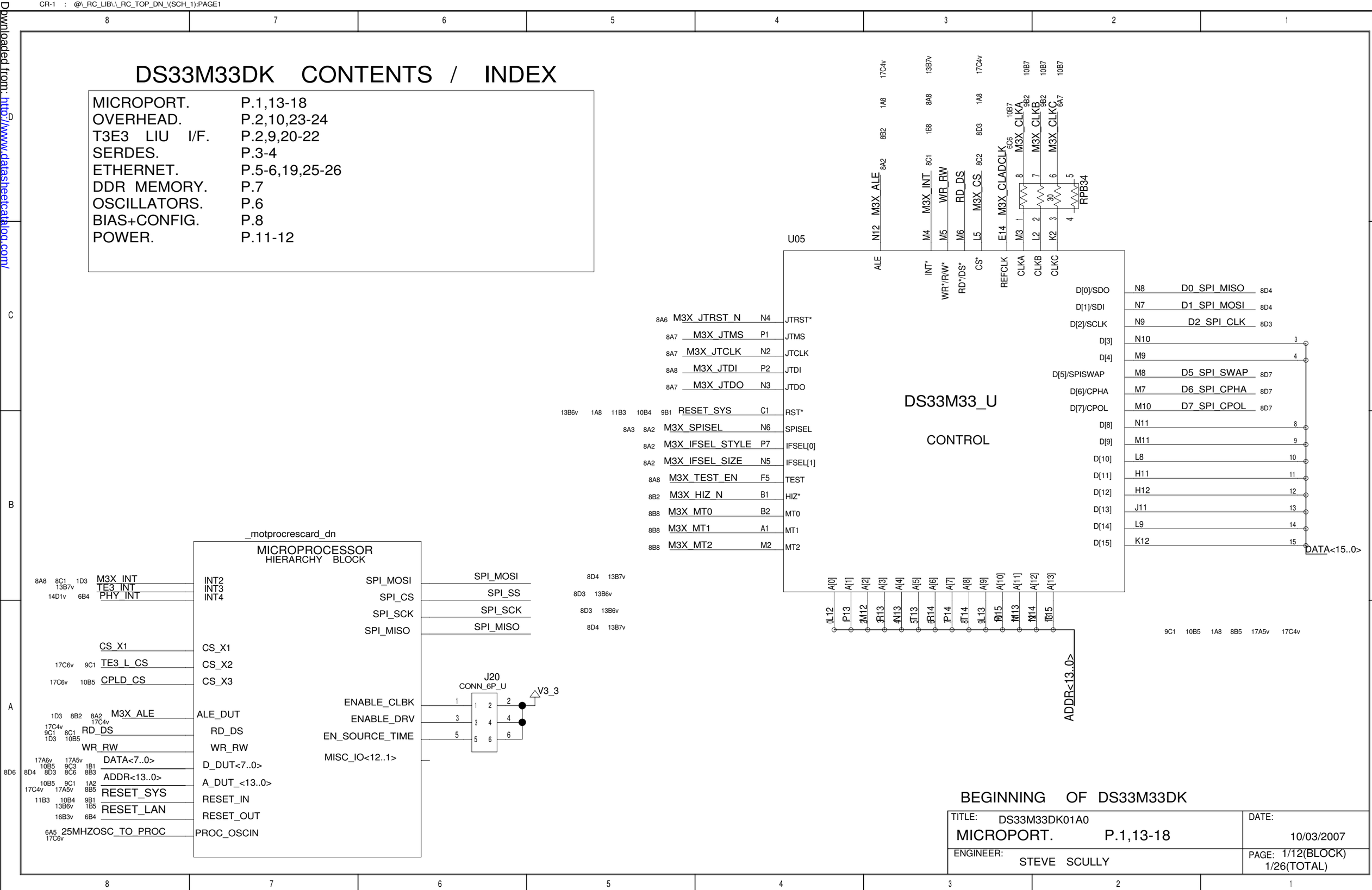
© 2008 Maxim Integrated Products ***MAXIM*** *is a registered trademark of Maxim Integrated Products.*

Downloaded from: http://www.datasheetcatalog.com/

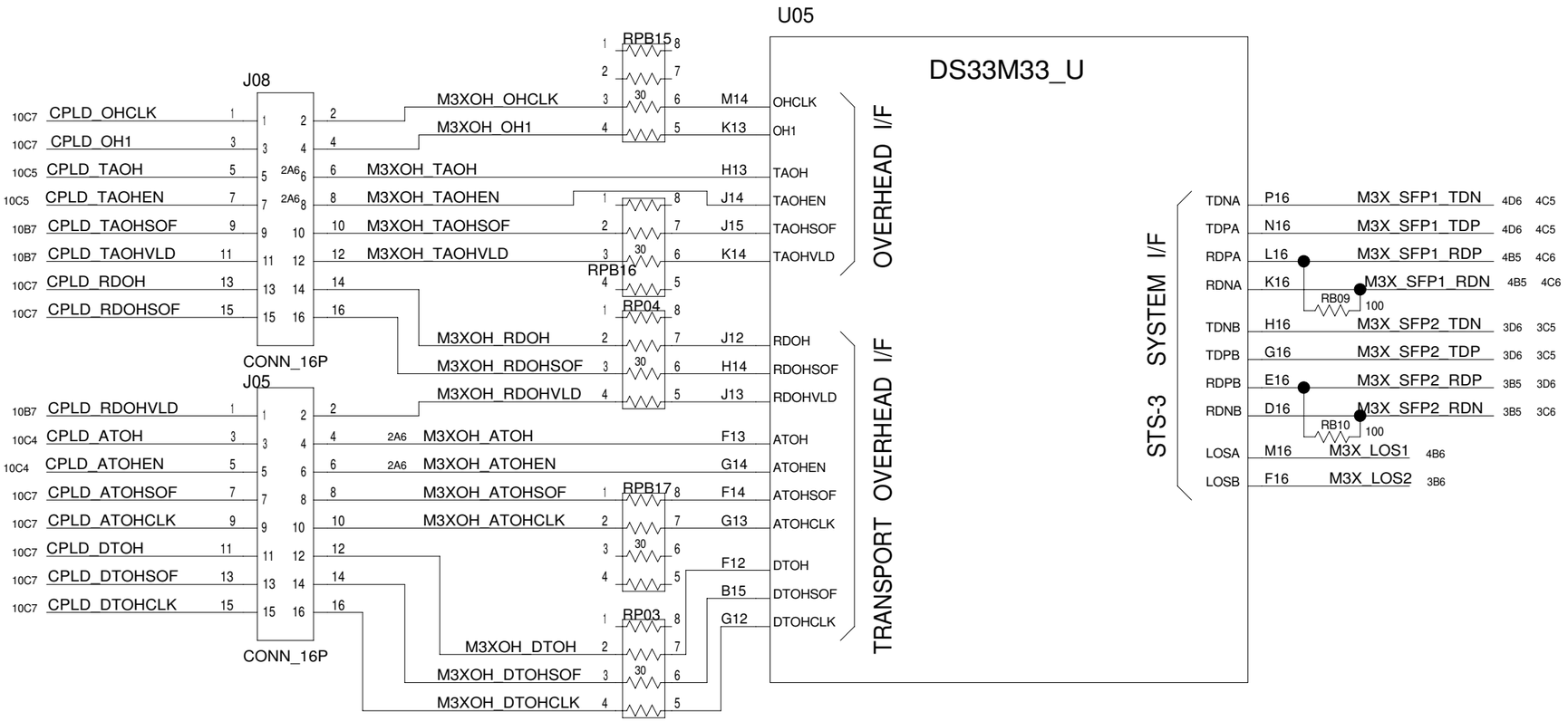
Downloaded from: http://www.datasheetcatalog.com/

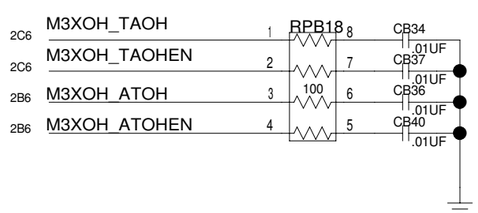
DS33M33DK CONTENTS / INDEX

MICROPORT.	P.1,13-18
OVERHEAD.	P.2,10,23-24
T3E3 LIU I/F.	P.2,9,20-22
SERDES.	P.3-4
ETHERNET.	P.5-6,19,25-26
DDR MEMORY.	P.7
OSCILLATORS.	P.6
BIAS+CONFIG.	P.8
POWER.	P.11-12



Downloaded from: http://www.datasheetcatalog.com/



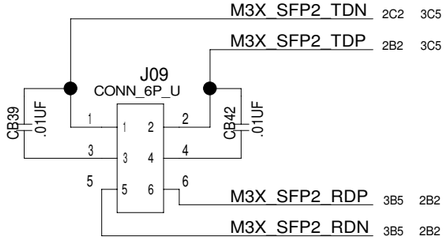


TITLE: DS33M33DK01A0 OVERHEAD. P.2,10,23-24 T3E3 LIU I/F. P.2,9,20-22	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 2/12(BLOCK) 2/26(TOTAL)

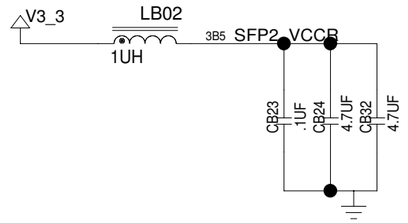
BLOCK NAME: _rc_top_dn_.

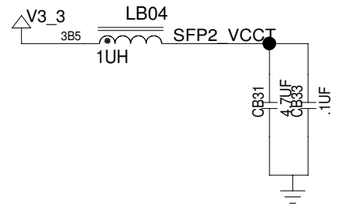
Downloaded from: http://www.datasheetcatalog.com/

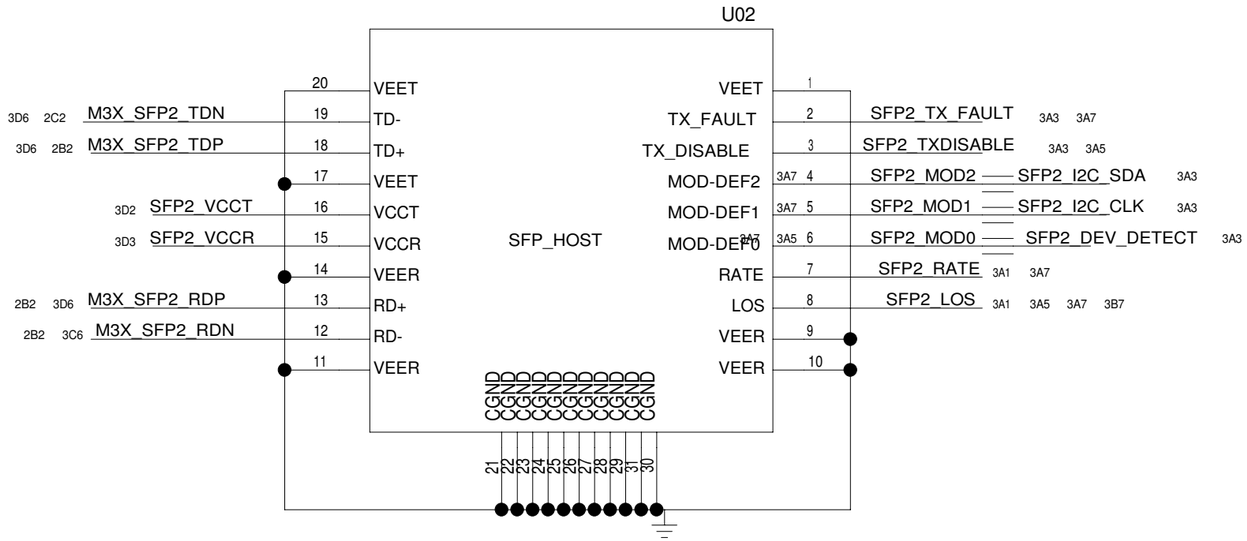
THIS SUBCIRCUIT IS FOR OBSERVATION AND LOOPBACK ONLY
NOT FOR PRODUCTION USE

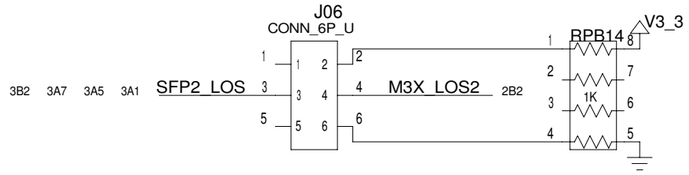


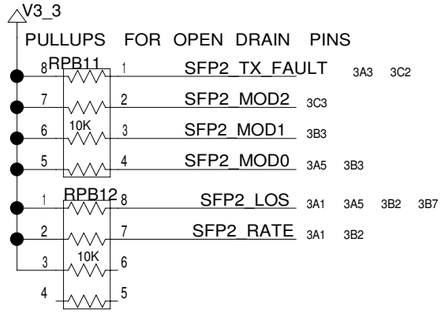
PLACE / ROUTE CAPS AND TESTPOINT
SUCH THAT THEY CAN REMOVED WITHOUT IMPACT

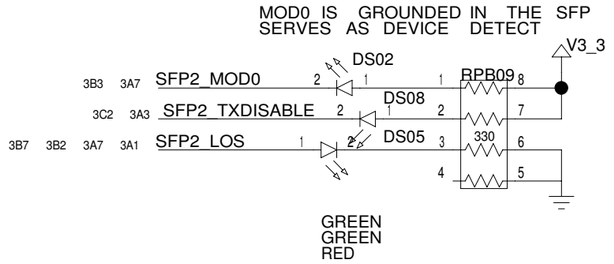


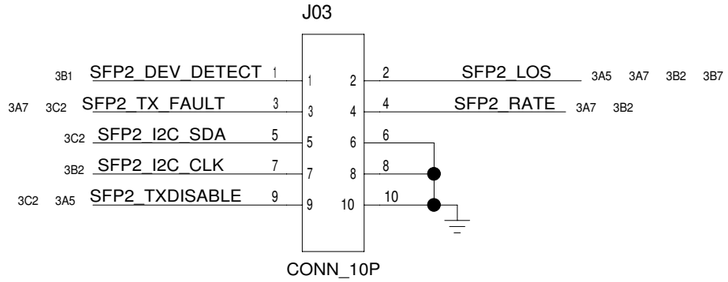










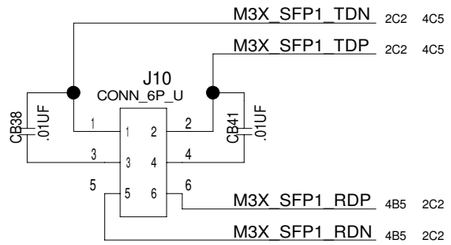


TITLE: DS33M33DK01A0 SERDES. P.3-4	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 3/12(BLOCK) 3/26(TOTAL)

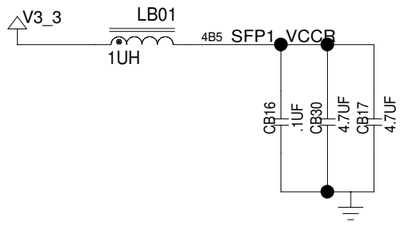
BLOCK NAME: _rc_top_dn_.

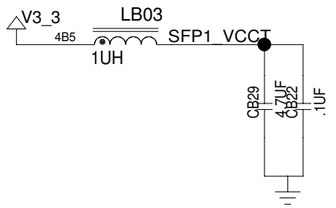
Downloaded from: http://www.datasheetcatalog.com/

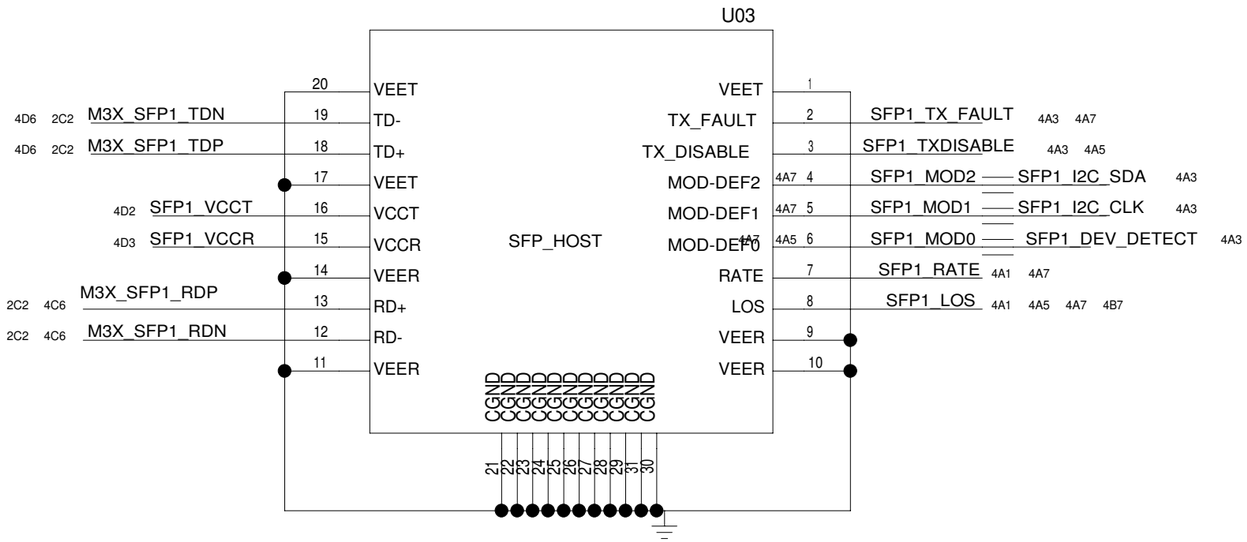
THIS SUBCIRCUIT IS FOR OBSERVATION AND LOOPBACK ONLY
NOT FOR PRODUCTION USE

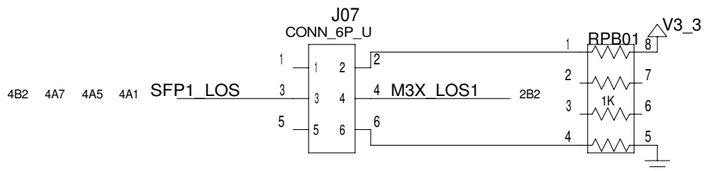


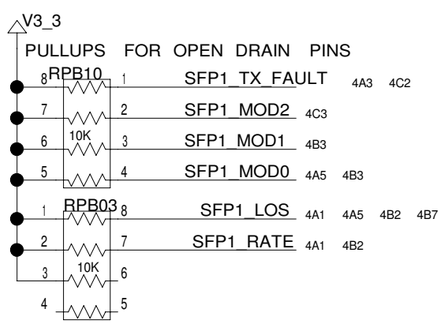
PLACE / ROUTE CAPS AND TESTPOINT
SUCH THAT THEY CAN REMOVED WITHOUT IMPACT

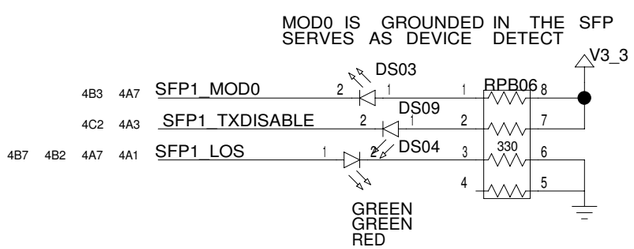


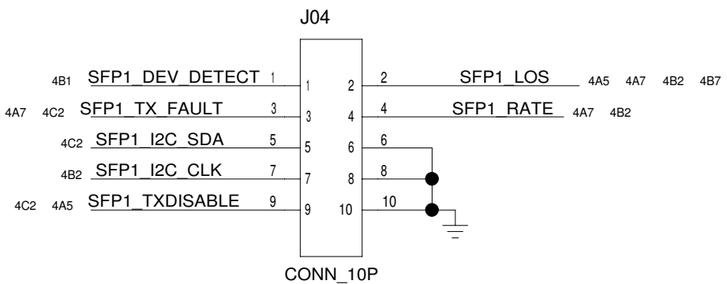












TITLE: DS33M33DK01A0 SERDES. P.3-4	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 4/12(BLOCK) 4/26(TOTAL)

BLOCK NAME: _rc_top_dn_.

Downloaded from: http://www.datasheetcatalog.com/

U05

DS33M33_U

ETHERNET MAC I/F

RPB27

6B1 6C4 GMII_TX_ER — 7 — 2 P3 — TXERR

6C3 ETH_TX_EN — 6 — 3 R2 — TXEN

6C3 ETH_TX_CLK — 5 — 4 T6 — TXCLK

RP08

RP10

6C3 6C4 ETH_TXD<7..0>

TXD[7] 8 R6

TXD[6] 7 P6

TXD[5] 6 R5

TXD[4] 5 P5

TXD[3] 8 T4

TXD[2] 7 R4

TXD[1] 6 P4

TXD[0] 5 R3

RXERR T11 ETH_RX_ERR 6C4

RXDV R11 ETH_RXDV 6D4

RXCLK T8 ETH_RX_CLK 6D3

RXD[7] P10

RXD[6] R10

RXD[5] T10

RXD[4] P9

RXD[3] R9

RXD[2] T9

RXD[1] P8

RXD[0] R8

ETH_RXD<7..0> 6D3 6C3

MDC P12 — ETH_MDC — 6B4

MDIO R12 — ETH_MDIO — 6B4

COL R7 — ETH_COL_DET — 6D4

CRS T7 — ETH_RX_CRS — 6D4

DCESEL P11 — M3X_DCESEL — 8B2

RMISEL T12 — M3X_RMIISEL — 8B2

LANCLKI T3 — M3X_LAN_CLK — 6A5

GTXCLK 8 T5 — GTXCLK — 6C4

LANCLKO 7 T2 — M3X_LAN_CLKO — 6A7

RP11

6A1

TITLE: DS33M33DK01A0 ETHERNET. P.5-6,19,25-26	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 5/12(BLOCK) 5/26(TOTAL)

BLOCK NAME: _rc_top_dn_.

Downloaded from: http://www.datasheetcatalog.com/

V3_3
L01 1UH
I24
YB02
OSC
VCC
GND
OUT
77.76MHZ_3.3V_SOCKET
.1UF 4.7UF
C04 C03 C02 C01
YB01
19.44MHZ_3.3V_SOCKET
JMP_3
JP01
RPB23
I22
30
M3X_CLADCLK 1D3 10B7
M3X_CLADCLK_TO_LIU 9B2

I23
phy_dp83865bvh_dn
HIERARCHY BLOCK
COL_DET
RXD<7..0>
RXDV
RX_CLK
RX_CRS
RX_ERR
TXD<7..0>
TX_CLK
TX_EN
TX_ER_
GMII ONLY
CLKTOMAC
CLKTOMAC_TESTPNT
GMII_CLKFROM_MAC
LAN_CLK
PHYOSC25M
MDC
MDIO
RESET_B
PHY_INT
SPARE<4..1>

ETH_COL_DET 25A1v 19C3v 5A5
ETH_RXD<7..0>
ETH_RXD<3..0> 25B7v 6D3 5B2 19C3v
ETH_RXDV 25A1v 5C3 19C3v
ETH_RX_CLK
ETH_RX_CRS 25A1v 5A5 19C3v
ETH_RX_ERR 25A1v 5C3 19B3v
ETH_TXD<7..0> 19C3v
ETH_TXD<3..0> 5B6 6C4 25B7v
ETH_TX_CLK
ETH_TX_EN
GMII_TX_ER 5C6 6B1 19B3v 25A7v
CLK_TO_MAC 6A7 6B1 19B3v 25B1v
GTXCLK 5A4 6A1 19B3v 25B7v
ETH_RXD<7..4>
ETH_TXD<7..4> 25B7v 19B3v 5B6 6C4
AV_LAN_CLK
PY25MHZOSC
ETH_MDC
ETH_MDIO
RESET_LAN
PHY_INT

V3_3
RB08 2.2K

SINGLE 50 PIN
I.M. CARD PLUG-CONNECTORS
USED ON BOTTOM OF MOTHERBOARD
FOR CONNECTION TO ETHERNET CARD

_phy_imbus_mb_dn
HIERARCHY BLOCK
PT1_COL_DET
PT1_RXD<3..0>
PT1_RXDV
PT1_RX_CLK
PT1_RX_CRS
PT1_RX_ERR
PT1_TXD<3..0>
PT1_TX_CLK
PT1_TX_EN
PT2_COL_DET
PT2_RXD<3..0>
PT2_RXDV
PT2_RX_CLK
PT2_RX_CRS
PT2_RX_ERR
PT2_TXD<3..0>
PT2_TX_CLK
PT2_TX_EN

ETHERNET (LAN)
CONNECTORS
LAN_CLK
OSC25M
MDC
MDIO
RESET_B
PHY_INT
SPARE
GMII_CLKFROM_MAC
GMII_TX_ER
GMII_CLKTOMAC_BUF

25B1v 19B3v 6C3 6A7 CLK_TO_MAC
25A7v 19B3v 6C4 5C6 GMII_TX_ER
25B7v 19B3v 5A4 6C4 GTXCLK

ETHERNET CONNECTOR (I.M. BUS)
IS INTENDED FOR USE AS TESTPOINTS
NOT CONNECTION TO A RESOURCE CARD

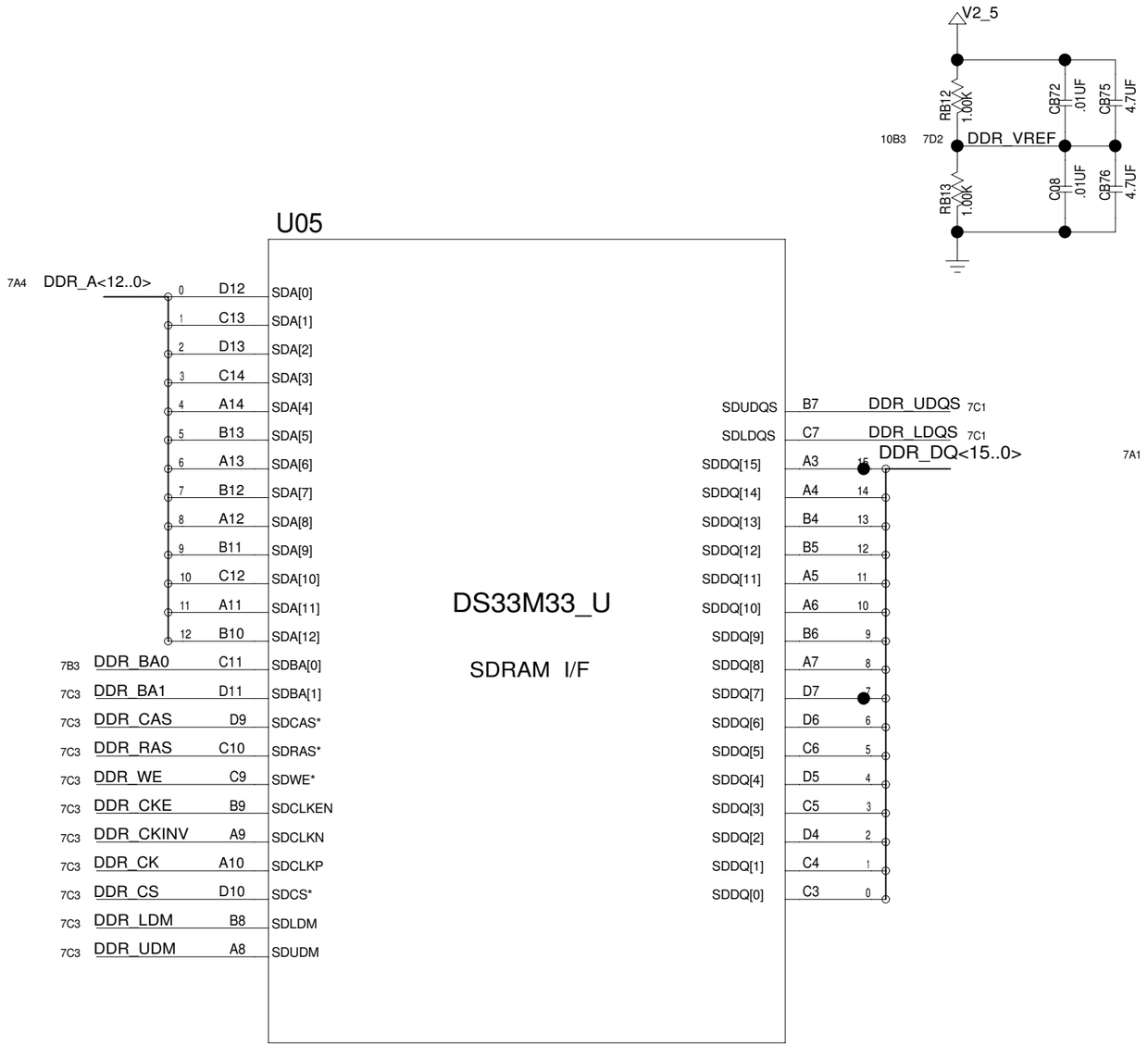
YB05
25.000MHZ_3.3V_SOCKET
OSC
V3_3
REFC_25M
RP13
30
25MHZOSC_TO_PROC 1A8
PY25MHZOSC 6B4 19B3v 25B4v
J19
CONN_6P_U
10B7 1D2 M3X_CLKC
5A4 M3X_LAN_CLKO
CLK_TO_MAC
25B1v 19B3v 6B1 6C3
RB15 30 M3X_LAN_CLK 5A4
RB14 30 AV_LAN_CLK 6B4 19B3v
ETH_REF_CLK IS ONLY
USED IN RMII MODE (50 MHZ)

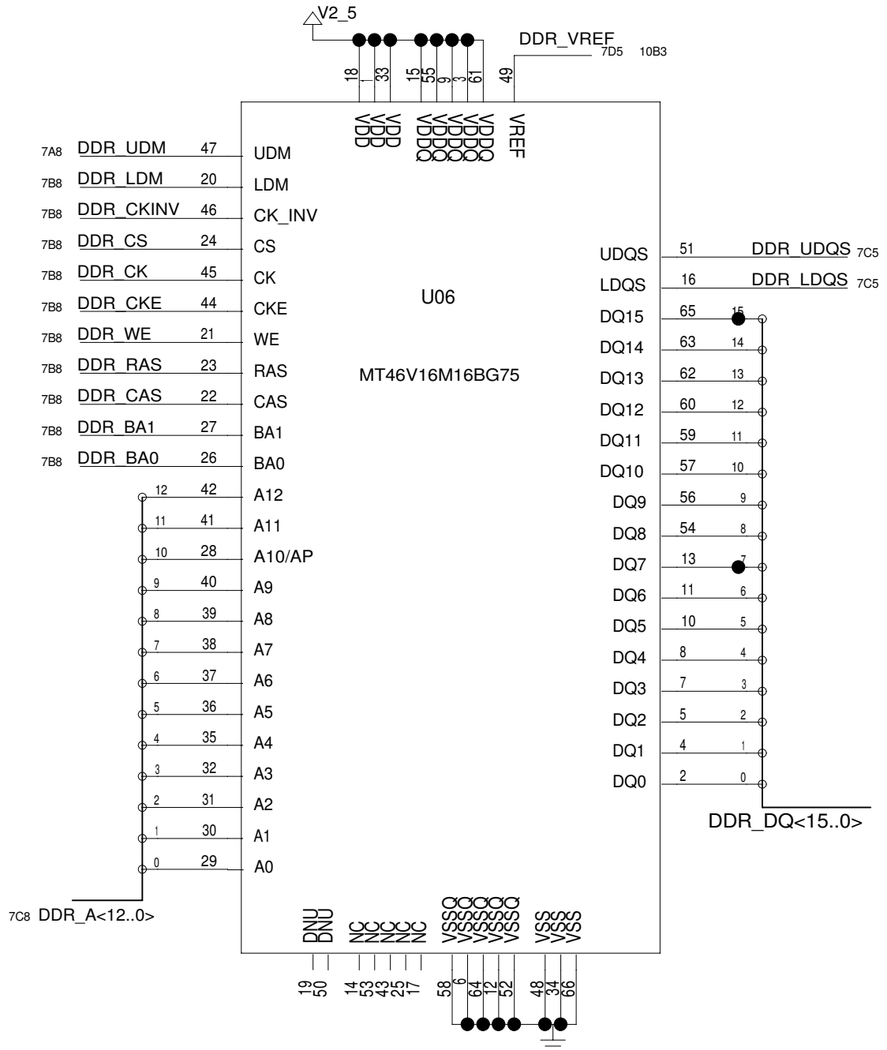
CLOCK TESTPOINTS:
REFCLK & CLKC TESTPOINTS ARE IN THE PHY BLOCK
CLKA AND CLKB TESTPOINTS ARE IN THE LIU BLOCK

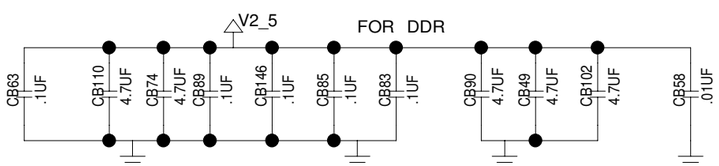
TITLE: DS33M33DK01A0 ETHERNET. P.5-6,19,25-26	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 6/12(BLOCK) 6/26(TOTAL)

BLOCK NAME: _rc_top_dn_.

Downloaded from: http://www.datasheetcatalog.com/



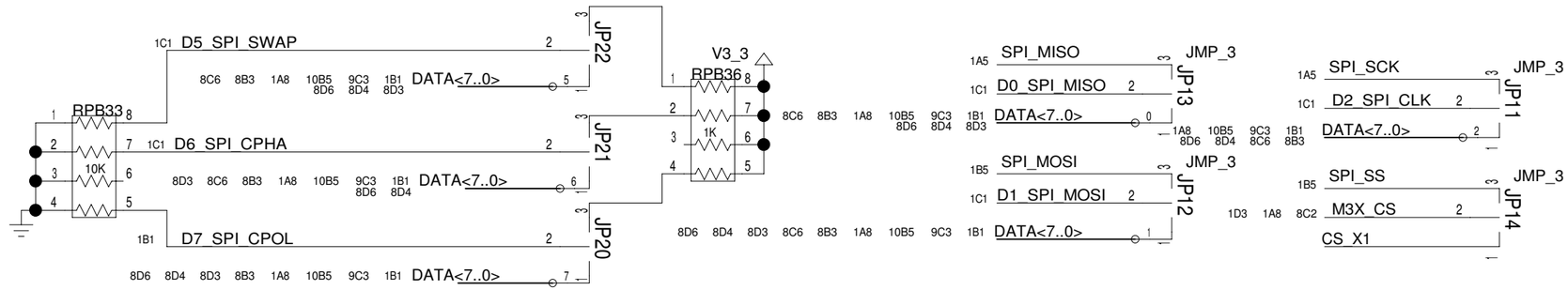


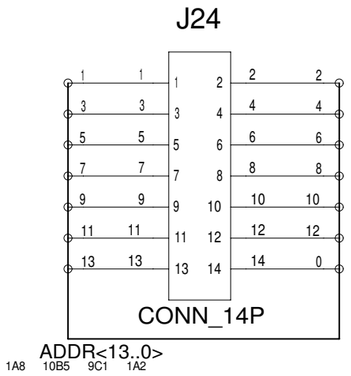


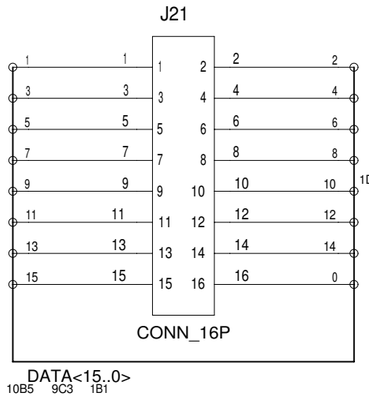
TITLE: DS33M33DK01A0 DDR MEMORY. P.7	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 7/12(BLOCK) 7/26(TOTAL)

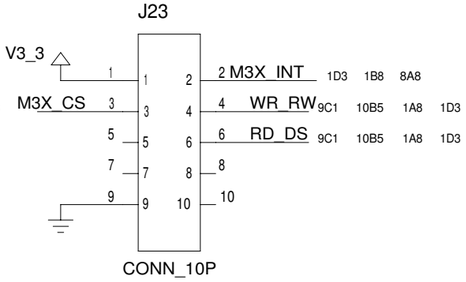
BLOCK NAME: _rc_top_dn_.

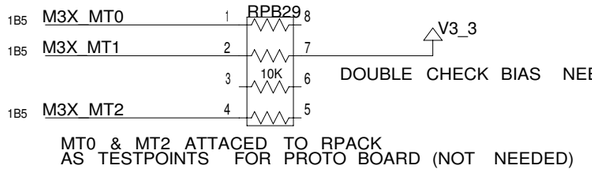
Downloaded from: http://www.datasheetcatalog.com/

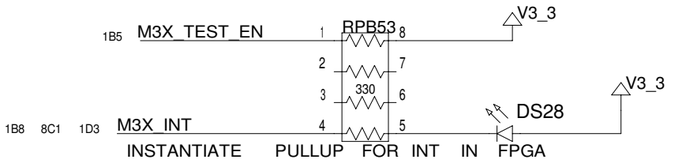


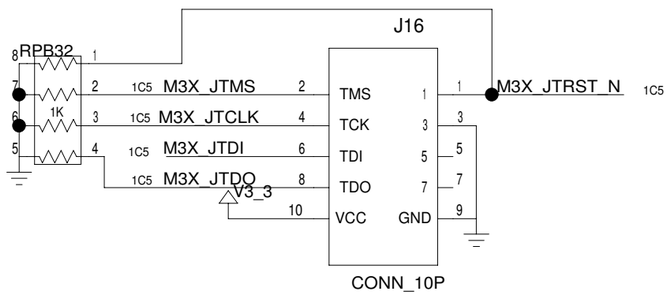


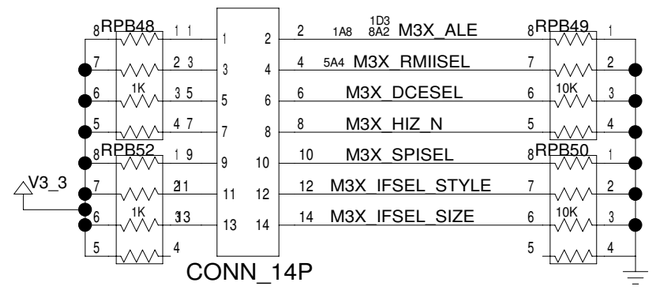




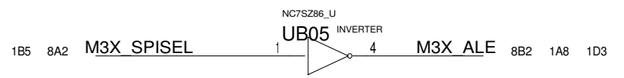








ALE SHOULD BE TIED HIGH FOR NON-MULTIPLEXED ADDRESS OPERATION AND TIED TIED LOW DURING SPI MODE (SPISEL=1). REMOVE THIS INVERTER TO MAKE USE OF THE JUMPER OPTIONS FOR ALE (ABOVE)



TITLE: DS33M33DK01A0 BIAS+CONFIG. P.8	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 8/12(BLOCK) 8/26(TOTAL)

BLOCK NAME: _rc_top_dn_.

Downloaded from: http://www.datasheetcatalog.com/

PORT / PIN ASSIGNMENTS
DS33M33_RCLK1 IS AT PIN F3
DS33M33_RCLK2 IS AT PIN H3
DS33M33_RCLK3 IS AT PIN J2

PLACE TESTPOINTS TO ALLOW LOOPBAK T--R

U05

DS33M33_U

PORT

9D1	M33_RCLK1	F3	RLCLK	TLCLK	E3	M33_TCLK1	9D4	
9D1	M33_RNEG1	G4	RNEG/RLCV	TNEG	F4	M33_TNEG1	9D4	
9D1	M33_RPOS1	E2	RPOS/RDAT	TPOS/TDAT	D2	M33_TPOS1	9D4	
				GPIOA	G2	M33_GPIOA1	9A5	10C4
				GPIOB	F2	M33_GPIOB1	9A5	10C4

U05

DS33M33_U

PORT

9D1	M33_RCLK2	H3	RLCLK	TLCLK	G3	M33_TCLK2	9D4	
9D1	M33_RNEG2	H4	RNEG/RLCV	TNEG	H6	M33_TNEG2	9D4	
9C1	M33_RPOS2	H2	RPOS/RDAT	TPOS/TDAT	G5	M33_TPOS2	9C4	
				GPIOA	H5	M33_GPIOA2	9A5	10C4
				GPIOB	J6	M33_GPIOB2	9A5	10C4

U05

DS33M33_U

PORT

9C1	M33_RCLK3	J2	RLCLK	TLCLK	J4	M33_TCLK3	9C4	
9C1	M33_RNEG3	K4	RNEG/RLCV	TNEG	J5	M33_TNEG3	9C4	
9C1	M33_RPOS3	J3	RPOS/RDAT	TPOS/TDAT	K5	M33_TPOS3	9C4	
				GPIOA	L4	M33_GPIOA3	9A5	10C4
				GPIOB	K3	M33_GPIOB3	9A5	10C4

J13 CONN_6P_U
9D6 M33_TCLK1 — LIU_TCLK1
9D6 M33_TNEG1 — LIU_TNEG1
9D6 M33_TPOS1 — LIU_TPOS1

J15 CONN_6P_U
9C6 M33_TCLK2 — LIU_TCLK2
9C6 M33_TNEG2 — LIU_TNEG2
9B6 M33_TPOS2 — LIU_TPOS2

J18 CONN_6P_U
9A6 M33_TCLK3 — LIU_TCLK3
9A6 M33_TNEG3 — LIU_TNEG3
9A6 M33_TPOS3 — LIU_TPOS3

DATA[7..0] — DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7

_ds3154_liublock_dn
HIERARCHY BLOCK

LIU_RCLK1 LIU_RNEG1 LIU_RPOS1
LIU_RCLK2 LIU_RNEG2 LIU_RPOS2
LIU_RCLK3 LIU_RNEG3 LIU_RPOS3

J12 CONN_6P_U
M33_RCLK1 9D8
M33_RNEG1 9D8
M33_RPOS1 9D8

J14 CONN_6P_U
M33_RCLK2 9C8
M33_RNEG2 9C8
M33_RPOS2 9B8

J17 CONN_6P_U
M33_RCLK3 9A8
M33_RNEG3 9A8
M33_RPOS3 9A8

ADDR[5..0] — ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5
21D2v 21D6v 1A2 10B5 1A8 8B5 21C2v 21C3v 21C6v
CS — TE3_L_CS 1A8 21C4v
RD_DS — RD_DS 8C1 10B5 1A8 1D3 21C4v
WR_RW — WR_RW 8C1 10B5 1A8 1D3 21C8v
INT — TE3_INT 21C7v 1B8 20D8v
RST — RESET_SYS 10B4 11B3 1A8 1B5 20B5v

1B1 10B5 1A8 8B3 8C3 11B3 9D4 8D6 21C2v 21C3v
21C8v 21D3v 21D7v

E3_MCLK_IO
T3_MCLK_IO
ALTERNATE_MCLK
M3X_CLKB
M3X_CLKA
M3X_CLADCLK_TO_LIU 6C6 20A5v
1D2 1D3 10B7 20A3v
10B7 20A2v

BUG FIX:
PCB REV 01A0 HAD THE
DATABUS TAPS WRONG [0:7]
THIS HAS BEEN FIXED IN THE FPGA.

J01 CONN_14P
M33_GPIOA1
M33_GPIOB1
M33_GPIOA2
M33_GPIOB2
M33_GPIOA3
M33_GPIOB3

RPB13 10K
RPB08 10K
RPB07 330
RPB04 330
RPB05 1K
RPB02 1K

V3_3

RED_GREEN DS07
RED_GREEN DS06
RED_GREEN DS01

TITLE: DS33M30M31M33EE01A0 T3E3 LIU I/F. P.2,9,20-22		DATE: 04/15/2007
ENGINEER: STEVE SCULLY		PAGE: 9/12(BLOCK) 9/26(TOTAL)

BLOCK NAME: _rc_top_dn_.

Downloaded from: http://www.datasheetcatalog.com/

overheadcpld_dn

HIERARCHY BLOCK

				CPLD_ATOH	CPLD_ATOH	2B7 23A5v
23A5v	2B7	CPLD_ATOHCLK	CPLD_ATOHCLK	CPLD_ATOHEN	CPLD_ATOHEN	2B7 23A5v
23A5v	2B7	CPLD_ATOHSOF	CPLD_ATOHSOF	CPLD_TAOH	CPLD_TAOH	2C7 23A6v
23A5v	2B7	CPLD_DTOH	CPLD_DTOH	CPLD_TAOHEN	CPLD_TAOHEN	2C7 23A6v
23A4v	2B7	CPLD_DTOHCLK	CPLD_DTOHCLK			
23A5v	2B7	CPLD_DTOHSOF	CPLD_DTOHSOF	M33_GPIOA1	M33_GPIOA1	9A5 9C6 23D6v
23A6v	2C7	CPLD_OH1	CPLD_OH1	M33_GPIOA2	M33_GPIOB1	9A5 9C6 23D6v
23A6v	2C7	CPLD_OHCLK	CPLD_OHCLK	M33_GPIOA3	M33_GPIOB2	9A5 9B6 23D6v
23A6v	2C7	CPLD_RDOH	CPLD_RDOH	M33_GPIOB1	M33_GPIOA3	9A5 9B6 23D6v
23A5v	2C7	CPLD_RDOHSOF	CPLD_RDOHSOF	M33_GPIOB2	M33_GPIOB3	9A5 9A6 23D6v
23A5v	2B7	CPLD_RDOHVLD	CPLD_RDOHVLD	M33_GPIOB3		9A5 9A6 23D6v
23A6v	2C7	CPLD_TAOHSOF	CPLD_TAOHSOF			
23A6v	2C7	CPLD_TAOHVLD	CPLD_TAOHVLD			
23D7v	1D3 6C6	M3X_CLADCLK	CP_DUT_CLADCLK	CPU_RESET	RESET_SYS	9B1 11B3 1A8 1B5 24B4v
23D7v	9B2 1D3	M3X_CLKA	CP_DUT_CLKA	RD	RD_DS	8C1 9C1 1A8 1D3 23C7v
23D7v	9B2 1D2	M3X_CLKB	CP_DUT_CLKB	WR	WR_RW	8C1 9C1 1A8 1D3 23C7v
23D7v	6A7 1D2	M3X_CLKC	CP_DUT_CLKC	CPLD_CS	CPLD_CS	1A8 23C7v
				ADDR<3..0>	ADDR<3..0>	1A2 9C1 1A8 8B5 23B7v 23C7v
				DAT<7..0>	DATA<7..0>	1B1 9C3 1A8 8B3 8C6 8D3 8D4 8D6 23B4v 23C4v

U05

DS33M33_U

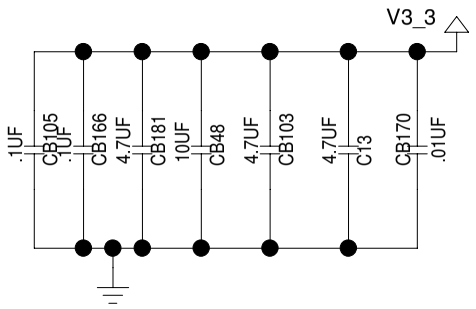
PWR & GND

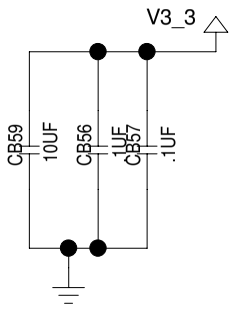
V1_8	K1	CVDD_1.8V
V1_8	M1	CVDD_1.8V
		VDD18[12..1]
		VDD33[6..1]
V3_3	M15	HVDDA_3.3V
	F15	HVDDB_3.3V
V1_8	K15	RVDDA_1.8V
	D15	RVDDB_1.8V
	P15	TVDDA_1.8V
	H15	TVDDB_1.8V
	D1	TVDD1_1_8V
	F1	TVDD2_1_8V
	H1	TVDD3_1_8V
V1_8 V2_5	B16	AVDD_1.8V
	E5	VDDP_2.5V
	E9	VDDP_2.5V
	E12	VDDP_2.5V
		VDDQ_2.5V[7..1]
7D5 7D2 DDR_VREF	E8	VREF
	A16	AVSS
	L1	CVSS1
	N1	CVSS2
	L15	RHVSSA
	E15	RHVSSB
	N15	TVSSA
	G15	TVSSB
	E1	TVSS1
	G1	TVSS2
	J1	TVSS3
		VSSI[22..1]
		VSSQ[7..1]

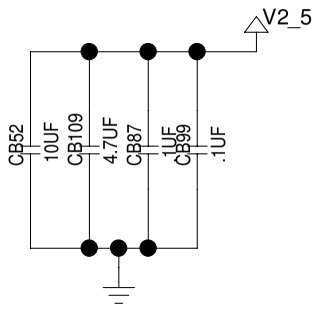
TITLE: DS33M33DK01A0 OVERHEAD. P.2,10,23-24	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 10/12(BLOCK) 10/26(TOTAL)

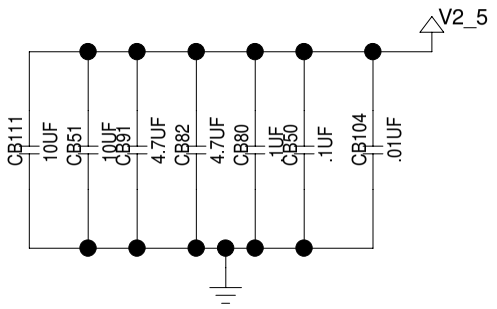
BLOCK NAME: _rc_top_dn_.

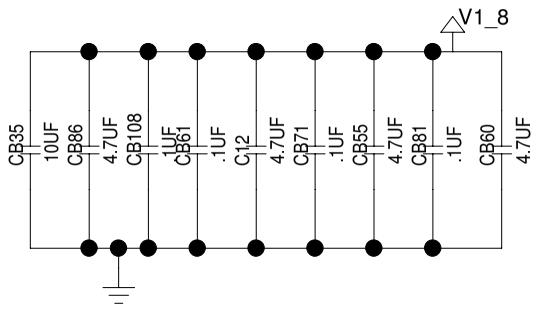
Downloaded from: http://www.datasheetcatalog.com/

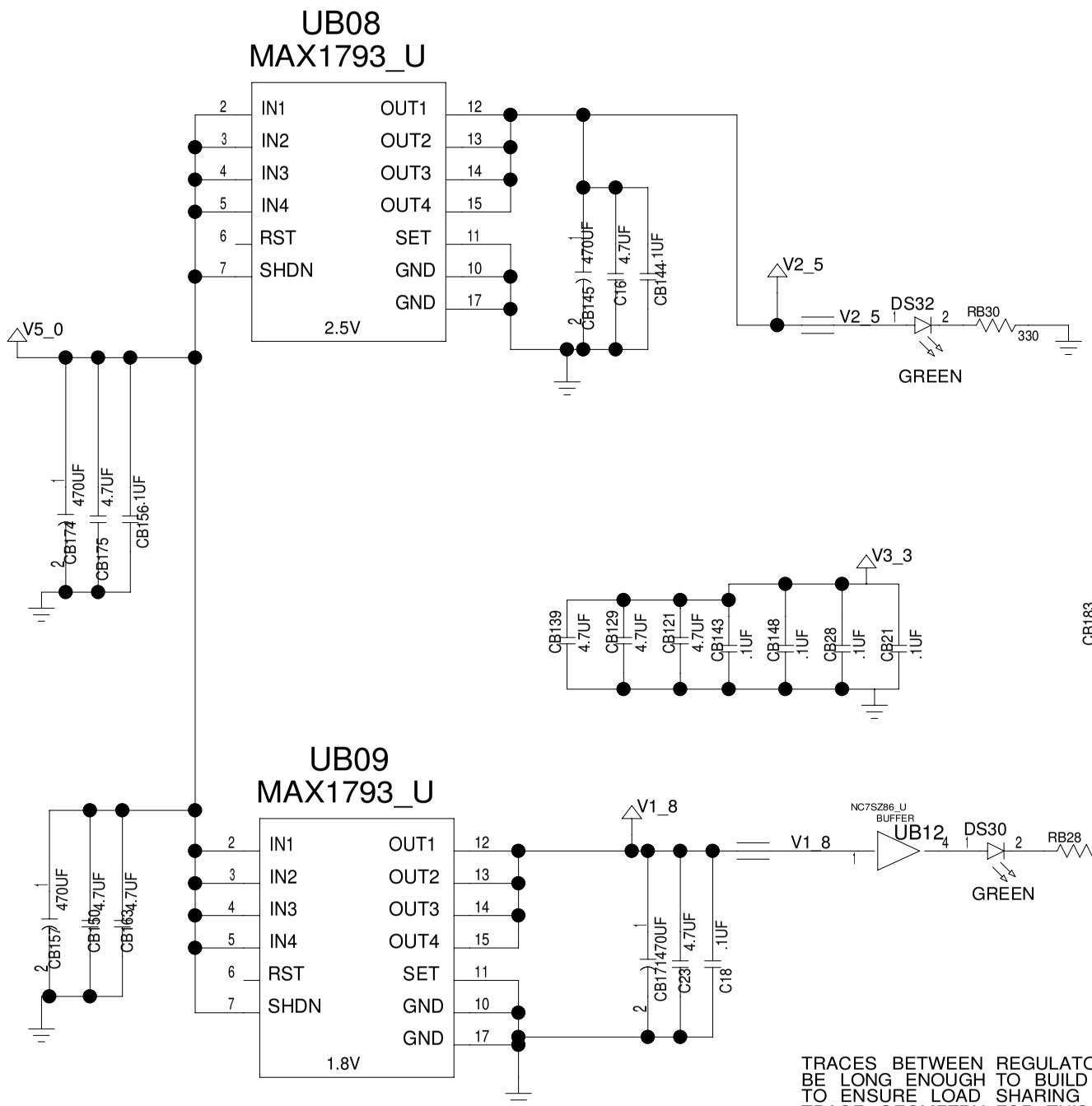


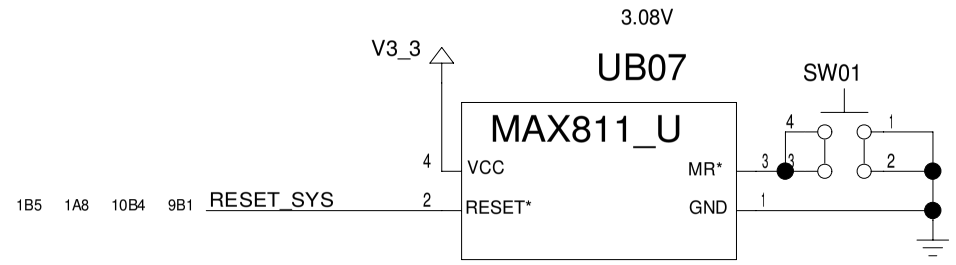


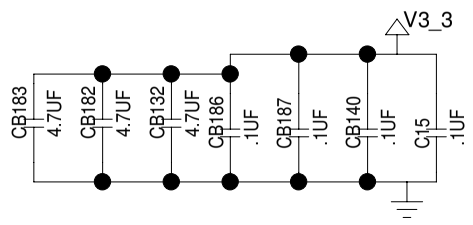


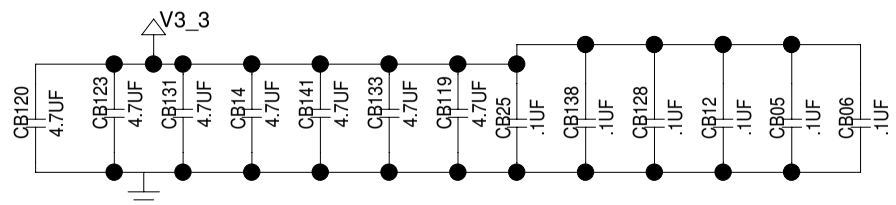


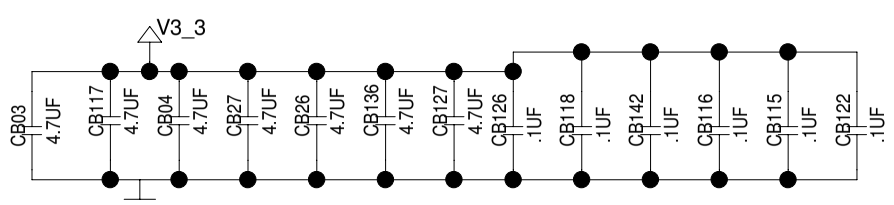












TRACES BETWEEN REGULATOR OUTPUT AND V2.5 SHOULD BE LONG ENOUGH TO BUILD 0.05 OHM OF RESISTANCE TO ENSURE LOAD SHARING BETWEEN THE 2.5V 1% REGULATORS TRACE GEOMETRY FOR THIS IS: 1 INCH LONG, 10 MIL WIDE, 1 OZ COPPER

TITLE: DS33M33DK01A0 POWER. P.11-12	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 11/12(BLOCK) 11/26(TOTAL)

BLOCK NAME: _rc_top_dn_. PARENT BLOCK: <CON_PARENT_NAME>

Downloaded from: http://www.datasheetcatalog.com/

V3_3

CB13 10UF
CB173 4.7UF
CB172 .1UF
CB179 .1UF
CB190 4.7UF
CB180 .1UF
CB149 .1UF
CB169 10UF
CB162 4.7UF
CB151 .1UF
CB152 .1UF
CB167 4.7UF
CB161 .1UF
CB155 .1UF

3.3V
UB11
MAX1793_U

V5_0

IN1 2
IN2 3
IN3 4
IN4 5
RST 6
SHDN 7
OUT1 12
OUT2 13
OUT3 14
OUT4 15
SET 11
GND 10
GND 17

68UF CB159
C21 10UF
R04 0.0
R02 0.0

3.3V
UB10
MAX1793_U

V5_0

IN1 2
IN2 3
IN3 4
IN4 5
12A4 POWEROK
RST 6
SHDN 7
OUT1 12
OUT2 13
OUT3 14
OUT4 15
SET 11
GND 10
GND 17

C19 10UF

3.3V 1% REGULATOR

V3_3

R03 0.0

CB176 470UF
CB153 4.7UF
CB154 4.7UF

V5_0

DS31
GREEN
RED
RED
GREEN

RPB59
330

POWEROK 12A8

UB13
MAX1793_U

0.0 R05

OUT1 12
OUT2 13
OUT3 14
OUT4 15
SET 11
GND 10
GND 17
IN1 2
IN2 3
IN3 4
IN4 5
RST 6
SHDN 7

3.3V

10UF C24
68UF CB158

100O100MZH

JB09
L1
C1 10UF

V5_0

68UF CB189
68UF CB185
C17 10UF
CB188 10UF
C20 10UF
C22 10UF

DB01
1 AMP

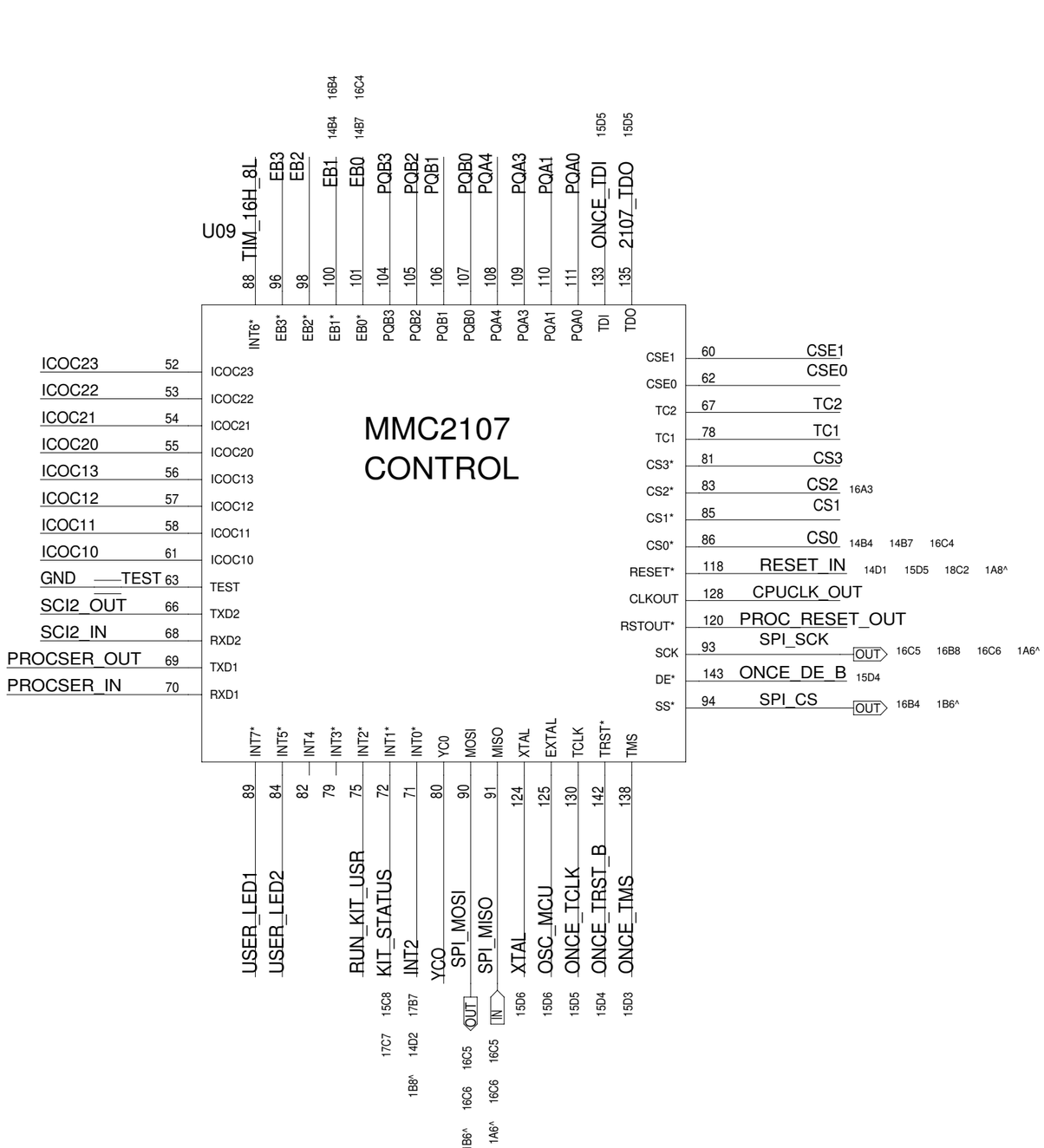
GND_TPB06
GND_TPB03
GND_TP11
GND_TP04
GND_TP02
GND_TP03
GND_TPB02
GND_TPB01
GND_TP01

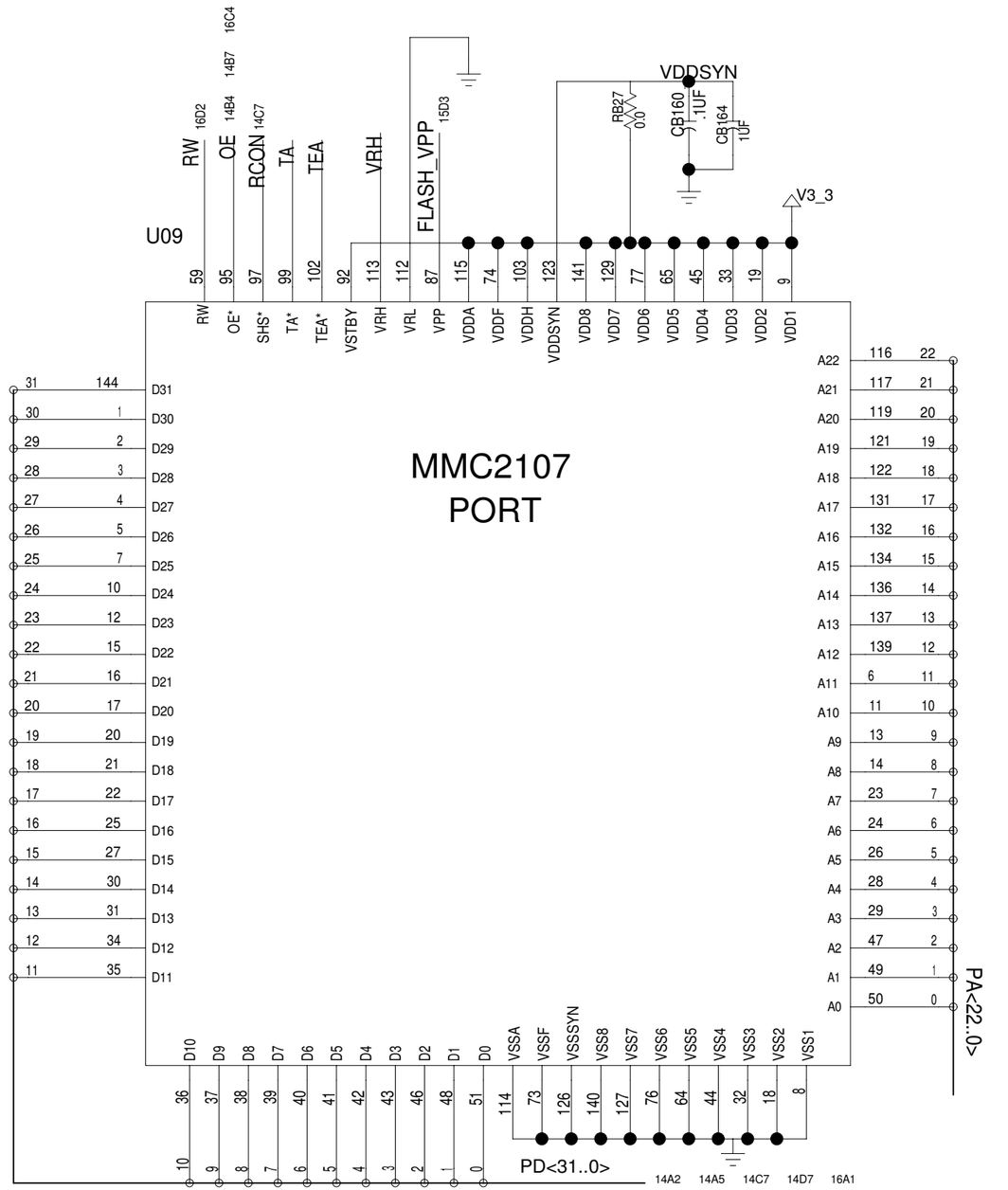
MOUTING HARDWARE
HB03 HB02 HB04
HB01 HB05

TITLE: DS33M33DK01A0 POWER. P.11-12	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 12/12(BLOCK) 12/26(TOTAL)

BLOCK NAME: _rc_top_dn_. PARENT BLOCK: <CON_PARENT_NAME>

Downloaded from: http://www.datasheetcatalog.com/





BEGINNING OF PROCESSOR HIERARCHY BLOCK

TITLE: DS33M33DK01A0 MICROPORT. P.1,13-18	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/6(BLOCK) 13/26(TOTAL)

Downloaded from: http://www.datasheetcatalog.com/

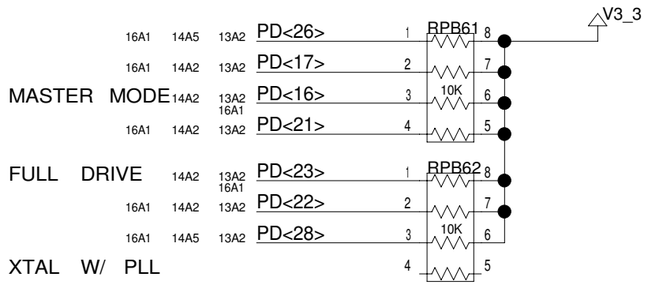
RESET CONFIGURATION

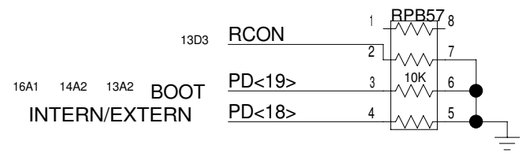
MASTER MODE

FULL DRIVE

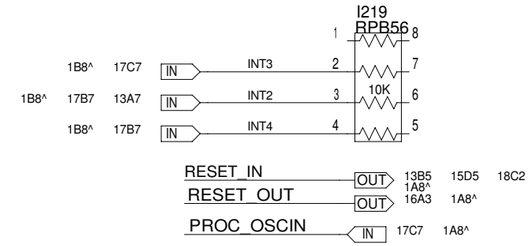
XTAL W/ PLL

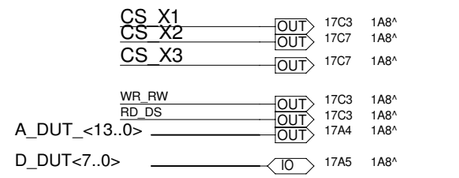
INTERNAL
FLASH ENABLE

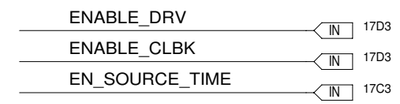




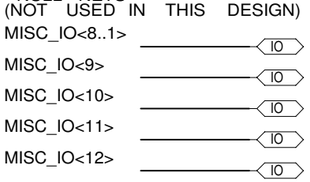
WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND

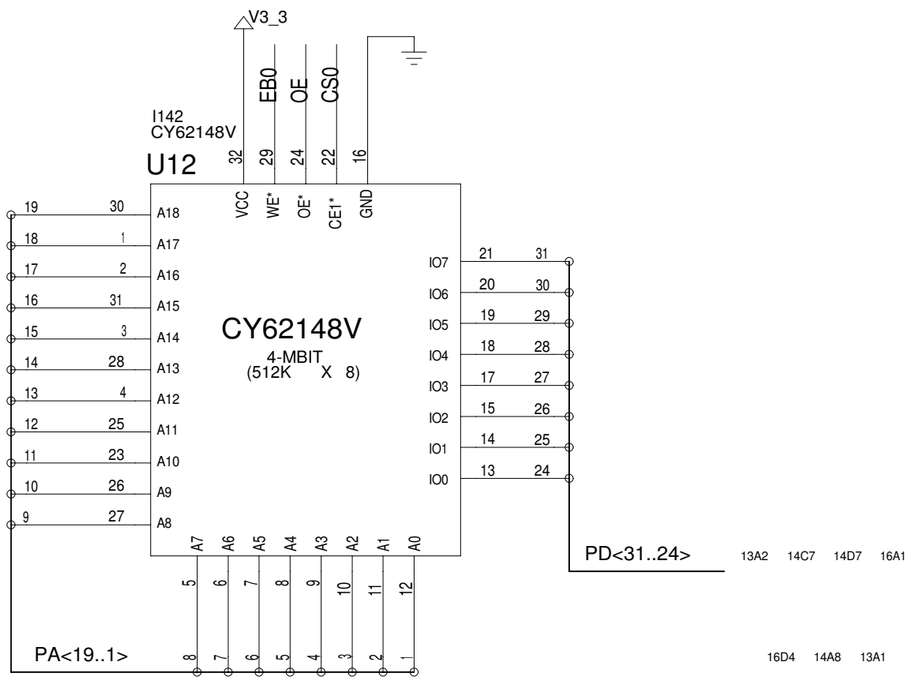


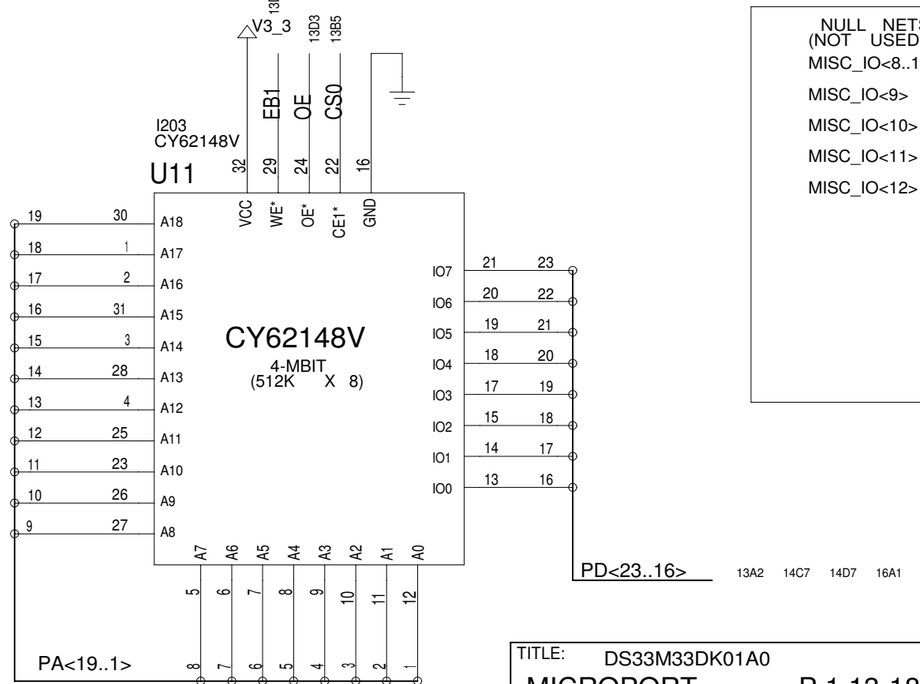




NULL NETS
(NOT USED IN THIS DESIGN)







TITLE: DS33M33DK01A0 MICROPORT. P.1,13-18	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 2/6(BLOCK) 14/26(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _rc_top_dn_\

Downloaded from: http://www.datasheetcatalog.com/

J33
CON14P

XB01
8.0MHZ
R03
1.0M
PLACE PADS FOR CAP
BUT DO NOT POPULATE
OSC_MCU 13A6
XTAL 13A7

DS29
GREEN
KIT_STATUS
17C7 13A7
RB26
330

CON14P
13D6 ONCE_TDI
13D6 2107_TDO
13A6 ONCE_TCLK
ALIGN KEY
1A8^ 18C2 14D1 13B5 V3_3
RESET_IN
ONCE_TMS 13A6
13B5 ONCE_DE_B
13A6 ONCE_TRST_B
V5_0
FLASH_VPP
JB08
RPB64
10K
V3_3

UB14
MAX3233E
1 R2OUT
2 INVALID*
3 T2IN
15A5 UART_DIGIN 4 T1IN
5 FORCEON
15A5 UART_DIGOUT 6 R1OUT
15A8 PRT1_OUT 7 T1OUT
15A8 PRT1_IN 8 R1IN
9 VCC
10 FORCEOFF*
20 R2IN
19 T2OUT
18 GND
17 V-
16 C2-
15 C2+
14 C1-
13 C1+
12 V+2
11 V+1
V3_3

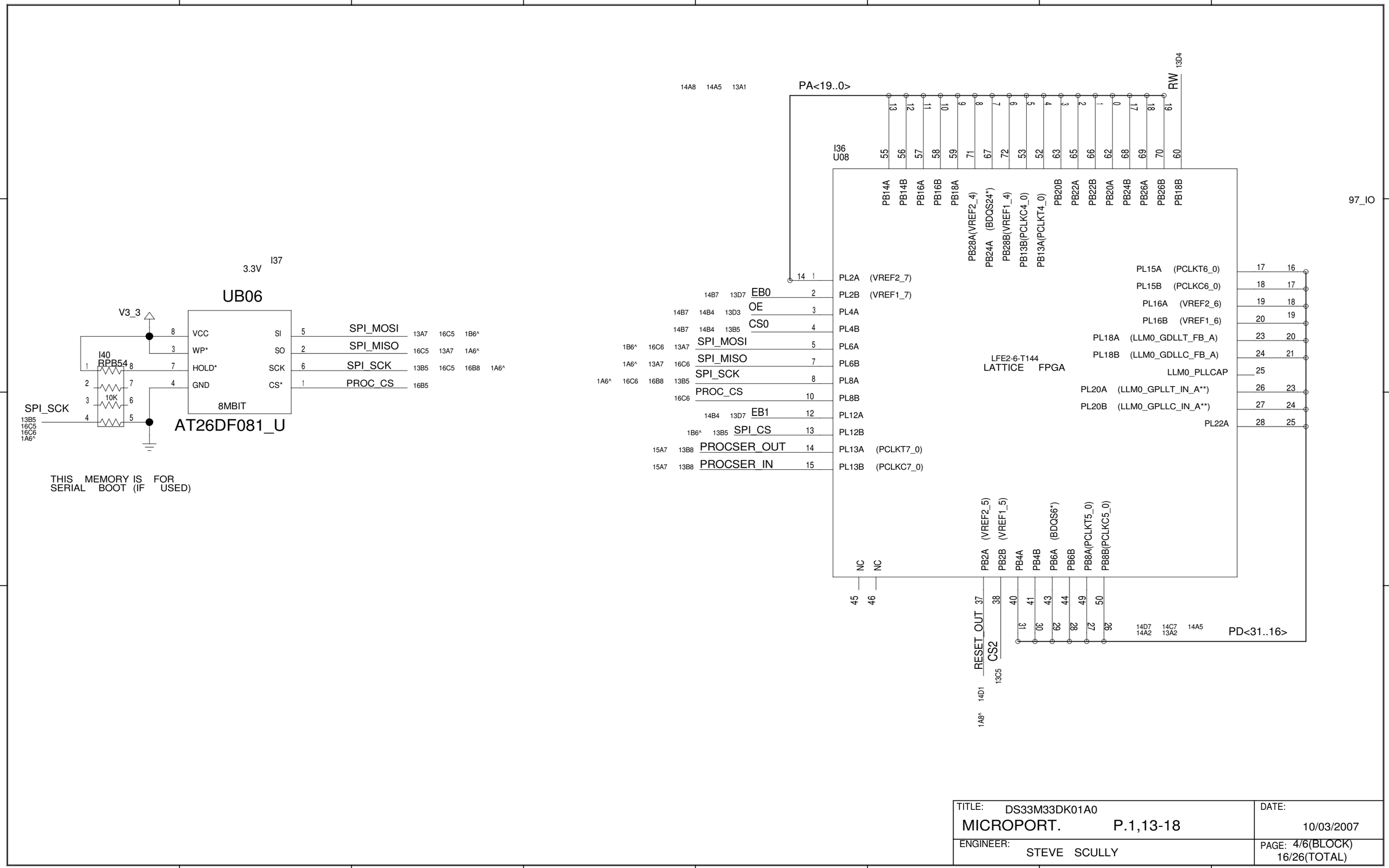
USB
J35
VDD
DAT-
DAT+
GND
RB29 10K
CB178 4.7UF
CB177 .1UF
VDD IS A (UNUSED) OUTPUT ON CP2101 CHIP
U10
CP2101
5 USBDM
4 USBDP
8 VBUS
9 RST*
7 REGIN
15B2 SSPL 11 SUSPEND_LOW*
12 SUSPEND_HIGH
CB184 1UF
GND
NC1 NC2 NC3 NC4 NC5 NC6
TXD 26 USB_DOUT 15A5
RXD 25 USB_DIN 15B5
RTS* 24
CTS* 23
DTR* 28
DSR* 27
DCD* 1
RI* 2
15B4 NC7 18
NC8 19
NC9 20
NC10 21
NC11 22
RPB58
RPB60
10K
SSPL
DTR AND RTS USE RPACK CONNECTION AS TESTPOINTS

16B5 13B8 PROCSER_OUT 2
JP25
USB_DIN 15B2
UART_DIGIN 15B8
16B5 13B8 PROCSER_IN 2
JP26
USB_DOUT 15B2
UART_DIGOUT 15B8

J34
CONN_DB9P
PRT1_OUT 15B8 2 B
PRT1_IN 15B8 3 C
A 1
D 4
E 5
F 6
G 7
H 8
J 9
RPB63
10K
V3_3

TITLE: DS33M33DK01A0 MICROPORT. P.1,13-18	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 3/6(BLOCK) 15/26(TOTAL)

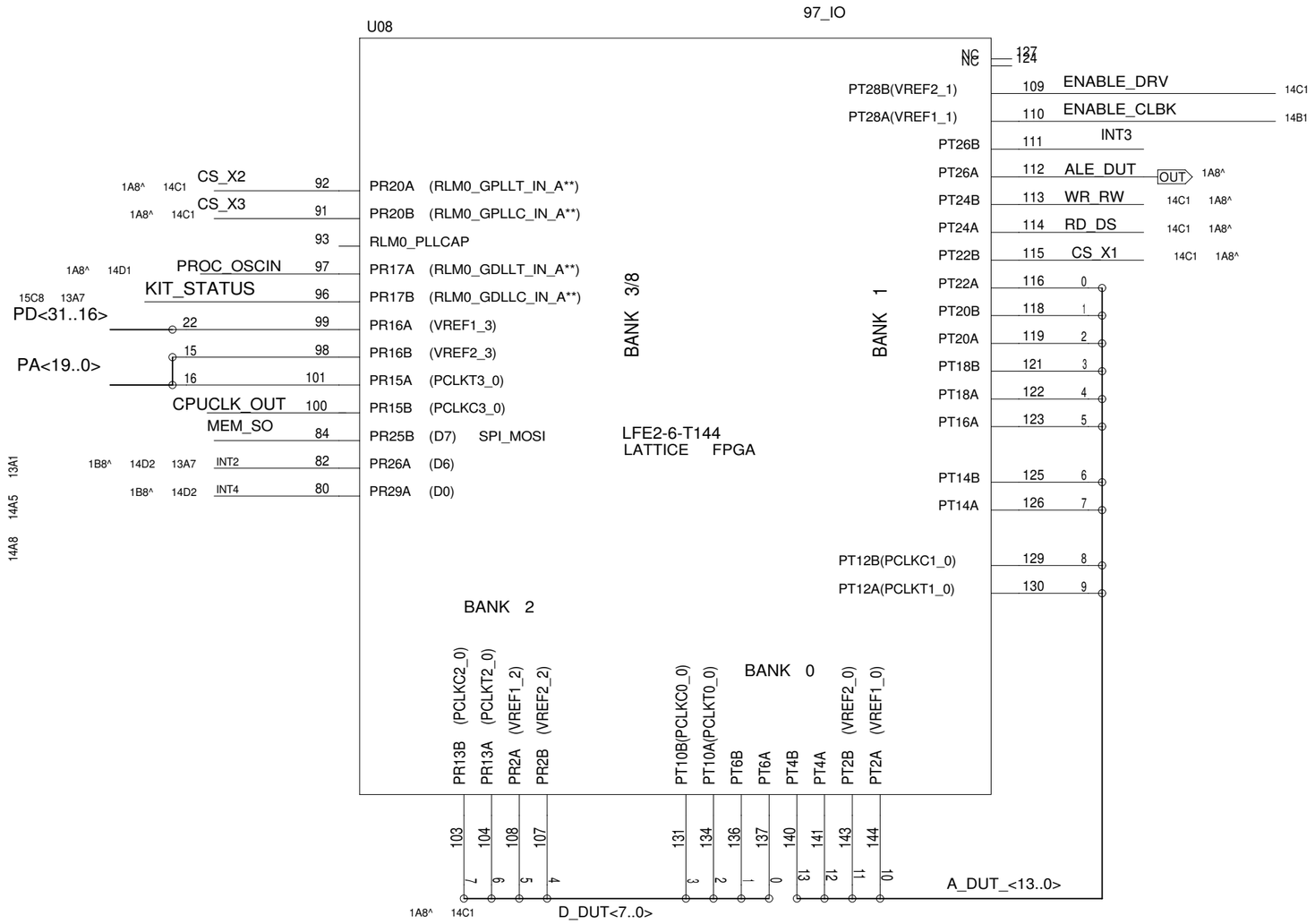
BLOCK NAME: motprocrescard_dn. PARENT BLOCK: \ rc_top_dn \



TITLE: DS33M33DK01A0 MICROPORT. P.1,13-18	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 4/6(BLOCK) 16/26(TOTAL)

Downloaded from: http://www.datasheetcatalog.com/

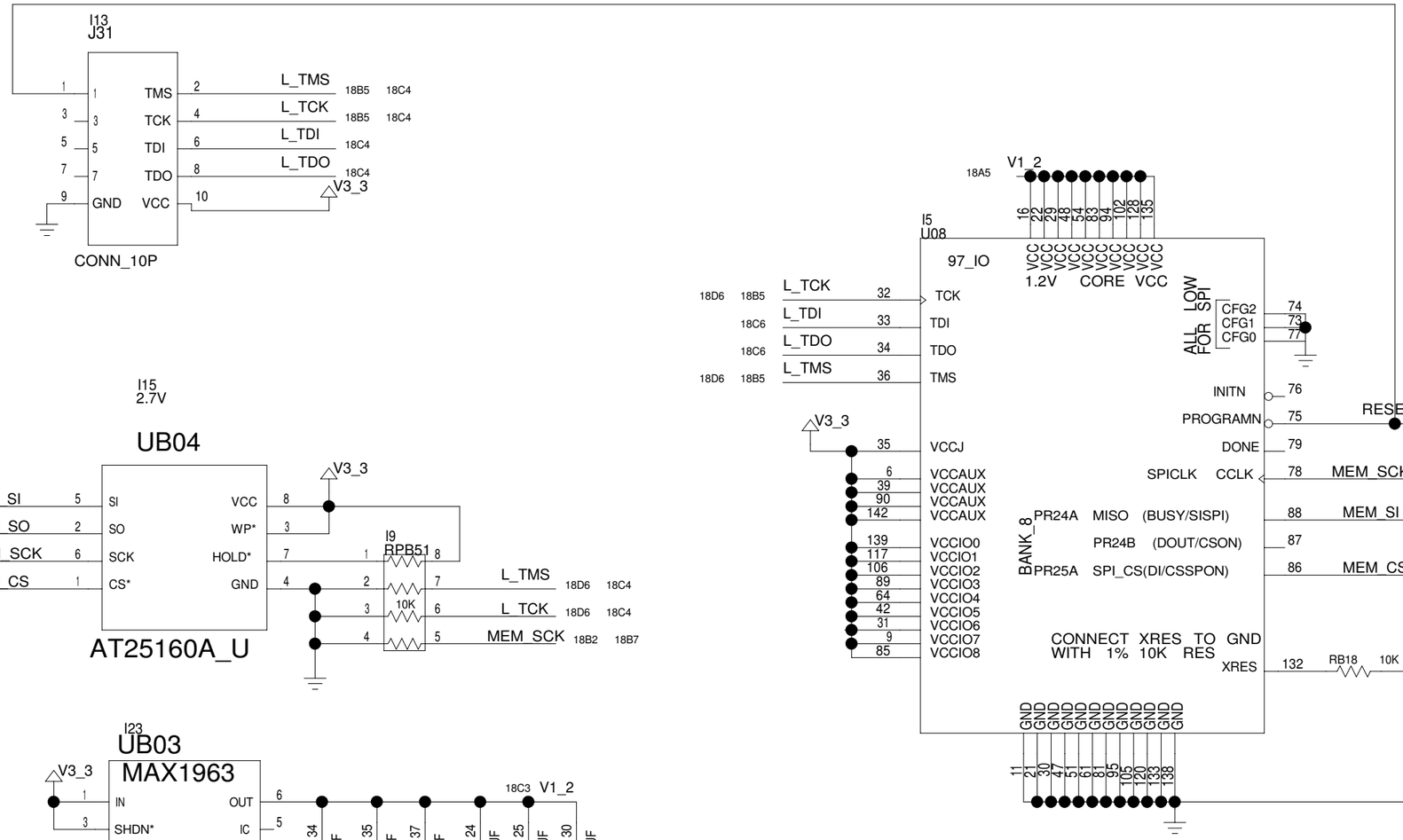
Downloaded from: http://www.datasheetcatalog.com/



TITLE: DS33M33DK01A0 MICROPORT. P.1,13-18	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 5/6(BLOCK) 31/39(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _rc_top_dn_\

Downloaded from: http://www.datasheetcatalog.com/



TITLE: DS33M33DK01A0 MICROPORT. P.1,13-18	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 31/39(TOTAL)

BLOCK NAME: _motprocrescard_dn. PARENT BLOCK: _rc_top_dn_\

Downloaded from: http://www.datasheetcatalog.com/

V3_3 I67 V3_3

I68 GND

JB03
SMT
SFM-125-L2-S-D-LC
NA
I78

6B3^ 19C4 19A8 RESET_B — PT1_RXD<3..0> 19C1 19C2 6D3^
6C3^ 19C4 19D1 PT1_TXD<3..0>
V1_8
PT1_RX_CRS 19C2 19D1 6D3^
PT1_RXDV 19C1 19C2 6D3^
6C3^ 19D1 19C4 PT1_TX_EN
6C3^ 19D1 19C4 PT1_TX_CLK
V3_3
PT1_RX_CLK 19C2 19D1 6D3^
PT1_COL_DET 19C2 19D1 6D3^
6B1^ 19B4 19A4 GMII_CLKFROM_MAC
PT1_RX_ERR 19B2 19D1 6C3^
6B1^ 19B4 19A4 GMII_TX_ER_
6B1^ 19B4 19A4 GMII_CLKTOMAC_BUF
PHY_INT 19A8 19B2 6B3^
6B3^ 19B4 IO OSC25M
SPARE 19A7 19B2
6B3^ 19B4 19A8 LAN_CLK
PT2_RXD<3..0> 19B1 19B2 6C3^
6C3^ 19B4 19C1 PT2_TXD<3..0>
PT2_RX_CRS 19B2 19C1
PT2_RXDV 19B2 19C1
19C1 19B4 PT2_TX_EN
V2_5
19C1 19A4 PT2_TX_CLK
PT2_RX_CLK 19A2 19C1
6B3^ 19A8 19A4 MDIO
PT2_COL_DET 19A2 19C1
6B3^ 19A8 19A4 MDC
PT2_RX_ERR 19A2 19C1

JB02
SMTTP
NA_NOTPOPULATED
NA
I130

6B3^ 19C7 19A8 RESET_B — PT1_RXD<3..0> 19C1 19C6 6D3^
6C3^ 19C8 19D1 PT1_TXD<3..0>
V1_8
PT1_RX_CRS 19C6 19D1 6D3^
PT1_RXDV 19C1 19C6 6D3^
6C3^ 19D1 19C8 PT1_TX_EN
V3_3
6C3^ 19D1 19C8 PT1_TX_CLK
PT1_RX_CLK 19C6 19D1 6D3^
PT1_COL_DET 19C6 19D1 6D3^
6B1^ 19B8 19A4 GMII_CLKFROM_MAC
PT1_RX_ERR 19B6 19D1 6C3^
6B1^ 19B8 19A4 GMII_TX_ER_
6B1^ 19B8 19A4 GMII_CLKTOMAC_BUF
PHY_INT 19A8 19B6 6B3^
6B3^ 19B8 IO OSC25M
SPARE 19A7 19B6
6B3^ 19B8 19A8 LAN_CLK
PT2_RXD<3..0> 19B1 19B6 6C3^
6C3^ 19B8 19C1 PT2_TXD<3..0>
PT2_RX_CRS 19B6 19C1
PT2_RXDV 19B6 19C1
19C1 19B8 PT2_TX_EN
V2_5
19C1 19A8 PT2_TX_CLK
PT2_RX_CLK 19A6 19C1
6B3^ 19A8 MDIO
PT2_COL_DET 19A6 19C1
6B3^ 19A8 MDC
PT2_RX_ERR 19A6 19C1

PT1_TXD<3..0> IO
PT1_TX_EN IO
PT1_TX_CLK IO
PT1_RX_CLK IO
PT1_COL_DET IO
PT1_RX_ERR IO
PT1_RX_CRS IO
PT1_RXDV IO
PT1_RXD<3..0> IO

PT2_TXD<3..0> IO
PT2_TX_EN IO
PT2_TX_CLK IO
PT2_RX_CLK IO
PT2_COL_DET IO
PT2_RX_ERR IO
PT2_RX_CRS IO
PT2_RXDV IO
PT2_RXD<3..0> IO

CONNECTORS FOR LAN MOTHERBOARD TO RESOURCE CARD

LAN_CLK IO
MDC IO
MDIO IO
RESET_B IO
PHY_INT IO

19B6 19B2 SPARE IO

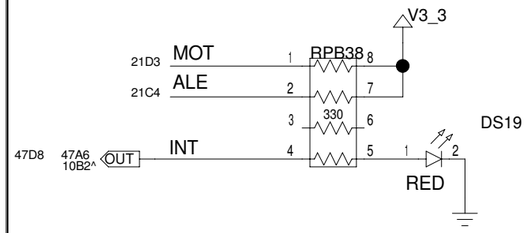
GMII_CLKFROM_MAC IO 19B4 19B8 6B1^
GMII_TX_ER_ IO 19B4 19B8 6B1^
GMII_CLKTOMAC_BUF IO 19B4 19B8 6B1^

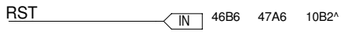
BEGIN/END PHY CONNECTOR HIERARCHY BLOCK

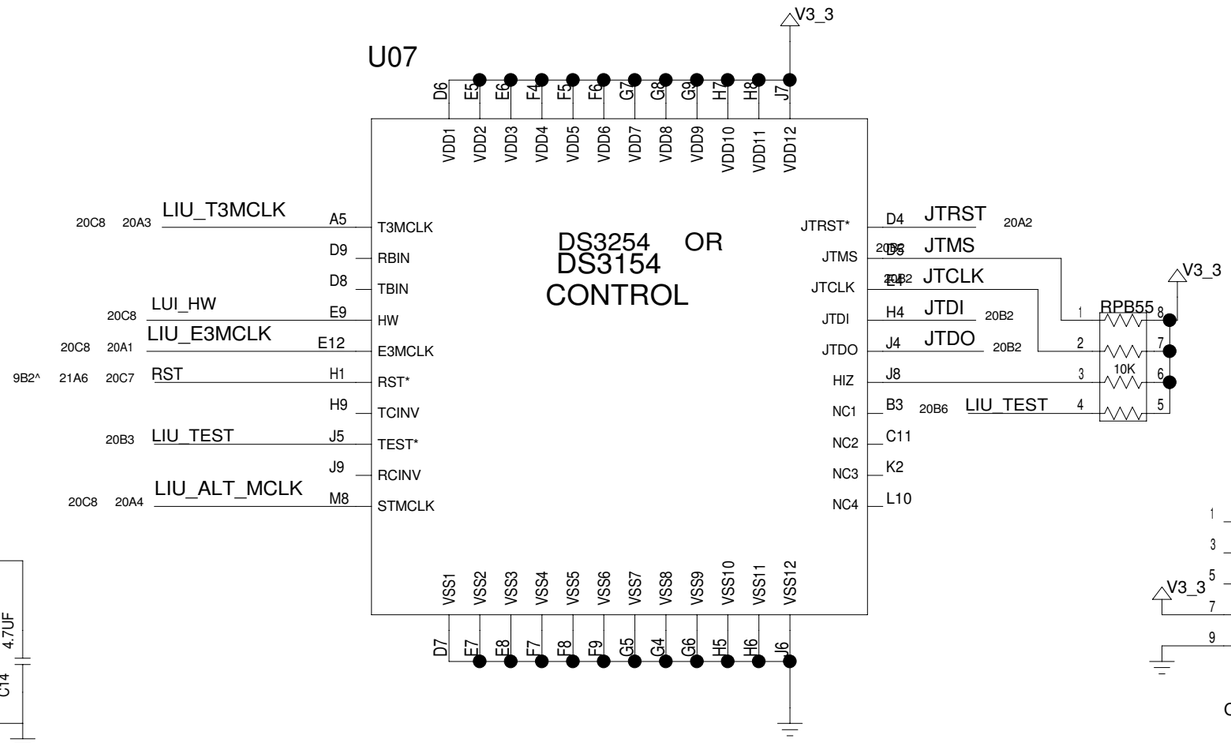
TITLE: DS33M33DK01A0 ETHERNET. P.5-6,19,25-26	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 19/26(TOTAL)

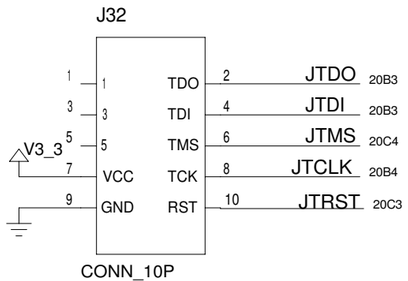
BLOCK NAME: _phy_imbus_mb_dn. PARENT BLOCK: _rc_top_dn_\

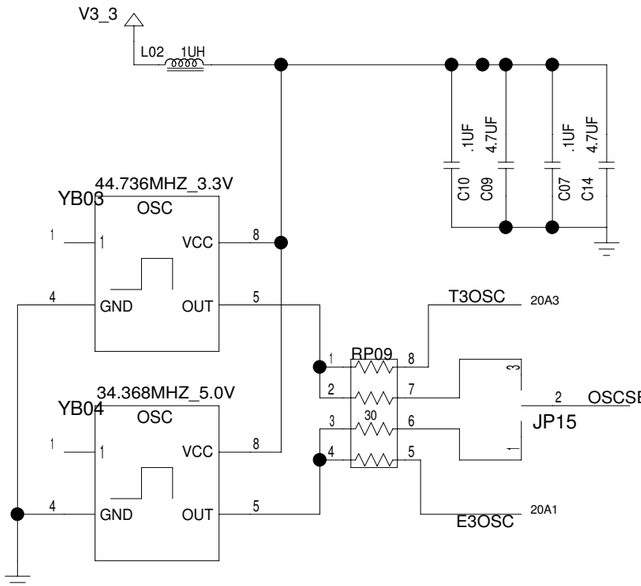
Downloaded from: http://www.datasheetcatalog.com/

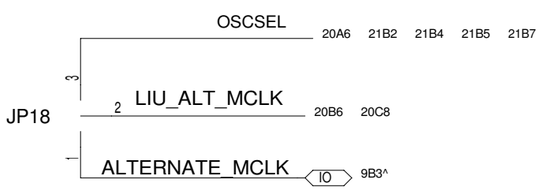


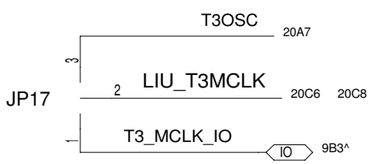


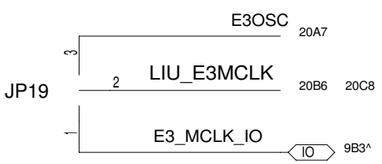












ALTERNATE_MCLK:
REG CACR[AMCSEL1:0]=00 FOR 19.44MHZ
REG CACR[AMCSEL1:0]=10 FOR 77.76MHZ

BEGIN LIU HIERARCHY BLOCK

TITLE: DS33M33DK01A0 T3E3 LIU I/F. P.2,9,20-22	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/3(BLOCK) 20/26(TOTAL)

BLOCK NAME: _ds3154_liublock_dn. PARENT BLOCK: _rc_top_dn_\

Downloaded from: http://www.datasheetcatalog.com/

PORT LOCATIONS
RLOS1 IS AT PIN A1
RLOS2 IS AT PIN M12
RLOS3 IS AT PIN A12

PORT 4 OF DS3254 IS NOT USED WITH DS33M33
IT IS A SPARE PORT IN THIS DESIGN
DS3253 IS RECOMMENDED FOR DS33M33

U07 DS3254 OR

DS3154 PORT

RLOS1 A1 — RLOS* — PRBS — B1 PRBS1 22C8 22B7
RPOS1 C2 — RPOS — TPOS — D1 LIU_TPOS1 IN
RNEG1 C3 — RNEG — TNEG — D2 LIU_TNEG1 IN
A4 — RMON — TDSB — G3 DATA4 21A8 9C3^
INT C5 — RLB — TLBO — E3 DATA0 21A8 9C2^
RCLK1 C1 — RCLK — TCLK — E1 LIU_TCLK1 IN
RTS1 B2 — RTS* — TTS* — E2 TTS1 22C8 22D8
B4 — RJA — TJA — C4
DATA1 F2 — STS — TDSA — G2 DATA3 21A8 9C3^
WR_RW B5 — LLB — TDM* — D3 TDM1 9C2^ 21A8
DATA2 F3 — E3M
RXP1 A3 — RXP — TXP — F1 TXP1 22D5 22A5
RXN1 A2 — RXN — TXN — G1 TXN1 22D5 22A5

U07 DS3254 OR

DS3154 PORT

RLOS2 M12 — RLOS* — PRBS — L12 PRBS2 22C8
RPOS2 K11 — RPOS — TPOS — J12 LIU_TPOS2 IN
RNEG2 K10 — RNEG — TNEG — J11 LIU_TNEG2 IN
M9 — RMON — TDSB — F10
ADDR4 K8 — RLB — TLBO — H10
RCLK2 K12 — RCLK — TCLK — H12 LIU_TCLK2 IN 47B5
RTS2 L11 — RTS* — TTS* — H11 TTS2 22C8
L9 — RJA — TJA — K9
G11 — STS — TDSA — F11
ADDR5 L8 — LLB — TDM* — J10 TDM2 22A7
G10 — E3M
RXP2 M10 — RXP — TXP — G12 TXP2 22B5
RXN2 M11 — RXN — TXN — F12 TXN2 22B5

U07 DS3254 OR

DS3154 PORT

RLOS3 A12 — RLOS* — PRBS — A11 PRBS3 22B8 22B7
RPOS3 B10 — RPOS — TPOS — A9 LIU_TPOS3 IN
RNEG3 C10 — RNEG — TNEG — B9 LIU_TNEG3 IN
D12 — RMON — TDSB — C6 MOT 20D8
E10 — RLB — TLBO — C8 9C3^ 21A8
RCLK3 A10 — RCLK — TCLK — A8 LIU_TCLK3 IN
RTS3 B11 — RTS* — TTS* — B8 TTS3 22C8 22C8
D11 — RJA — TJA — D10
CS B7 — STS — TDSA — B6 RD_DS 9C2^ 21A8
E11 — LLB — TDM* — C9 TDM3 22A7 9C3^ 21A8
ALE C7 — E3M 9C2^ 21A8
RXP3 C12 — RXP — TXP — A7 TXP3 22D3 22A3
RXN3 B12 — RXN — TXN — A6 TXN3 22D3 22A3

U07 DS3254 OR

DS3154 PORT

RLOS4 M1 — RLOS* — PRBS — M2 PRBS4 22B8
RPOS4 L3 — RPOS — TPOS — M4 LIU_TPOS4 21A4
RNEG4 K3 — RNEG — TNEG — L4 LIU_TNEG4 21A4
J1 — RMON — TDSB — K7 ADDR2 21A8 9C2^
DATA6 H3 — RLB — TLBO — K5
RCLK4 M3 — RCLK — TCLK — M5 LIU_TCLK4 21A4 21B2
RTS4 L2 — RTS* — TTS* — L5 TTS4 22C8
J2 — RJA — TJA — J3 DATA7 21A8 9C3^
ADDR1 L6 — STS — TDSA — L7 ADDR3 21A8 9C2^
DATA5 H2 — LLB — TDM* — K4 TDM4 22A7
ADDR0 K6 — E3M
RXP4 K1 — RXP — TXP — M6 TXP4 22B3
RXN4 L1 — RXN — TXN — M7 TXN4 22B3

RPB35 (30)
RCLK1 21C8 — 2 — 7 LIU_RCLK1 OUT 47B7
RPOS1 21D8 — 3 — 6 LIU_RPOS1 OUT
RNEG1 21D8 — 4 — 5 LIU_RNEG1 OUT

RPB37 (30)
RCLK2 21C6 — 7 — 2 LIU_RCLK2 OUT 47B5
RPOS2 21D6 — 6 — 3 LIU_RPOS2 OUT
RNEG2 21D6 — 5 — 4 LIU_RNEG2 OUT

RPB31 (30)
RCLK3 21C4 — 2 — 7 LIU_RCLK3 OUT 47B4
RPOS3 21D4 — 3 — 6 LIU_RPOS3 OUT
RNEG3 21D4 — 4 — 5 LIU_RNEG3 OUT

RPB44 (30)
RCLK4 21C3 — 2 — 7 LIU_RCLK4 21A3 21B2
RPOS4 21D3 — 3 — 6 LIU_RPOS4 21A3
RNEG4 21D3 — 4 — 5 LIU_RNEG4 21A3

JMP_3 JP16: OSCSEL 20A4 20A6 21B2 21B4 21B5 — 2 LIU_TCLK1 21C6 — LIU_RCLK1 21B7

JMP_3 JP24: OSCSEL 20A4 20A6 21B2 21B4 21B7 — 2 LIU_TCLK2 21C5 — LIU_RCLK2 21B5

JMP_3 JP23: OSCSEL 20A4 20A6 21B2 21B5 21B7 — 2 LIU_TCLK3 21C3 — LIU_RCLK3 21B3

JMP_3 JPB01: OSCSEL 20A4 20A6 21B4 21B5 21B7 — 2 LIU_TCLK4 21A4 21C1 — LIU_RCLK4 21A3 21B2

JB07
CONN_6P_U

21D1	LIU_TPOS4	1	2	LIU_RCLK4	21B2
21D1	LIU_TNEG4	3	4	LIU_RPOS4	21B2
21C1 21B2	LIU_TCLK4	5	6	LIU_RNEG4	21B2

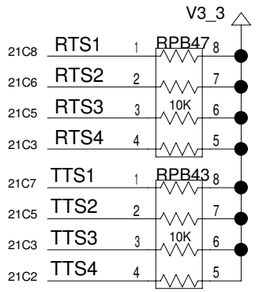
DATA0 IO 21D7 9C3^
DATA1 IO 21C8 9C3^
DATA2 IO 21C8 9C3^
10C2^ 47C3 DATA3 IO IN ADDR0 21C7 9C3^
10C2^ 47C3 DATA4 IO IN ADDR1 21D7 9C3^
10C2^ 47D2 DATA5 IO IN ADDR2 21C3 9C3^
10C2^ 47C2 DATA6 IO IN ADDR3 21D3 9C3^
10C2^ 47D6 DATA7 IO IN ADDR4 21C2 9C3^
10C2^ 47C6 IN ADDR5

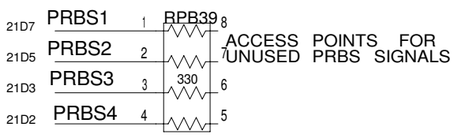
RST IN 46B6 46C7 10B2^
INT OUT 46D8 47D8 10B2^
CS IN 47C4 10C2^
RD_DS IN 47C3 10C2^
WR_RW IN 47C8 10C2^

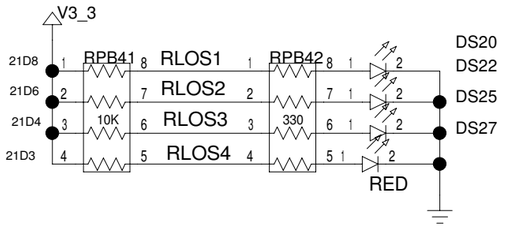
TITLE: DS33M33DK01A0 T3E3 LIU I/F. P.2,9,20-22	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 2/3(BLOCK) 21/26(TOTAL)

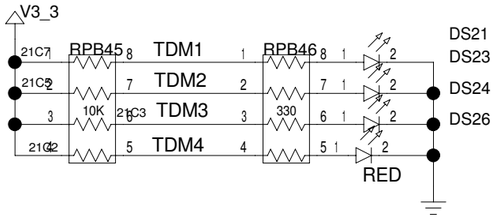
BLOCK NAME: _ds3154_liublock_dn. PARENT BLOCK: _rc_top_dn_\

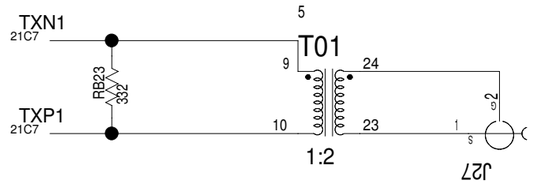
Downloaded from: http://www.datasheetcatalog.com/

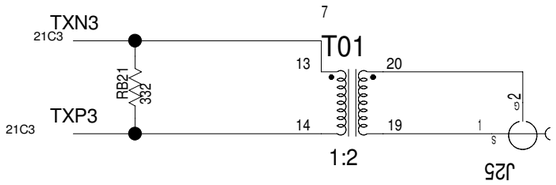


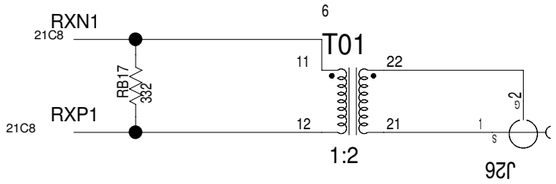


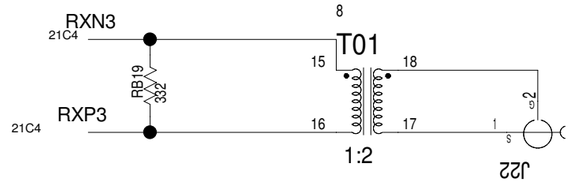


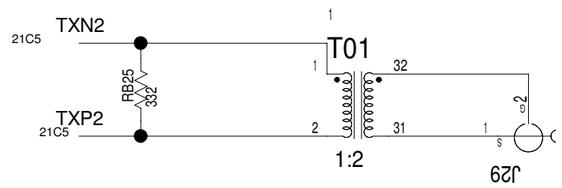


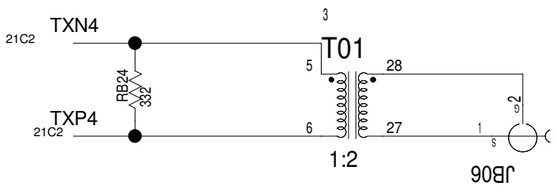


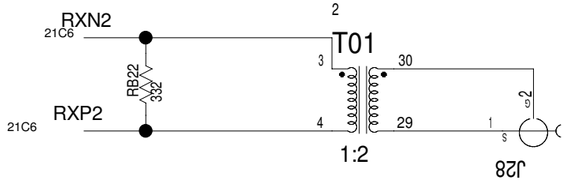


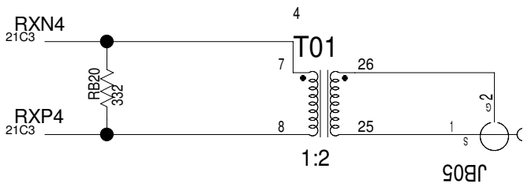












END LIU HIERARCHY BLOCK

TITLE: DS33M30M31M33EE01A0 T3E3 LIU I/F. P.2,9,20-22	DATE: 04/15/2007
ENGINEER: STEVE SCULLY	PAGE: 8/11(BLOCK) 8/34(TOTAL)

BLOCK NAME: _rc_top_dn_. PARENT BLOCK: _rc_top_dn_\

Downloaded from: http://www.datasheetcatalog.com/

SIGNALS FORSIGNALS FOR HIERARCHY INTERFACE

BEGIN CPLD HIERARCHY BLOCK

TITLE: DS33M33DK01A0 OVERHEAD. P.2,10,23-24	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 23/26(TOTAL)

BLOCK NAME: overheadcpld_dn_ PARENT BLOCK: _rc_top_dn_\

V3_3 GND V3_3

DS10 DS11 DS12 DS13 RED_GREEN

RP01 330

ADDR<3..0> 11B5^ IN

CPLD_CS 11B5^ IN
RD 11B5^ IN
WR 11B5^ IN

J02 CONN_16P

BANK 7

PL2A/VREF2_7	2	
PL2B/VREF1_7	3	
PL7A	4	
PL7B	5	
PL8A	6	
PL8B	7	
PL9A/PCLKT7_0	8	PLL INPUT
PL9B/PCLKC7_0	9	

BANK 6

PL11A/LLM0_PLLT_IN_A	20	PLL INPUT
PL11B/LLM0_PLLC_IN_A	21	
PL12A/LLM0_PLLT_FB_A	22	
PL12B/LLM0_PLLC_FB_A	23	
PL13A	25	
PL13B	26	
PL14A	27	
PL14B	29	
PL15A/LDQS15	30	
PL15B	31	
PL16A	32	
PL16B	33	
PL18A/VREF1_6	34	
PL18B/VREF2_6	35	

BANK 5

PB10A	39	
PB10B	40	
PB11A	41	
PB11B	42	
PB13B	43	
PB14A/BDQS14	45	
PB14B	46	11C7^ IN CPLD_OHCLK
PB15A	47	11C7^ IN CPLD_OH1
PB15B	48	11C5^ OUT CPLD_TAOH
PB16A/VREF2_5	49	11C5^ OUT CPLD_TAOHEN
PB16B/VREF1_5	50	11B7^ IN CPLD_TAOHSOF
PB17A/PCLKT5_0	51	PLL INPUT
PB17B/PCLKC5_0	53	
PB18A/WRITE*	56	11B7^ IN CPLD_TAOHVLD
PB18B/CS1*	57	11C7^ IN CPLD_RDOH
PB19A/VREF1_4	58	11C7^ IN CPLD_RDOHSOF
PB19B/CS*	59	
PB20A/VREF2_4	60	
PB20B/D0/SPID7	61	11B7^ IN CPLD_RDOHVLD
PB21A/D2/SPID5	62	11C5^ OUT CPLD_ATOH
PB21B/D1/SPID6	64	11C5^ OUT CPLD_ATOHEN
PB22A/BDQS22	65	11C5^ IN CPLD_ATOHSOF
PB22B/D3/SPID4	66	11C5^ IN CPLD_ATOHCLK
PB23A	67	11C7^ IN CPLD_DTOH
PB23B/D4/SPID3	68	11C7^ IN CPLD_DTOHSOF
PB24B/D5/SPID2	69	11C7^ IN CPLD_DTOHCLK
PB25B/D6/SPID1	70	

BANK 4

PR18A/VREF1_3	74	
PR16B	75	
PR16A	76	
PR15B	77	
PR15A/RDQS15	78	
PR14B/RLM0_PLLC_FB_A	79	PLL INPUT
PR14A/RLM0_PLLT_FB_A	81	
PR13B/RLM0_PLLC_IN_A	82	
PR13A/RLM0_PLLT_IN_A	83	

BANK 3

PR12A/DOUT/CSO*	86	
PR12B/DI/CSSPI*	85	MEM_CS 24B8
PR11B/BUSY/SISPI	87	MEM_SI 24C8
PR11A/D7/SPID0	88	MEM_SO 24C8

BANK 2

PR9B/PCLKC2_0	100	PLL INPUT
PR9A/PCLKT2_0	101	
PR8B	102	
PR8A	103	
PR7B	104	
PR7A	105	
PR2B/VREF1_2	106	
PR2A/VREF2_2	107	

RB04 0.0 MEM_SCK

MEM_SCK MUST BE AT PIN77 FOR TQFP144

U01 LFEC_T144_U I/O PORT 97_IO

BANK 1

PT22A/TDQS22	115	
PT22B	114	
PT23A	113	
PT25A	112	
PT25B	111	
PT20A	120	9
PT20B	119	11
PT21A	118	13
PT21B	116	15
PT18A	124	1
PT18B	123	3
PT19A/VREF1_1	122	5
PT19B/VREF2_1	121	7

BANK 0

PT17A/PCLKT0_0	129	PLL INPUT
PT17B/PCLKC0_0	127	
PT16A/VREF2_0	131	M33_GPIOA3
PT16B/VREF1_0	130	M33_GPIOB3
PT15A	133	M33_GPIOA2
PT15B	132	M33_GPIOB2
PT14A/TDQS14	135	M33_GPIOA1
PT14B	134	M33_GPIOB1
PT13A	138	
PT13B	137	
PT12A	140	CP_DUT_CLKB 23A3 10B7^
PT12B	139	CP_DUT_CLKC 23A3 10B7^
PT10A	142	CP_DUT_CLADCLK 23A3 10B7^
PT10B	141	CP_DUT_CLKA 23A3 10B7^

11B5^ IN ADDR<3..0>

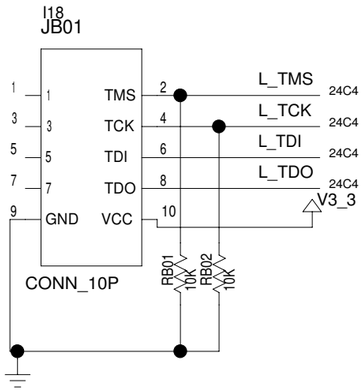
11B5^ IN WR
11B5^ IN RD
IN CPLD_CS

DAT<7..0> 0 1 2 3 4 5 6 7 IO 10B5^

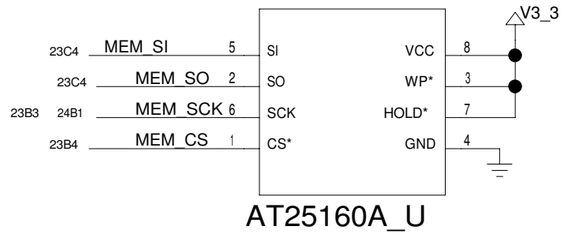
11B7^ 49D7 IN CP_DUT_CLADCLK
11B7^ 49D7 IN CP_DUT_CLKA
11B7^ 49D7 IN CP_DUT_CLKB
11B7^ 49D7 IN CP_DUT_CLKC

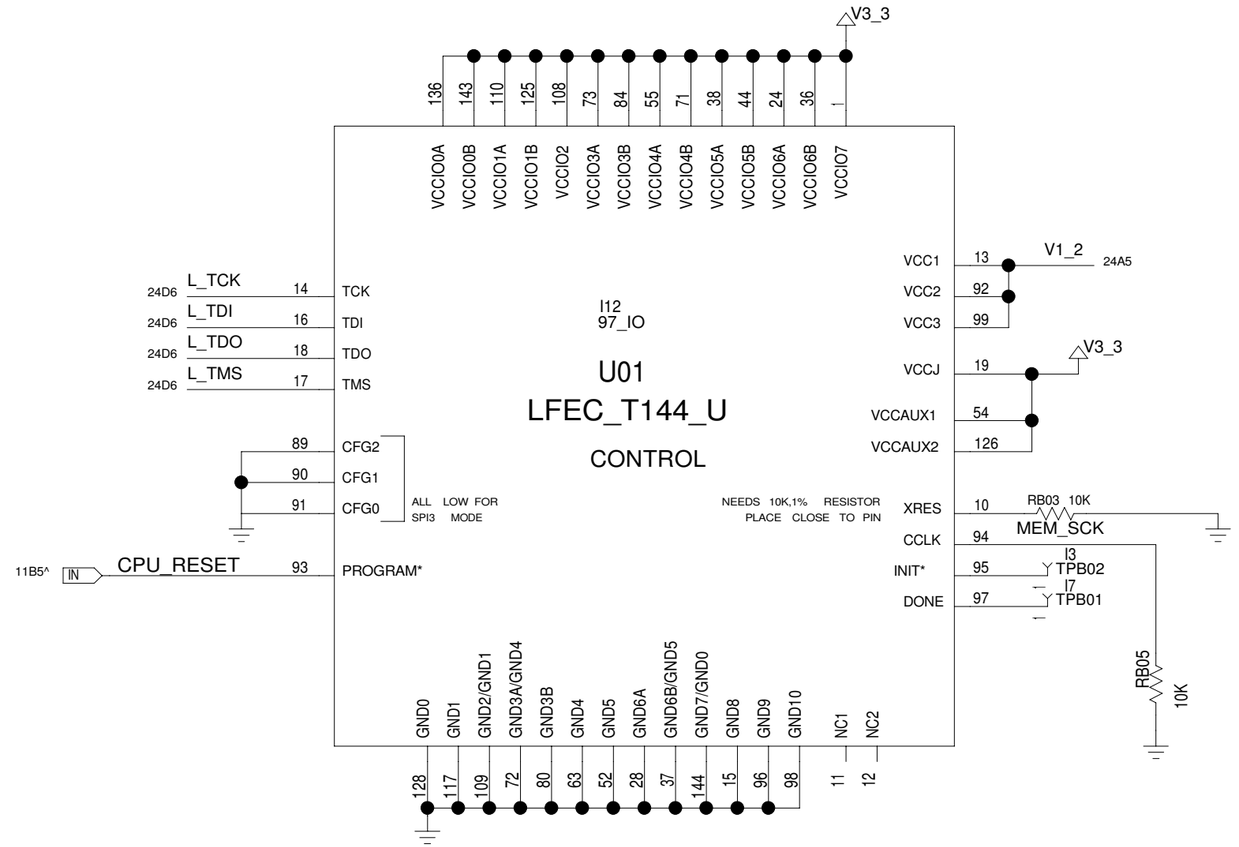
IO M33_GPIOA1
IO M33_GPIOB1
IO M33_GPIOA2
IO M33_GPIOB2
IO M33_GPIOA3
IO M33_GPIOB3

Downloaded from: http://www.datasheetcatalog.com/



I27
2.7V





END CPLD HIERARCHY BLOCK

TITLE: DS33M33DK01A0 OVERHEAD. P.2,10,23-24	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 24/26(TOTAL)

BLOCK NAME: overheadcpld_dn_. PARENT BLOCK: _rc_top_dn_\

Downloaded from: http://www.datasheetcatalog.com/

PLACE 9.76K RES CLOSE TO BG_REF

RESET_B — RB16 9.76K — BG_REF

V3_3 V1_8 V2_5 V1_8

U04

DP83865_U

33	RESET*	
102	BG_REF	
34	VDD_SEL_STRAP	
90	IO_VDD<1..12>	
92	CORE_VDD<1..8>	
96	2V5_AVDD<1..2>	
123	1V8_AVDD1_<1..5>	
98	1V8_AVDD2	
100	1V8_AVDD3	
32	TRST*	
31	TDI	
28	TDO	
27	TMS	
24	TCK	
40	CRS/RGMII_SEL1	
39	COL	
60	TX_CLK/RGMII_SEL0	
76	TXD<0>/TX0	
75	TXD<1>/TX1	
72	TXD<2>/TX2	
71	TXD<3>/TX3	
68	TXD<4>	
67	TXD<5>	
66	TXD<6>	
65	TXD<7>	
62	TX_EN/TXEN_ER	
79	GTX_CLK/TCK	
61	TX_ER	
57	RX_CLK	
56	RXD<0>/RX0	
55	RXD<1>/RX1	
52	RXD<2>/RX2	
51	RXD<3>/RX3	
50	RXD<4>	
47	RXD<5>	
46	RXD<6>	
45	RXD<7>	
41	RX_ER/RXDV_ER	
44	RX_DV/RCK	
81	MDC	
80	MDIO	
3	INTERRUPT*	
108	MDIA_P	
109	MDIA_N	
114	MDIB_P	
115	MDIB_N	
120	MDIC_P	
121	MDIC_N	
126	MDID_P	
127	MDID_N	
86	CLK_IN	
87	CLK_OUT	
85	CLK_TO_MAC	
1	NON_IEEE_STRAP	
6	MAN_MDIX_STRAP/TX_TCLK	
7	ACTIVITY_LED/SPEED0_STRAP	
8	LINK10_LED/SPEED1_STRAP	
9	LINK100_LED/DUPLEX_STRAP	
10	LINK1000_LED/AN_EN_STRAP	
13	DUPLEX_LED/PHYADDR<0>_STRAP	
14	PHYADDR<1>_STRAP	
17	PHYADDR<2>_STRAP	
18	PHYADDR<3>_STRAP	
95	PHYADDR<4>_STRAP	
94	MULTI_EN_STRAP/TX_TRIGGER	
89	MDIX_EN_STRAP	
88	MAC_CLK_EN_STRAP/TX_SYN_CLK	
128	VSS<1..35>	

OUTPUT

COL	PIN39
CRS	PIN40
RXER	PIN41
RXDV	PIN44
RXD[0:7]	[PIN56:PIN45]
RXCLK	PIN57
TXCLK	PIN60
CLKTOMAC	PIN85
CLKOUT	PIN87

INPUT

TXERR	PIN61
TXEN	PIN62
TXD[0:7]	[PIN76:PIN65]
GTXCLK	PIN79
MDC	PIN81
CLKIN	PIN86

RB11 2.0K — RP02 30

TXD<7..0> (6C4^ 25C1)

RXD<7..0> (6D4^ 25B1)

RP07 30 — RP06 30

RPB26 0603_2PCT_50 — RPB24 0603_2PCT_50

PLACE MDI RESISTORS CLOSE TO PHY

MAINTAIN 50OHM STIPLINE TO V2_5PHY

RPB30 1K

RB07 330 — DS18 GREEN — RB06 2.0K

RPB20 1K

RPB25 30 — RP12 30 — RP05 30 — RPB03

PHYOSC25M (IN 25B3 6B4^)

LAN_CLK (6B4^ IO)

MDC (6B4^ 25C3 IO)

MDIO (6B4^ 26C6 25C3 IO)

RESET_B (6B4^ 26C6 25D6 IO)

PHY_INT (6B4^ 26C6 25C3 IO)

SPARE<4..1> (IO)

GMII_CLKFROM_MAC (IO 25B7 6C4^)

TX_ER (IO 25A7 25B7 6C4^)

CLKTOMAC_TESTPNT (IO 25B1)

CLKTOMAC (IO 25B1 6C4^)

TXD<7..0> (IO 25B7 6C4^)

TX_EN (IO 25B7 6C4^)

TX_CLK (IO 25B1 6C4^)

RX_CLK (IO 25B1 6D4^)

COL_DET (IO 25B1 6D4^)

RX_ERR (IO 25A1 6C4^)

RX_CRS (IO 25A1 6D4^)

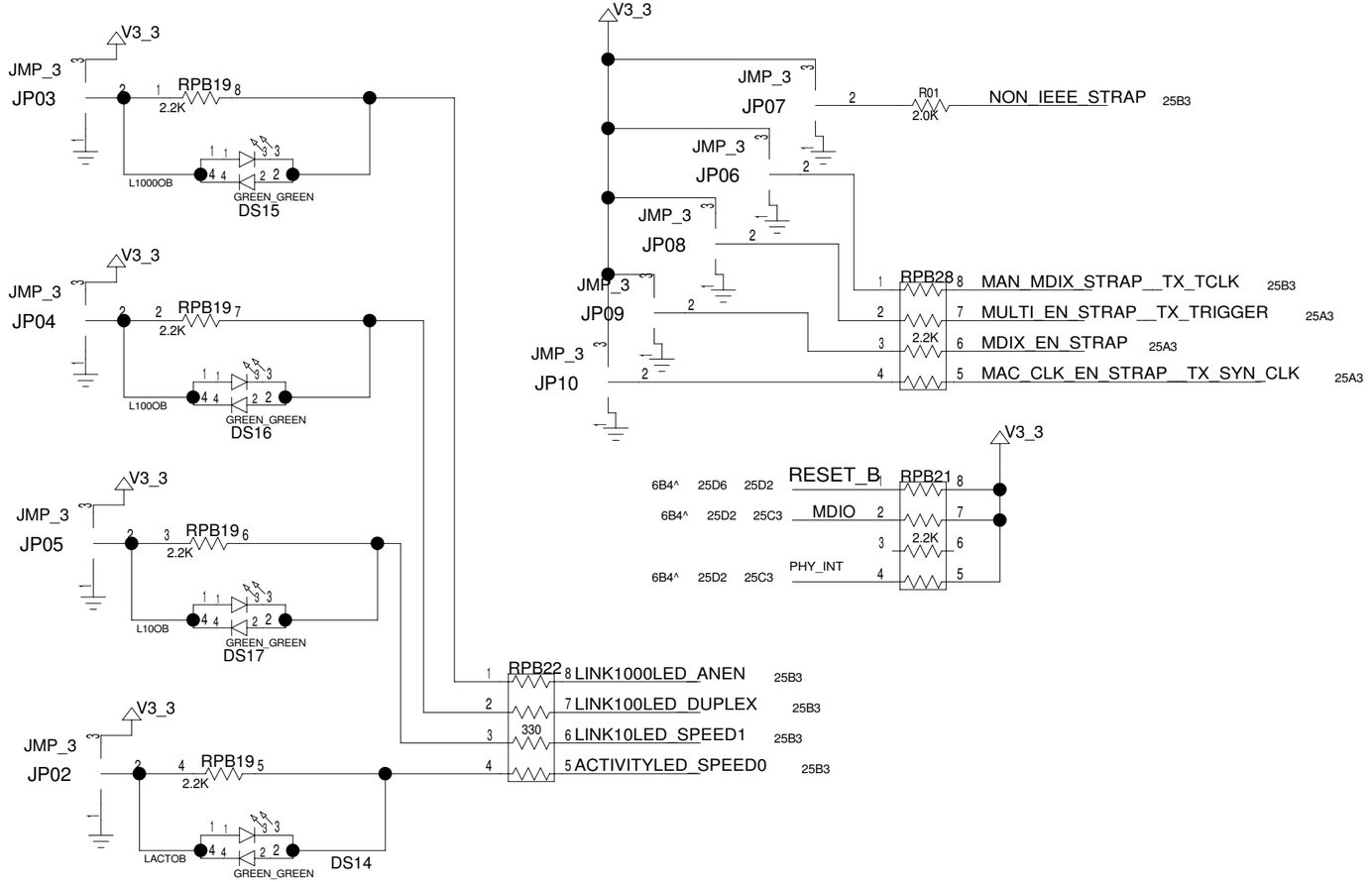
RXDV (IO 25A1 6D4^)

RXD<7..0> (IO 25A8 6D4^)

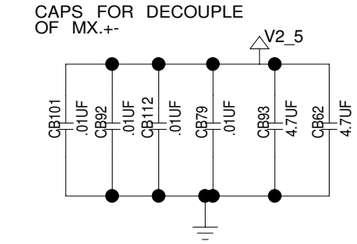
BEGIN PHY HIERARCHY BLOCK

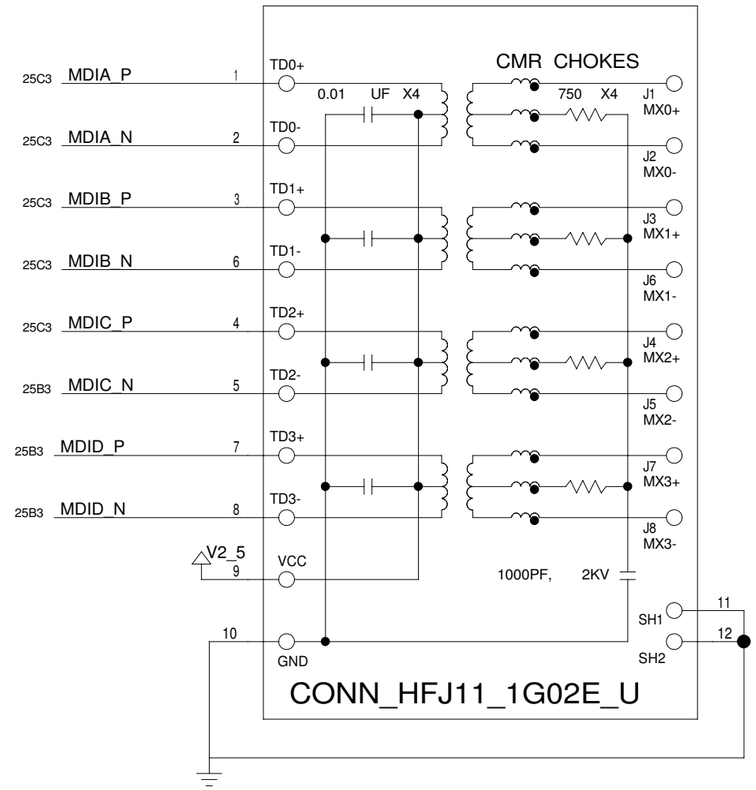
TITLE: DS33M33DK01A0 ETHERNET. P.5-6,19,25-26	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 1/2(BLOCK) 25/26(TOTAL)

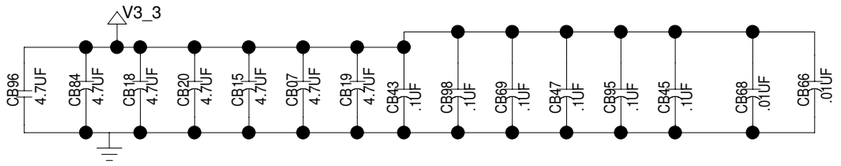
Downloaded from: http://www.datasheetcatalog.com/

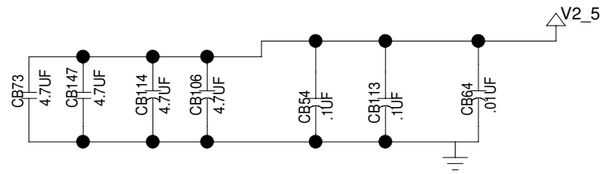


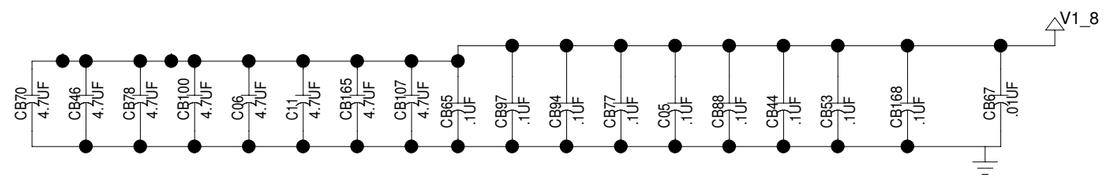
CHECK THAT 2.2K RES USE THE SAME RPACK
STRAP OPTIONS HERE DO NOT FOLLOW DATASHEET











END PHY HIERARCHY BLOCK

TITLE: DS33M33DK01A0 ETHERNET. P.5-6,19,25-26	DATE: 10/03/2007
ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 26/26(TOTAL)

BLOCK NAME: _phy_dp83865bvh_dn. PARENT BLOCK: _rc_top_dn_\