



U74AHC2G126

CMOS IC

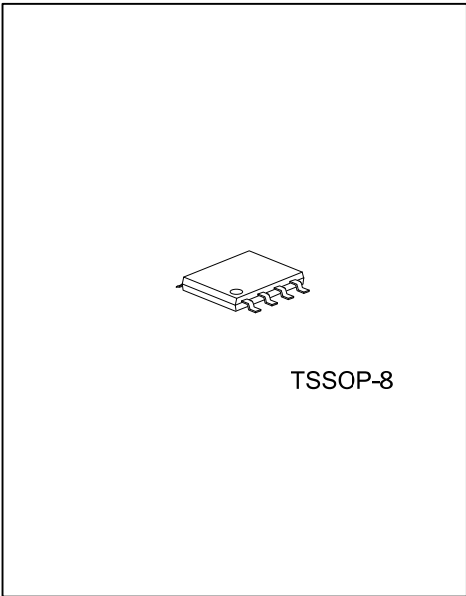
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

DESCRIPTION

The **U74AHC2G126** consists of two bus buffers with 3-state output controlled by enable input (nOE), when nOE is low, the output is disable.

FEATURES

- * Wide supply voltage range from 2.0V to 5.5V
- * Low static power consumption; $I_{CC}=2\mu A$ (Max.)
- * $\pm 8mA$ output driver at 5V

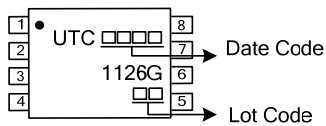


ORDERING INFORMATION

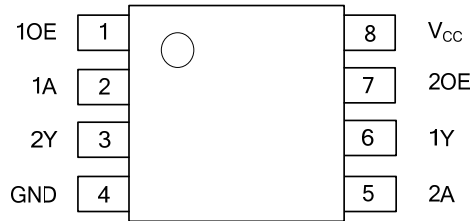
Ordering Number	Package	Packing
U74AHC2G126G-P08-R	TSSOP-8	Tape Reel

U74AHC2G126G-P08-R		
(1) Packing Type	(1) R: Tape Reel	
(2) Package Type	(2) P08: TSSOP-8	
(3) Green Package	(3) G: Halogen Free and Lead Free	

MARKING



■ PIN CONFIGURATION

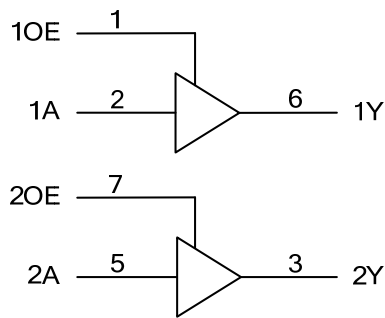


■ FUNCTION TABLE

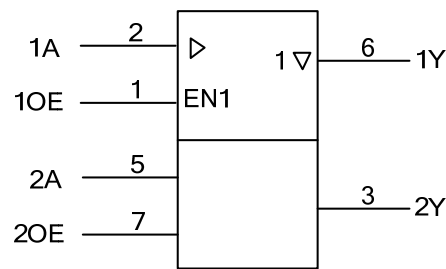
INPUT(OE)	INPUT(A)	OUTPUT(Y)
H	L	L
H	H	H
L	X	Z

Note: H: High voltage level; L: Low voltage level; Z: High impedance; X: Don't care

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC Logic symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ +7.0	V
Output Voltage	V_{OUT}		-0.5 ~ $V_{CC} + 0.5$	V
Continuous V_{CC} or GND Current	I_{CC}		50	mA
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	± 25	mA
Input Clamp Current	I_{IK}	$V_{IN} < 0V$	-20	mA
Output Clamp Current	I_{OK}	$V_{OUT} > V_{CC}$ or $V_{OUT} < 0V$	± 20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	$^{\circ}C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2.0		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Operating Temperature (Note)	T_A		-40		125	$^{\circ}C$
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=3.3V \pm 0.3V$			100	ns/V
		$V_{CC}=5V \pm 0.5V$			20	ns/V

Note: This condition is only determined from design. It can't be 100% tested in mass production.

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5			V	
		$V_{CC}=3.0V$	2.1			V	
		$V_{CC}=5.5V$	3.85			V	
Low-level Input Voltage	V_{IL}	$V_{CC}=2.0V$			0.5	V	
		$V_{CC}=3.0V$			0.9	V	
		$V_{CC}=5.5V$			1.65	V	
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V$	1.9	2		V	
		$V_{CC}=3.0V$			2.9	3	V
		$V_{CC}=4.5V$			4.4	4.5	V
		$V_{CC}=3.0V, I_{OH}=-4mA$	2.58		V		
		$V_{CC}=4.5V, I_{OH}=-8mA$	3.94		V		
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V$			0.1	V	
		$V_{CC}=3.0V$			0.1	V	
		$V_{CC}=4.5V$			0.1	V	
		$V_{CC}=3.0V, I_{OH}=-4mA$		0.36	V		
		$V_{CC}=4.5V, I_{OH}=-8mA$		0.36	V		
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND			± 0.1	μA	
3-state Output OFF-state Current	I_{OZ}	$V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=V_{CC}$ or GND, $V_{CC}=5.5V$			± 0.25	μA	
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0A$			2	μA	
Input Capacitance	C_I	$V_{CC}=5.0V, V_{IN}=V_{CC}$ or GND		2		pF	

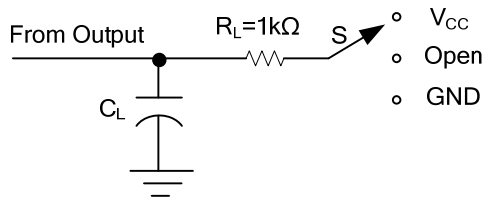
■ SWITCHING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t _{PD}	C _L =15pF	V _{CC} =3.3±0.3V		9.5	ns
			V _{CC} =5±0.5V		6.5	ns
		C _L =50pF	V _{CC} =3.3±0.3V		13	ns
			V _{CC} =5±0.5V		8.5	ns
Propagation delay from input (OE) to output(Y)	t _{en}	C _L =15pF	V _{CC} =3.3±0.3V		9.5	ns
			V _{CC} =5±0.5V		6	ns
		C _L =50pF	V _{CC} =3.3±0.3V		13	ns
			V _{CC} =5±0.5V		8	ns
Propagation delay from input (OE) to output(Y)	t _{dis}	C _L =15pF	V _{CC} =3.3±0.3V		11.5	ns
			V _{CC} =5±0.5V		8	ns
		C _L =50pF	V _{CC} =3.3±0.3V		15	ns
			V _{CC} =5±0.5V		10	ns

■ OPERATING CHARACTERISTICS (f=10MHz, T_A =25°C , unless otherwise specified)

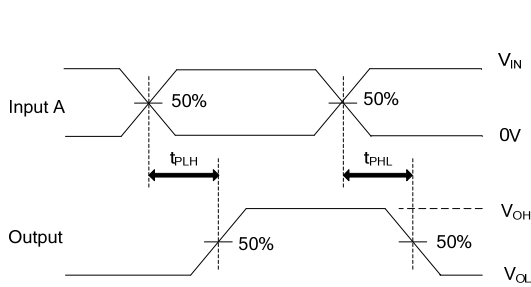
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C _{PD}	V _{CC} =5V, No load.		14		pF

■ TEST CIRCUIT AND WAVEFORMS

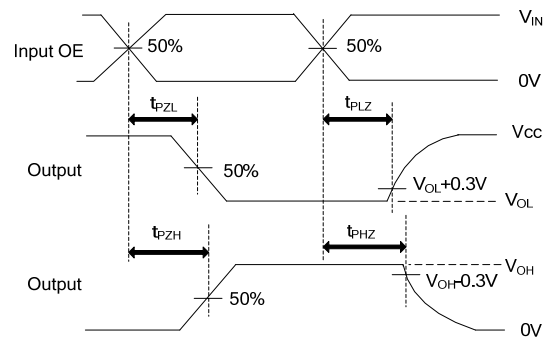


TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\Omega$.

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