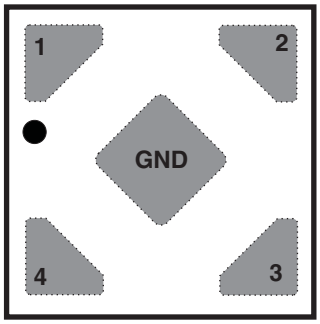
ESDAVLC5-4BX4

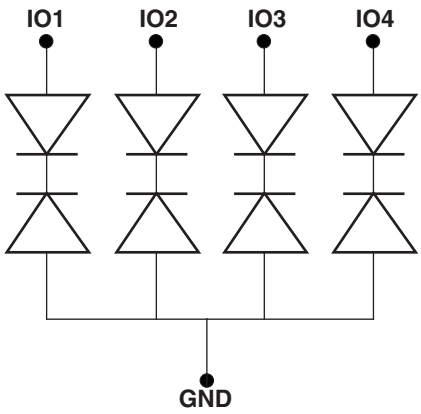
4-line bidirectional Transil™, transient surge voltage suppressor for ESD protection

Datasheet – production data



4-lead micro package

Figure 1. Functional diagram



Features

- 4 bidirectional Transil diodes
- Breakdown voltage V_{BR} = 5.5 V min.
- Low leakage current: < 50 nA
- Very small PCB area: 0.64 mm^2
- Lead-free and RoHS compliant

Complies with the following standards

- IEC 61000-4-2 level 4:
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Mobile phones
- Portable multimedia devices and accessories
- Computers, tablets and peripherals
- Set top boxes
- Audio equipment

Description

The ESDAVLC5-4BX4 is monolithic array designed to protect up to 4 bidirectional lines against ESD transients.

The device is ideal for applications where both reduced printed circuit board space and high ESD protection level are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP} (1)	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	16 16	kV
I_{PP}	Peak pulse current (8/20 µs)		2	A
P_{PP}	Peak pulse power (8/20 µs)		30	W
T_j	Operating temperature range		-30 to +85	°C
T_{stg}	Storage temperature range		- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

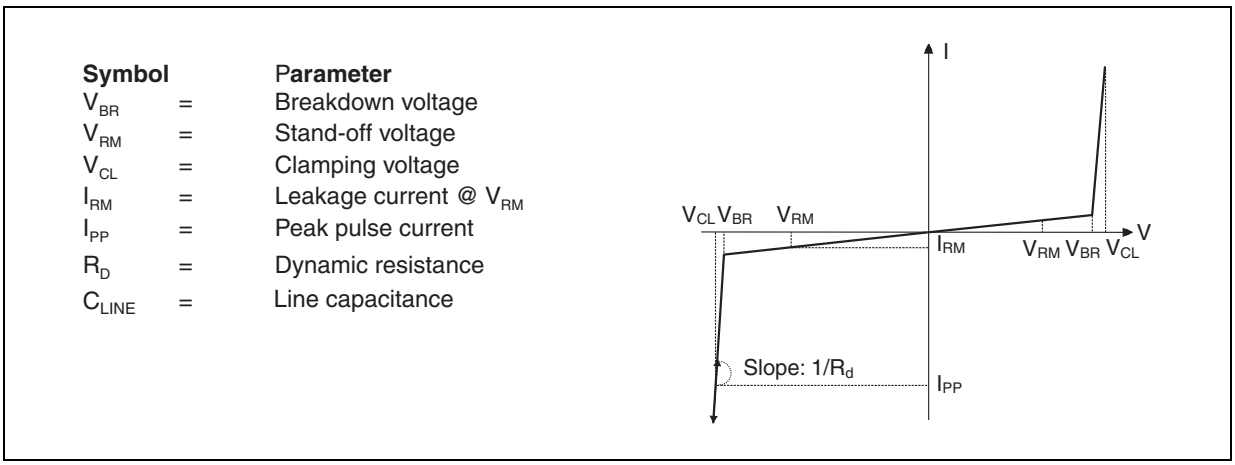


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{BR}	Breakdown voltage	I_R = 1 mA	5.5			V
I_{RM}	Leakage current	V_{RM} = 3 V			50	nA
V_{CL}	Clamping voltage	I_{PP} = 1 A, 8/20 µs			18	V
C_{line}	Line capacitance, I/O to GND	V_R = 0 V, F_{osc} = 1 MHz, V_{osc} = 30 mV			10	pF
R_d	Dynamic resistance, pulse width 100 ns	I/O to GND		0.53		Ω
		GND to I/O		0.37		

Figure 3. Leakage current versus junction temperature (typical values)

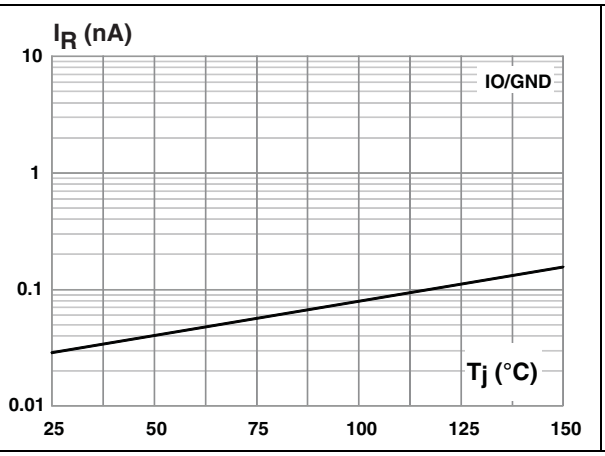


Figure 4. Junction capacitance versus reverse applied voltage (typical values)

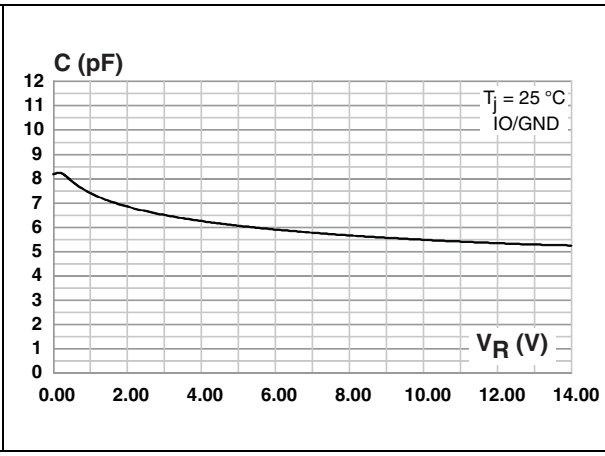


Figure 5. ESD response to IEC 61000-4-2 (typical values, +8 kV contact discharge)

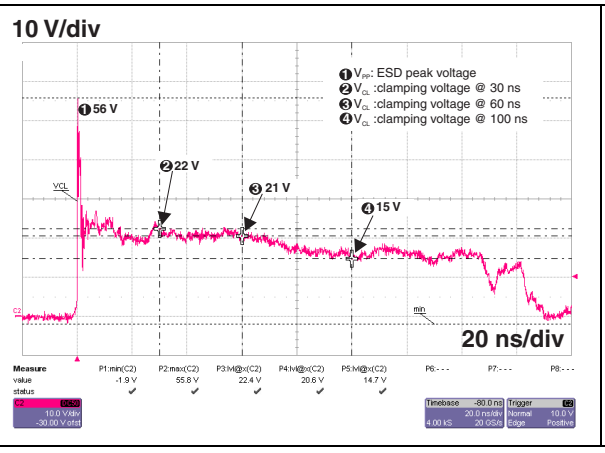


Figure 6. ESD response to IEC 61000-4-2 (typical values, -8 kV contact discharge)

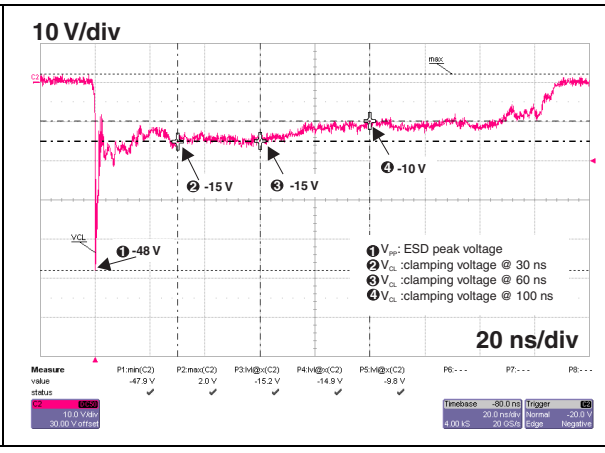


Figure 7. S21 attenuation measurement

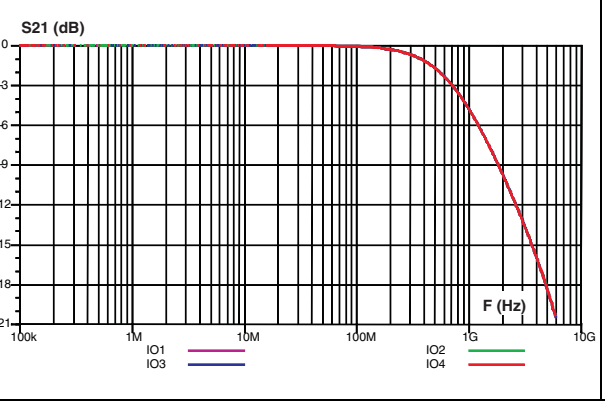
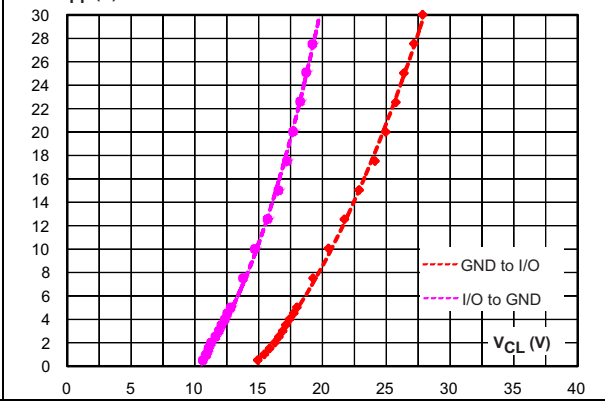


Figure 8. TLP measurement



2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 9. Micro package dimensions

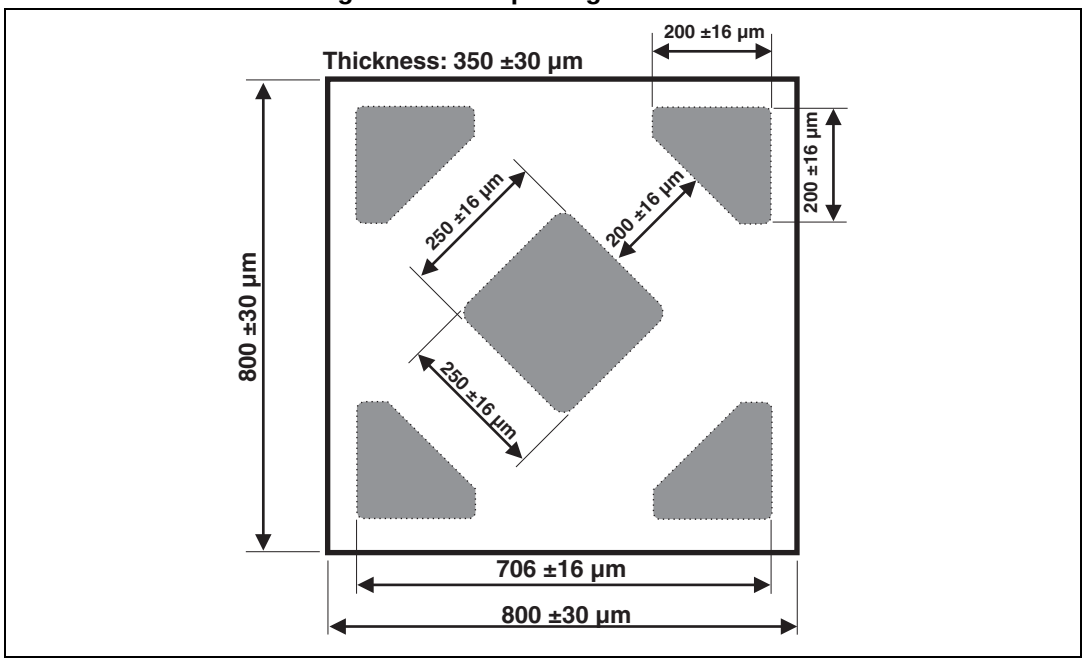
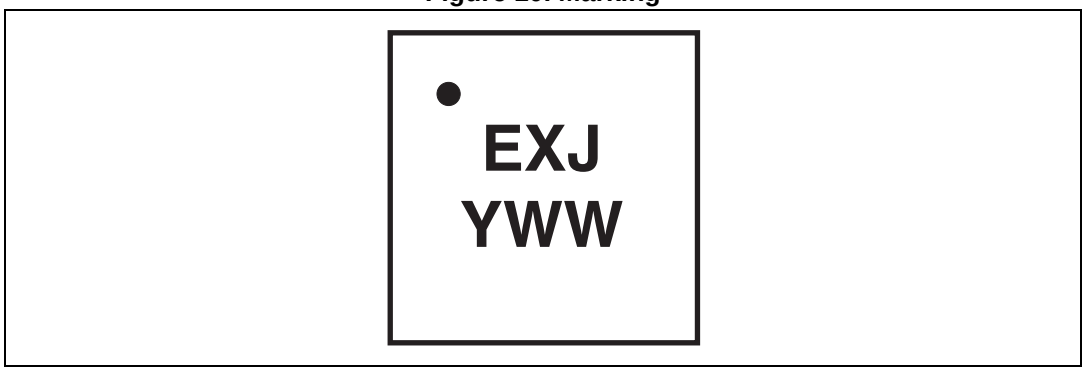
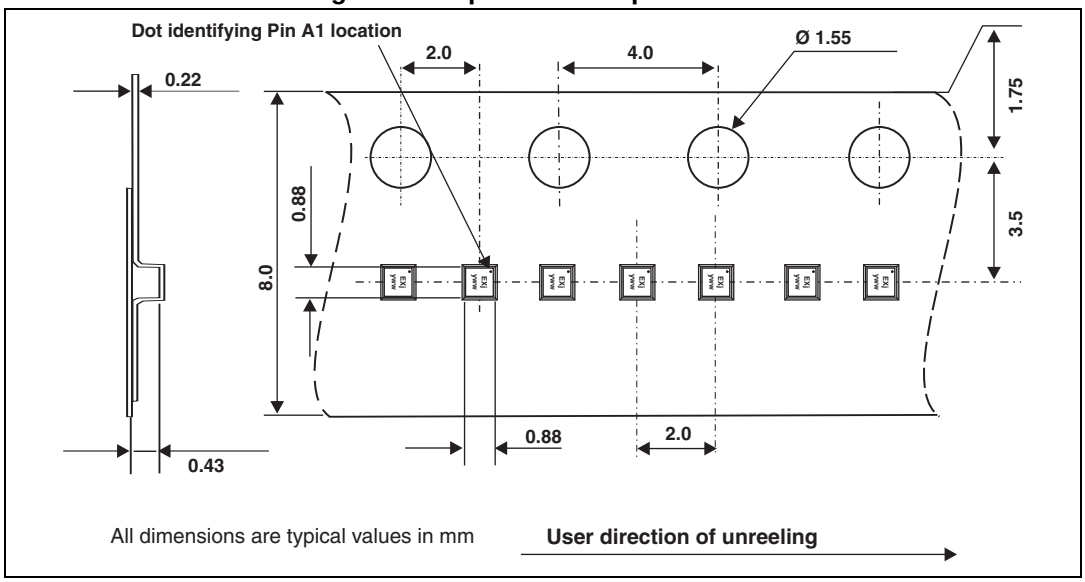


Figure 10. Marking



Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 11. Tape and reel specification



3 Recommendation on PCB assembly

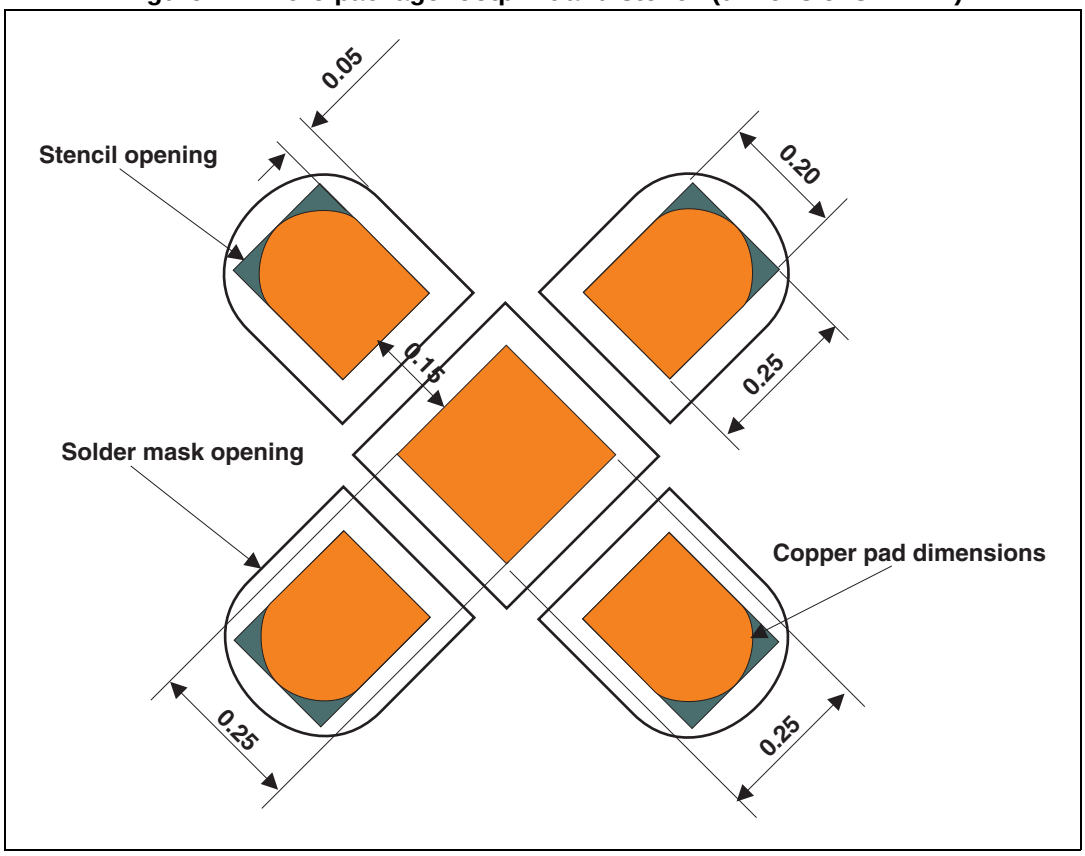
3.1 PCB design recommendations

- PCB pad design: Non solder mask defined
- PCB pad size: see *Figure 12*.
- Solder mask opening: 50 µm between the edge of the pad and the edge of the solder mask

3.2 Stencil recommendations

- Stencil aperture: see *Figure 12*.
- Stencil thickness: 75 µm

Figure 12. Micro package footprint and stencil (dimensions in mm)



3.3 Solder paste recommendations

Near eutectic 95.8% Sn, 3.5% Ag, 0.7% Cu solder paste, Type 4.

4 Ordering information

Figure 13. Ordering information scheme

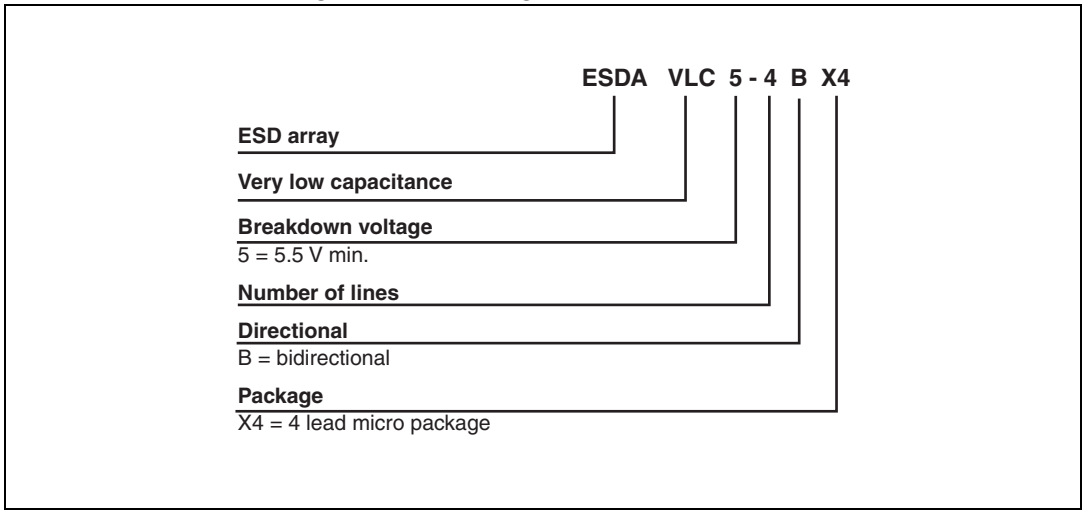


Table 3. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDAVLC5-4BX4	EX(1)	0.504 mg	10 000	Tape and reel

1. The marking codes can be rotated by multiples of 90° to differentiate assembly location

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
18-Sep-2012	1	First issue
05-Jun-2014	2	Updated values for dynamic resistance in *Table 2* and added *Figure 8*.

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