DDR II SDRAM

8M x 16 Bit x 4 Banks DDR II SDRAM

Features

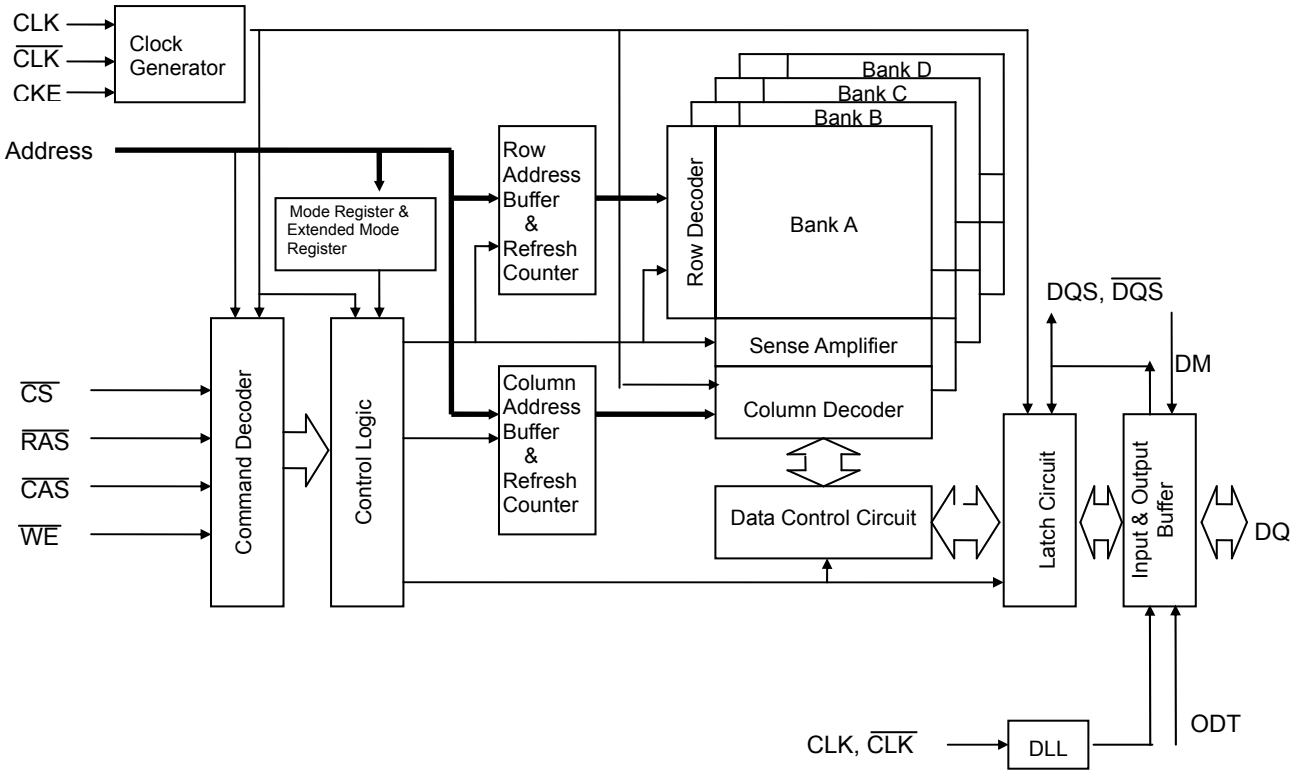
- JEDEC Standard
- V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.8V ± 0.1V
- Internal pipelined double-data-rate architecture; two data access per clock cycle
- Bi-directional differential data strobe (DQS, $\overline{DQS}$); $\overline{DQS}$ can be disabled for single-ended data strobe operation.
- On-chip DLL
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transition with CLK transition
- Quad bank operation
- CAS Latency : 3, 4, 5, 6, 7
- Additive Latency: 0, 1, 2, 3, 4, 5, 6
- Burst Type : Sequential and Interleave
- Burst Length : 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock(CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- Off-Chip-Driver (OCD) impedance adjustment
- On-Die-Termination for better signal quality
- Special function support
  - 50/ 75/ 150 ohm ODT
  - High Temperature Self refresh rate enable
  - Duty Cycle Corrector
  - Partial Array Self Refresh (PASR)
- Auto & Self refresh
- Refresh cycle :
  - 8192 cycles/64ms (7.8μ s refresh interval) at 0 ℃ ≦ T_C ≦ +85 ℃
  - 8192 cycles/32ms (3.9μ s refresh interval) at +85 ℃ < T_C ≦ +95 ℃
- SSTL_18 interface
- If t_{CK} < 1.875ns, the device can not support Write with Auto Precharge function.

Ordering Information:

Product ID	Max Freq.	VDD	Data Rate (CL-tRCD-tRP)	Package	Comments
M14D5121632A -1.3BG2K *	750MHz	1.8V	DDR2-1500 (7-10-10)	84 ball BGA A(max) = 1.2mm	Pb-free
M14D5121632A -1.5BG2K	667MHz	1.8V	DDR2-1333 (7-9-9)		
M14D5121632A -1.8BG2K	533MHz	1.8V	DDR2-1066 (7-7-7)		
M14D5121632A -2.5BG2K	400MHz	1.8V	DDR2-800 (5-5-5)		
M14D5121632A -1.8BBG2K	533MHz	1.8V	DDR2-1066 (7-7-7)	84 ball BGA A(max) = 1.0mm	
M14D5121632A -2.5BBG2K	400MHz	1.8V	DDR2-800 (5-5-5)		

Note: * All specification for speed grade -1.3 is preliminary data.

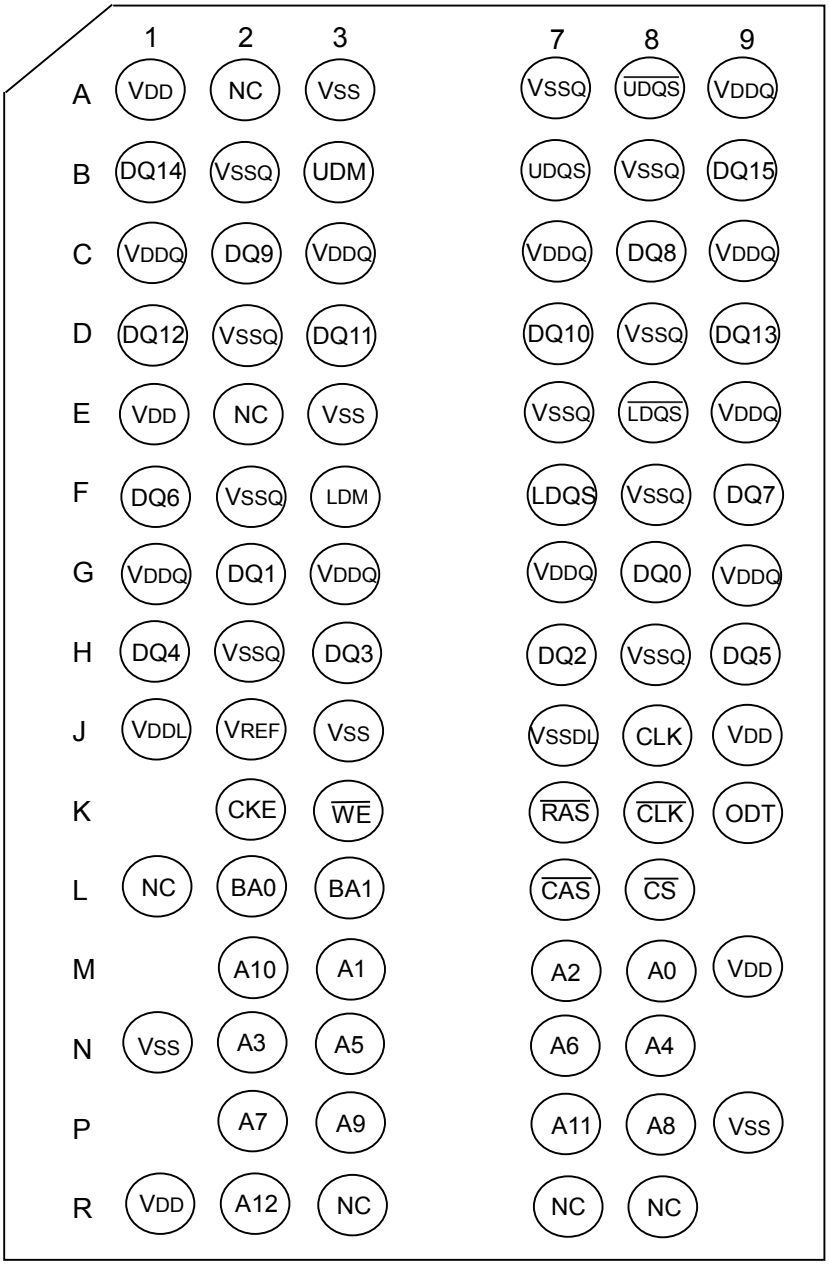
Functional Block Diagram



Ball Configuration (Top View)

(BGA84, 8mmX12.5mmX1.2mm Body, 0.8mm Ball Pitch)

(BGA84, 8mmX12.5mmX1.0mm Body, 0.8mm Ball Pitch)



Pin Description

Pin Name	Function	Pin Name	Function
A0~A12, BA0,BA1	Address inputs - Row address A0~A12 - Column address A0~A9 A10/AP : Auto Precharge BA0, BA1 : Bank selects (4 Banks)	DM (LDM, UDM)	DM is an input mask signal for write data. LDM is DM for DQ0~DQ7 and UDM is DM for DQ8~DQ15.
DQ0~DQ15	Data-in/Data-out	CLK, $\overline{CLK}$	Differential clock input
$\overline{RAS}$	Command input	CKE	Clock enable
$\overline{CAS}$	Command input	$\overline{CS}$	Chip select
$\overline{WE}$	Command input	V_{DDQ}	Supply Voltage for DQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power	V_{REF}	Reference Voltage
DQS, $\overline{DQS}$ (LDQS, $\overline{LDQS}$ UDQS, $\overline{UDQS}$)	Bi-directional differential Data Strobe. LDQS and $\overline{LDQS}$ are DQS for DQ0~DQ7; UDQS and $\overline{LDQS}$ are DQS for DQ8~DQ15.	V_{DDL}	Supply Voltage for DLL
ODT	On-Die-Termination. ODT is only applied to DQ0~DQ15, DM, DQS and $\overline{DQS}$.	V_{SSDL}	Ground for DLL
NC	No connection		

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.3	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-1.0 ~ 2.3	V
Voltage on V_{DDL} supply relative to V_{SS}	V_{DDL}	-0.5 ~ 2.3	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.3	V
Storage temperature	T_{STG}	-55 ~ +100	°C (**Note ***)

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note *: Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Operation Temperature Condition

Parameter	Symbol	Value	Unit
Operation temperature	T_C	0 ~ +95	°C

Note: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.

2. Supporting 0 to +85℃ with full AC and DC specifications.
Supporting 0 to + 85℃ and being able to extend to + 95 ℃ with doubling auto-refresh commands in frequency to a 32ms period (t_{REFI} = 3.9μ s) and higher temperature Self-Refresh entry via A7 "1" on EMRS(2).

DC Operation Condition & Specifications

DC Operation Condition

(Recommended DC operating conditions)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{DD}	1.7	1.8	1.9	V	4,9
Supply voltage for DLL	V_{DDL}	1.7	1.8	1.9	V	4,9
Supply voltage for output	V_{DDQ}	1.7	1.8	1.9	V	4,9
Input reference voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	1,2,9
Termination voltage (system)	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	3,9
Input logic high voltage	V_{IH} (DC)	V_{REF} + 0.125	-	V_{DDQ} + 0.3	V	
Input logic low voltage	V_{IL} (DC)	-0.3	-	V_{REF} - 0.125	V	

(All voltages referenced to VSS)

Parameter	Symbol	Value	Unit	Note
Minimum required output pull-up under AC test load	V_{OH}	V_{TT} + 0.603	V	8
Maximum required output pull-down under AC test load	V_{OL}	V_{TT} - 0.603	V	8
Input leakage current	$\|I_{LI}\|$	5	uA	5
Output leakage current	$\|I_{LO}\|$	5	uA	6
Output minimum source DC current (V_{DDQ}(min); V_{OUT} =1.42V)	I_{OH}	-13.4	mA	7, 8
Output minimum sink DC current (V_{DDQ}(min); V_{OUT} = 0.28V)	I_{OL}	+13.4	mA	7, 8

Note:

1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
2. Peak to peak AC noise on V_{REF} may not exceed ±2% V_{REF}(DC).
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. V_{DDQ} and V_{DDL} track V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.
5. Any input 0V ≤ V_{IN} ≤ V_{DD}; all other balls not under test = 0V.
6. 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT disabled.
7. The DC value of V_{REF} applied to the receiving device is expected to be set to V_{TT}.
8. After OCD calibration to 18Ω at T_C = 25℃, V_{DD} = V_{DDQ} = 1.8V
9. There is no specific device V_{DD} supply voltage requirement for SSTL_18 compliance. However, under all conditions V_{DDQ} must be less than or equal to V_{DD}.

DC Specifications

(IDD values are for the operation range of Voltage and Temperature)

Parameter	Symbol	Test Condition		Version				Unit
				-1.3	-1.5	-1.8	-2.5	
Operating Current (Active - Precharge)	IDD0	One bank; $t_{CK} = t_{CK}$ (IDD), $t_{RC} = t_{RC}$ (IDD), $t_{RAS} = t_{RAS}$ (IDD)min; CKE is High, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		130	100	80	75	mA
Operating Current (Active - Read - Precharge)	IDD1	One bank; I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK}$ (IDD), $t_{RC} = t_{RC}$ (IDD), $t_{RAS} = t_{RAS}$ (IDD)min, $t_{RCD} = t_{RCD}$ (IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		160	130	100	95	mA
Precharge Power-Down Standby Current	IDD2P	All banks idle; $t_{CK} = t_{CK}$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		18	15	12	12	mA
Precharge Quiet Standby Current	IDD2Q	All banks idle; $t_{CK} = t_{CK}$ (IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		80	60	40	40	mA
Idle Standby Current	IDD2N	All banks idle; $t_{CK} = t_{CK}$ (IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		65	55	45	45	mA
Active Power-down Standby Current	IDD3P	All banks open; $t_{CK} = t_{CK}$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus input are FLOATING	Fast PDN Exit MRS(12) = 0	55	45	35	35	mA
			Slow PDN Exit MRS(12) = 1	40	30	20	20	
Active Standby Current	IDD3N	All banks open; $t_{CK} = t_{CK}$ (IDD), $t_{RAS} = t_{RAS}$ (IDD)max, $t_{RP} = t_{RP}$ (IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		80	60	50	50	mA
Operation Current (Read)	IDD4R	All banks open, continuous burst Reads, I_{OUT} = 0mA; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK}$ (IDD), $t_{RAS} = t_{RAS}$ (IDD)max, $t_{RP} = t_{RP}$ (IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is the same as IDD4W;		200	180	160	140	mA
Operation Current (Write)	IDD4W	All banks open, continuous burst Writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK}$ (IDD), $t_{RAS} = t_{RAS}$ (IDD)max, $t_{RP} = t_{RP}$ (IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		190	170	150	130	mA

Parameter	Symbol	Test Condition	Version				Unit
			-1.3	-1.5	-1.8	-2.5	
Auto Refresh Current	IDD5	$t_{CK} = t_{CK}$ (IDD); Refresh command every t_{RFC} (IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	140	120	100	100	mA
Self Refresh Current	IDD6	Self Refresh Mode; CLK and $\overline{CLK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	8				mA
Operating Current (Bank interleaving)	IDD7	All bank interleaving Reads, I_{OUT} = 0mA; BL = 4, CL= CL (IDD), AL = t_{RCD} (IDD) – 1 × t_{CK} (IDD); $t_{CK} = t_{CK}$ (IDD), $t_{RC} = t_{RC}$ (IDD), $t_{RRD} = t_{RRD}$ (IDD), t_{RCD} = 1 × t_{CK} (IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during Deslects; Data pattern is the same as IDD4W;	280	230	210	200	mA

Note:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Input Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS and $\overline{DQS}$, IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD:
   LOW is defined as $V_{IN} \leq V_{IL}$ (AC) (max.).
   HIGH is defined as $V_{IN} \geq V_{IH}$ (AC) (min.).
   STABLE is defined as inputs stable at a HIGH or LOW level.
   FLOATING is defined as inputs at $V_{REF} = V_{DDQ}/2$
   SWITCHING is defined as:
   Address and control signal Inputs are changed between HIGH and LOW every other clock cycle (once per two clocks), and DQ (not including mask or strobe) signal inputs are changed between HIGH and LOW every other data transfer (once per clock).
6. When $T_C \geqq +85$ ℃, IDD6 must be derated by 80%.
   IDD6 will increase by this amount if $T_C \geqq +85$ ℃ and double refresh option is still enabled.
7. AC Timing for IDD test conditions
   For purposes of IDD testing, the following parameters are to be utilized.

Parameter	-1.3	-1.5	-1.8	-2.5	Unit
	DDR2-1500 (7-10-10)	DDR2-1333 (7-9-9)	DDR2-1066 (7-7-7)	DDR2-800 (5-5-5)	
CL (IDD)	7	7	7	5	t_{CK}
tRCD (IDD)	13.3	13.5	13.125	12.5	ns
tRC (IDD)	80	58.125	58.125	57.5	ns
tRRD (IDD)	12	10	10	10	ns
tCK (IDD)	1.333	1.5	1.875	2.5	ns
tRAS (IDD) min.	60	45	45	45	ns
tRAS (IDD) max.	70000				ns
tRP (IDD)	13.3	13.5	13.25	12.5	ns
tRFC (IDD)	150	130	105	105	ns

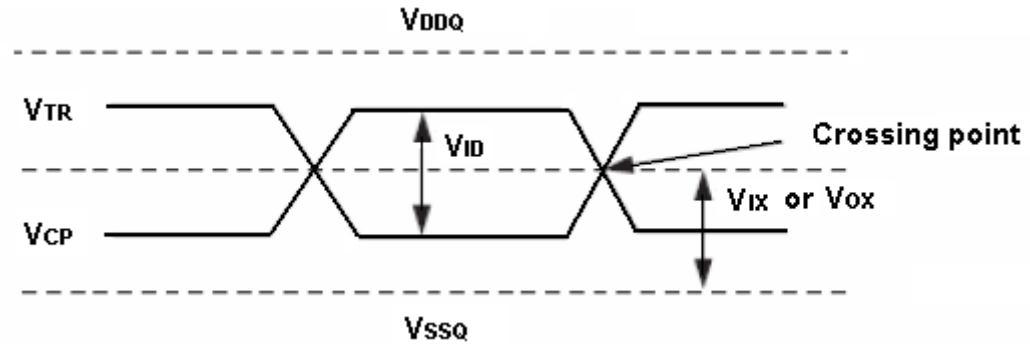
AC Operation Conditions & Timing Specification

AC Operation Conditions

Parameter	Symbol	-1.3/ 1.5/ 1.8/ 2.5		Unit	Note
		Min.	Max.		
Input High (Logic 1) Voltage	V_{IH}(AC)	V_{REF} + 0.2		V	
Input Low (Logic 0) Voltage	V_{IL}(AC)		V_{REF} - 0.2	V	
Input Differential Voltage	V_{ID}(AC)	0.5	V_{DDQ}+0.6	V	1
Input Crossing Point Voltage	V_{IX}(AC)	0.5 x V_{DDQ} - 0.175	0.5 x V_{DDQ} + 0.175	V	2
Output Crossing Point Voltage	V_{OX}(AC)	0.5 x V_{DDQ} - 0.125	0.5 x V_{DDQ} + 0.125	V	2

Note:

1. V_{ID}(AC) specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CLK,DQS) and V_{CP} is the complementary input signal (such as $\overline{CLK}$, $\overline{DQS}$). The minimum value is equal to V_{IH}(AC) – V_{IL}(AC).
2. The typical value of V_{IX} / V_{OX}(AC) is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{IX} / V_{OX}(AC) is expected to track variations in V_{DDQ}. V_{IX} / V_{OX}(AC) indicates the voltage at which differential input / output signals must cross.



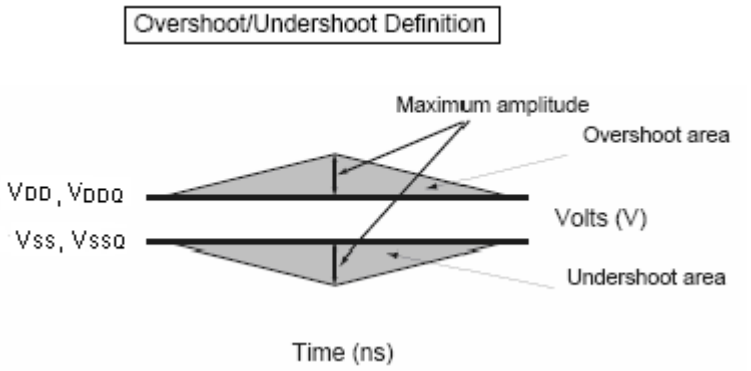
Input / Output Capacitance

Parameter	Symbol	Min.	Max.	Unit	Note
Input capacitance (A0~A12, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT)	C_{IN1}	2	5	pF	1
Input capacitance (CLK, $\overline{CLK}$)	C_{IN2}	2	5	pF	1
DQS, $\overline{DQS}$ & Data input/output capacitance	$C_{I/O}$	2	5	pF	2
Input capacitance (DM)	C_{IN3}	2	5	pF	2

Note: 1. Capacitance delta is 0.25 pF.
2. Capacitance delta is 0.5 pF.

AC Overshoot / Undershoot Specification

Parameter	Pin	Value		Unit
		-1.3 / 1.5 / 1.8	-2.5	
Maximum peak amplitude allowed for overshoot	Address, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, CLK, $\overline{CLK}$, DQ, DQS, $\overline{DQS}$, DM	0.5	0.5	V
Maximum peak amplitude allowed for undershoot	Address, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, CLK, $\overline{CLK}$, DQ, DQS, $\overline{DQS}$, DM	0.5	0.5	V
Maximum overshoot area above V_{DD}	Address, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT,	0.5	0.66	V-ns
	CLK, $\overline{CLK}$, DQ, DQS, $\overline{DQS}$, DM	0.19	0.23	V-ns
Maximum undershoot area below V_{SS}	Address, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT,	0.5	0.66	V-ns
	CLK, $\overline{CLK}$, DQ, DQS, $\overline{DQS}$, DM	0.19	0.23	V-ns

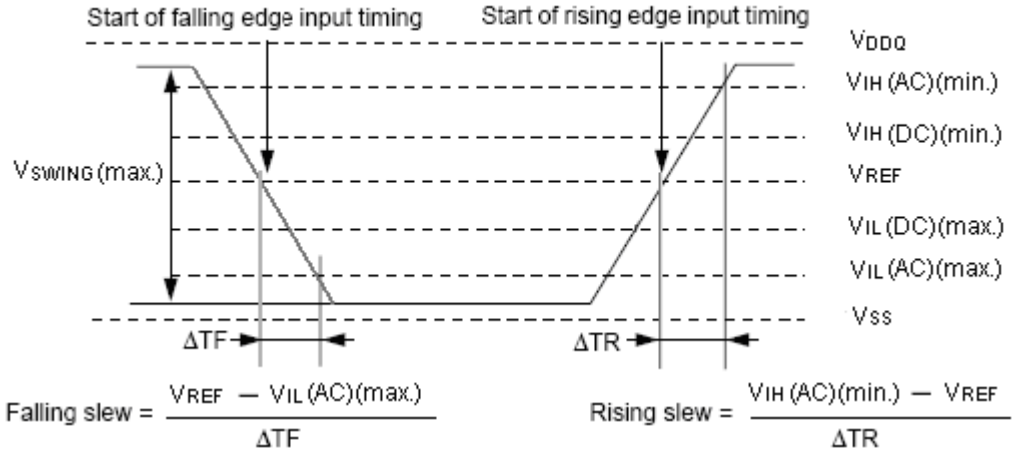


AC Operating Test Conditions

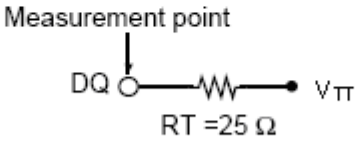
Parameter	Value	Unit	Note
Input reference voltage (V_{REF})	0.5 x V_{DDQ}	V	1
Input signal maximum peak swing (V_{SWING}(max.))	1.0	V	1
Input signal minimum slew rate	1.0	V/ns	2,3
Input level	V_{IH} / V_{IL}	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level (V_{OTR})	0.5 x V_{DDQ}	V	4

Note:

1. Input waveform timing is referenced to the input signal crossing through the V_{IH} / V_{IL} (AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH} (AC) (min.) for rising edges and the range from V_{REF} to V_{IL} (AC)(max.) for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL} (AC) to V_{IH} (AC) on the positive transitions and V_{IH} (AC) to V_{IL} (AC) on the negative transitions.
4. The V_{DDQ} of the device under test is reference.



AC Input Test Signal Wave forms



Output Load

AC Timing Parameter & Specifications

Parameter		Symbol	-1.3		-1.5		Unit	Note
			Min.	Max.	Min.	Max.		
Clock period	CL=7	t_{CK} (avg)	1333	3000	1500	3000	ps	13
DQ output access time from CLK/ $\overline{CLK}$		t_{AC}	-400	+400	-350	+350	ps	10
CLK high-level width		t_{CH} (avg)	0.48	0.52	0.48	0.52	t_{CK} (avg)	13
CLK low-level width		t_{CL} (avg)	0.48	0.52	0.48	0.52	t_{CK} (avg)	13
DQS output access time from CLK/ $\overline{CLK}$		t_{DQSCK}	-350	+350	-300	+300	ps	10
Clock to first rising edge of DQS delay		t_{DQSS}	-0.25	+0.25	-0.25	+0.25	t_{CK} (avg)	
Data-in and DM setup time (to DQS)		t_{DS} (base)	200		200		ps	4
Data-in and DM hold time (to DQS)		t_{DH} (base)	200		200		ps	5
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		t_{CK} (avg)	
Address and Control Input setup time		t_{IS} (base)	125		125		ps	4
Address and Control Input hold time		t_{IH} (base)	250		200		ps	5
Control and Address input pulse width		t_{IPW}	0.6		0.6		t_{CK} (avg)	
DQS input high pulse width		t_{DQSH}	0.35		0.44		t_{CK} (avg)	
DQS input low pulse width		t_{DQSL}	0.35		0.44		t_{CK} (avg)	
DQS falling edge to CLK rising setup time		t_{DSS}	0.2		0.2		t_{CK} (avg)	
DQS falling edge from CLK rising hold time		t_{DSH}	0.2		0.2		t_{CK} (avg)	
Data strobe edge to output data edge		t_{DQSQ}		200		250	ps	
Data-out high-impedance window from CLK/ $\overline{CLK}$		t_{HZ}		t_{AC}(max.)		t_{AC}(max.)	ps	10
Data-out low-impedance window from CLK/ $\overline{CLK}$		t_{LZ} (DQS)	t_{AC}(min.)	t_{AC}(max.)	t_{AC}(min.)	t_{AC}(max.)	ps	10
DQ low-impedance window from CLK/ $\overline{CLK}$		t_{LZ} (DQ)	2 x t_{AC}(min.)	t_{AC}(max.)	2 x t_{AC}(min.)	t_{AC}(max.)	ps	10
Half clock period		t_{HP}	Min (t_{CL}(abs),t_{CH}(abs))		Min (t_{CL}(abs),t_{CH}(abs))		ps	6,13
DQ/DQS output hold time from DQS		t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ps	
DQ hold skew factor		t_{QHS}		300		250	ps	

AC Timing Parameter & Specifications - Contiuned

Parameter	Symbol	-1.3		-1.5		Unit	Note
		Min.	Max.	Min.	Max.		
Active to Precharge command	t_{RAS}	60	70K	45	70K	ns	
Active to Active command (same bank)	t_{RC}	80		58.125		ns	
Auto Refresh row cycle time	t_{RFC}	150		130		ns	
Active to Read, Write delay	t_{RCD}	13.3		13.5		ns	
Precharge command period	t_{RP}	13.3		13.5		ns	
Active bank A to Active bank B command	t_{RRD}	12		10		ns	
Write recovery time	t_{WR}	15		15		ns	
Write data in to Read command delay	t_{WTR}	7.5		7.5		ns	19
Col. address to Col. address delay	t_{CCD}	4		2		t_{CK}	
Average periodic Refresh interval (0℃ ≦T_C ≦ +85℃)	t_{REFI}		7.8		7.8	us	
Average periodic Refresh interval (+85℃ <T_C ≦ +95℃)	t_{REFI}		3.9		3.9	us	
Write preamble	t_{WPRE}	0.35		0.35		t_{CK} (avg)	
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK} (avg)	
DQS Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK} (avg)	11
DQS Read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK} (avg)	12
Load Mode Register / Extended Mode Register cycle time	t_{MRD}	2		5		t_{CK}	
Auto Precharge write recovery + Precharge time	t_{DAL}	X		- X		t_{CK}	1, 20
Internal Read to Precharge command delay	t_{RTP}	10		7.5		ns	
Exit Self Refresh to Read command	t_{XSRD}	200		200		t_{CK}	
Exit Self Refresh to non-Read command	t_{XSNR}	t_{RFC} + 10		t_{RFC} + 10		ns	
Exit Precharge Power-Down to any non-Read command	t_{XP}	5		5		t_{CK}	
Exit Active Power-Down to Read command	t_{XARD}	5		5		t_{CK}	3
Exit active power-down to Read command (slow exit / low power mode)	t_{XARDS}	12 - AL		10 - AL		t_{CK}	2,3
CKE minimum pulse width (high and low pulse width)	t_{CKE}	5		5		t_{CK}	

AC Timing Parameter & Specifications - Contiuned

Parameter	Symbol	-1.3		-1.5		Unit	Note
		Min.	Max.	Min.	Max.		
Minimum time clocks remains ON after CKE asynchronously drops low	t_{DELAY}	t_{IS} + t_{CK} (avg)*2+t_{IH}		t_{IS} + t_{CK} (avg)+t_{IH}		ns	
Output impedance test driver delay	t_{OIT}	0	12	0	12	ns	
MRS command to ODT update delay	t_{MOD}	0	12	0	12	ns	
ODT turn-on delay	t_{AOND}	2	2	2	2	t_{CK}	
ODT turn-on	t_{AON}	t_{AC}(min.)	t_{AC}(max.) + 700	t_{AC}(min.)	t_{AC}(max.) + 2575	ps	14,16
ODT turn-on (Power-Down mode)	t_{AONPD}	t_{AC}(min.) + 2000	2 x t_{CK} +t_{AC}(max.) + 1000	t_{AC}(min.) + 2000	3 x t_{CK} +t_{AC}(max.) + 1000	ps	
ODT turn-off delay	t_{AOFD}	5	5	2.5	2.5	t_{CK}	15,17, 18
ODT turn-off	t_{AOF}	t_{AC}(min.)	t_{AC}(max.) + 600	t_{AC}(min.)	t_{AC}(max.) + 600	ps	
ODT turn-off (Power-Down mode)	t_{AOFPD}	t_{AC}(min.) + 2000	2.5 x t_{CK} +t_{AC}(max.) + 1000	t_{AC}(min.) + 2000	2.5 x t_{CK} +t_{AC}(max.) + 1000	ps	
ODT to Power-Down entry latency	t_{ANPD}	5		4		t_{CK}	
ODT Power-Down exit latency	t_{AXPD}	10		11		t_{CK}	

AC Timing Parameter & Specifications - Contiuned

Parameter		Symbol	-1.8		-2.5		Unit	Note
			Min.	Max.	Min.	Max.		
Clock period	CL=7	t_{CK} (avg)	1875	7500	-	-	ps	13
	CL=6		X	X	2500	8000		
	CL=5		X	X	2500	8000		
	CL=4		X	X	X	X		
DQ output access time from CLK/ $\overline{CLK}$		t_{AC}	-350	+350	-400	+400	ps	10
CLK high-level width		t_{CH} (avg)	0.48	0.52	0.48	0.52	t_{CK} (avg)	13
CLK low-level width		t_{CL} (avg)	0.48	0.52	0.48	0.52	t_{CK} (avg)	13
DQS output access time from CLK/ $\overline{CLK}$		t_{DQSCK}	-300	+300	-350	+350	ps	10
Clock to first rising edge of DQS delay		t_{DQSS}	-0.25	+0.25	-0.25	+0.25	t_{CK} (avg)	
Data-in and DM setup time (to DQS)		t_{DS} (base)	0		50		ps	4
Data-in and DM hold time (to DQS)		t_{DH} (base)	75		125		ps	5
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		t_{CK} (avg)	
Address and Control Input setup time		t_{IS} (base)	125		175		ps	4
Address and Control Input hold time		t_{IH} (base)	200		250		ps	5
Control and Address input pulse width		t_{IPW}	0.6		0.6		t_{CK} (avg)	
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK} (avg)	
DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK} (avg)	
DQS falling edge to CLK rising setup time		t_{DSS}	0.2		0.2		t_{CK} (avg)	
DQS falling edge from CLK rising hold time		t_{DSH}	0.2		0.2		t_{CK} (avg)	
Data strobe edge to output data edge		t_{DQSQ}		175		200	ps	
Data-out high-impedance window from CLK/ $\overline{CLK}$		t_{HZ}		t_{AC}(max.)		t_{AC}(max.)	ps	10
Data-out low-impedance window from CLK/ $\overline{CLK}$		t_{LZ} (DQS)	t_{AC}(min.)	t_{AC}(max.)	t_{AC}(min.)	t_{AC}(max.)	ps	10
DQ low-impedance window from CLK/ $\overline{CLK}$		t_{LZ} (DQ)	2 x t_{AC}(min.)	t_{AC}(max.)	2 x t_{AC}(min.)	t_{AC}(max.)	ps	10
Half clock period		t_{HP}	Min (t_{CL}(abs),t_{CH}(abs))		Min (t_{CL}(abs),t_{CH}(abs))		ps	6,13

AC Timing Parameter & Specifications - Contiuned

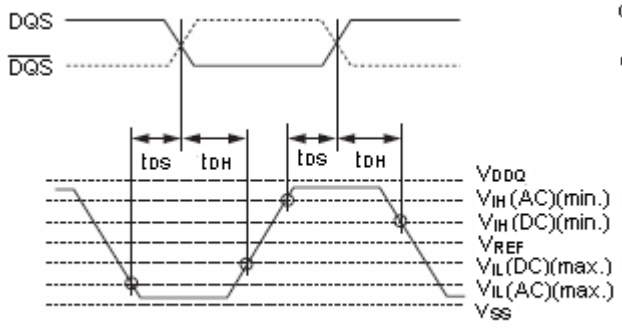
Parameter	Symbol	-1.8		-2.5		Unit	Note
		Min.	Max.	Min.	Max.		
DQ/DQS output hold time from DQS	t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ps	
DQ hold skew factor	t_{QHS}		250		300	ps	
Active to Precharge command	t_{RAS}	45	70K	45	70K	ns	
Active to Active command (same bank)	t_{RC}	58.125		57.5		ns	
Auto Refresh row cycle time	t_{RFC}	105		105		ns	
Active to Read, Write delay	t_{RCD}	13.125		12.5		ns	
Precharge command period	t_{RP}	13.125		12.5		ns	
Active bank A to Active bank B command	t_{RRD}	10		10		ns	
Write recovery time	t_{WR}	15		15		ns	
Write data in to Read command delay	t_{WTR}	7.5		7.5		ns	19
Col. address to Col. address delay	t_{CCD}	2		2		t_{CK}	
Average periodic Refresh interval (0℃ ≦T_C ≦ +85℃)	t_{REFI}		7.8		7.8	us	
Average periodic Refresh interval (+85℃ <T_C ≦ +95℃)	t_{REFI}		3.9		3.9	us	
Write preamble	t_{WPRE}	0.35		0.35		t_{CK} (avg)	
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK} (avg)	
DQS Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK} (avg)	11
DQS Read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK} (avg)	12
Load Mode Register / Extended Mode Register cycle time	t_{MRD}	2		2		t_{CK}	
Auto Precharge write recovery + Precharge time	t_{DAL}	WR+tn_{RP}		WR+tn_{RP}		t_{CK}	1
Internal Read to Precharge command delay	t_{RTP}	7.5		7.5		ns	
Exit Self Refresh to Read command	t_{XSRD}	200		200		t_{CK}	
Exit Self Refresh to non-Read command	t_{XSNR}	t_{RFC} + 10		t_{RFC} + 10		ns	
Exit Precharge Power-Down to any non-Read command	t_{XP}	3		2		t_{CK}	
Exit Active Power-Down to Read command	t_{XARD}	3		2		t_{CK}	3
Exit active power-down to Read command (slow exit / low power mode)	t_{XARDS}	10 - AL		8 - AL		t_{CK}	2,3
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3		3		t_{CK}	

AC Timing Parameter & Specifications - Contiuned

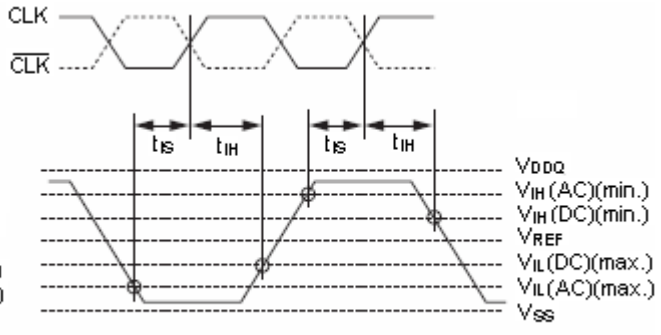
Parameter	Symbol	-1.8		-2.5		Unit	Note
		Min.	Max.	Min.	Max.		
Minimum time clocks remains ON after CKE asynchronously drops low	t_{DELAY}	t_{IS} + t_{CK} (avg)+t_{IH}		t_{IS} + t_{CK} (avg)+t_{IH}		ns	
Output impedance test driver delay	t_{OIT}	0	12	0	12	ns	
MRS command to ODT update delay	t_{MOD}	0	12	0	12	ns	
ODT turn-on delay	t_{AOND}	2	2	2	2	t_{CK}	
ODT turn-on	t_{AON}	t_{AC}(min.)	t_{AC}(max.) + 2575	t_{AC}(min.)	t_{AC}(max.) + 700	ps	14,16
ODT turn-on (Power-Down mode)	t_{AONPD}	t_{AC}(min.) + 2000	3 x t_{CK} +t_{AC}(max.) + 1000	t_{AC}(min.) + 2000	2 x t_{CK} +t_{AC}(max.) + 1000	ps	
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	t_{CK}	15,17, 18
ODT turn-off	t_{AOF}	t_{AC}(min.)	t_{AC}(max.) + 600	t_{AC}(min.)	t_{AC}(max.) + 600	ps	
ODT turn-off (Power-Down mode)	t_{AOFPD}	t_{AC}(min.) + 2000	2.5 x t_{CK} +t_{AC}(max.) + 1000	t_{AC}(min.) + 2000	2.5 x t_{CK} +t_{AC}(max.) + 1000	ps	
ODT to Power-Down entry latency	t_{ANPD}	4		3		t_{CK}	
ODT Power-Down exit latency	t_{AXPD}	11		8		t_{CK}	

Note:

1. t_{DAL}[nCLK] = WR[nCLK] + tn_{RP} [nCLK] =WR+RU{t_{RP}[ps]/t_{CK}(avg)[ps]}, where WR is the value programmed in the mode register set and RU status for round up.
2. AL: Additive Latency.
3. MRS A12 bit defines which Active Power-Down Exit timing to be applied.
4. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the V_{IH} (AC) level for a rising signal and V_{IL} (AC) for a falling signal applied to the device under test.
5. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the V_{IL} (DC) level for a rising signal and V_{IH} (DC) for a falling signal applied to the device under test.



Input Waveform Timing 1 (t_{DS}, t_{DH})



Input Waveform Timing 2 (t_{IS} , t_{IH})

6. t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation;
   t_{HP} = Min (t_{CH} (abs), t_{CL} (abs)), where:
   t_{CH} (abs) is the minimum of the actual instantaneous clock HIGH time;
   t_{CL} (abs) is the minimum of the actual instantaneous clock LOW time;

7. t_{QHS} accounts for:
   a. The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and
   b. The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers.
8. $t_{QH} = t_{HP} - t_{QHS}$, where:
   t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.}
   Examples:
   a. If the system provides t_{HP} of 825 ps into a DDR2-1066 SDRAM, the DRAM provides t_{QH} of 575 ps minimum.
   b. If the system provides t_{HP} of 900 ps into a DDR2-1066 SDRAM, the DRAM provides t_{QH} of 650 ps minimum.
9. RU stands for round up. WR refers to the t_{WR} parameter stored in the MRS.
10. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual t_{ERR} (6-10per) of the input clock. (output de-ratings are relative to the SDRAM input clock.)
    For example, if the measured jitter into a DDR2- 1066 SDRAM has t_{ERR} (6-10per)(min.) = - 202 ps and t_{ERR} (6-10per)(max.) = + 223 ps, then t_{DQSCK} (min.)(derated) = t_{DQSCK} (min.) - t_{ERR} (6-10per)(max.) = -300 ps – 223 ps = -523 ps and t_{DQSCK} (max.) (derated) = t_{DQSCK} (max.) - t_{ERR} (6-10per)(min.) = 300 ps + 202 ps = +502 ps. Similarly, t_{LZ} (DQ) for DDR2-1066 de-rates to t_{LZ} (DQ)(min.)(derated) = -700 ps - 223 ps = -923 ps and t_{LZ} (DQ)(max.)(derated) = 350 ps + 202 ps = +552 ps.
11. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual t_{JIT} (per) of the input clock. (output de-ratings are relative to the SDRAM input clock.)
    For example, if the measured jitter into a DDR2-1066 SDRAM has t_{JIT} (per)(min.) = - 72 ps and t_{JIT} (per)(max.) = + 63 ps, then t_{RPRE} (min.)(derated) = t_{RPRE} (min.) + t_{JIT} (per)(min.) = 0.9 x t_{CK} (avg) - 72 ps = + 1615.5 ps and t_{RPRE} (max.)(derated) = t_{RPRE} (max.) + t_{JIT} (per)(max.) = 1.1 x t_{CK} (avg) + 63 ps = + 2125.5 ps.
12. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual t_{JIT} (duty) of the input clock. (output de-ratings are relative to the SDRAM input clock.)
    For example, if the measured jitter into a DDR2-1066 SDRAM has t_{JIT} (duty)(min.) = - 72 ps and t_{JIT} (duty)(max.) = + 63 ps, then t_{RPST} (min.)(derated) = t_{RPST} (min.) + t_{JIT} (duty)(min.) = 0.4 x t_{CK} (avg) - 72 ps = + 678 ps and t_{RPST} (max.)(derated) = t_{RPST} (max.) + t_{JIT} (duty)(max.) = 0.6 x t_{CK} (avg) + 63 ps = + 1188 ps.
13. Refer to the Clock Jitter table.
14. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
    ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}.
15. ODT turn off time min is when the device starts to turn off ODT resistance.
    ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}.
16. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual t_{ERR} (6-10per) of the input clock. (output de-ratings are relative to the SDRAM input clock.)
17. When the device is operated with input clock jitter, this parameter needs to be derated by { - t_{JIT} (duty)(max.) - t_{ERR} (6-10per)(max.) } and { - t_{JIT} (duty)(min.) - t_{ERR} (6-10per)(min.) } of the actual input clock. (output deratings are relative to the SDRAM input clock.)
    For example, if the measured jitter into a DDR2- 1066 SDRAM has t_{ERR} (6-10per)(min.) = - 202 ps, t_{ERR} (6- 10per)(max.) = + 223 ps, t_{JIT} (duty)(min.) = - 66 ps and t_{JIT} (duty)(max.) = + 74 ps, then t_{AOF}(min.)(derated) = t_{AOF}(min.) + { - t_{JIT} (duty)(max.) - t_{ERR} (6-10per)(max.) } = - 350 ps + { - 74 ps - 223 ps} = - 647 ps and t_{AOF}(max.)(derated) = t_{AOF}(max.) + { - t_{JIT} (duty)(min.) - t_{ERR} (6-10per)(min.) } = 950 ps + { 66 ps + 202 ps } = + 1218 ps.
18. For t_{AOFD} of DDR2-800/1066, the 1/2 clock of t_{CK} in the 2.5 x t_{CK} assumes a t_{CH} (avg), average input clock HIGH pulse width of 0.5 relative to t_{CK} (avg). t_{AOF} (min.) and t_{AOF} (max.) should each be derated by the same amount as the actual amount of t_{CH} (avg) offset present at the DRAM input with respect to 0.5.
    For example, if an input clock has a worst case t_{CH} (avg) of 0.48, the t_{AOF} (min.) should be derated by subtracting 0.02 x t_{CK} (avg) from it, whereas if an input clock has a worst case t_{CH} (avg) of 0.52, the t_{AOF} (max.) should be derated by adding 0.02 x t_{CK} (avg) to it. Therefore, we have;
    t_{AOF} (min.)(derated) = t_{AC} (min.) - [0.5 - Min(0.5, t_{CH} (avg)(min.))] x t_{CK} (avg)
    t_{AOF} (max.)(derated) = t_{AC} (max.) + 0.6 + [Max(0.5, t_{CH} (avg)(max.)) - 0.5] x t_{CK} (avg) or
    t_{AOF} (min.)(derated) = Min(t_{AC} (min.), t_{AC} (min.) - [0.5 - t_{CH} (avg)(min.)] x t_{CK} (avg))
    t_{AOF} (max.)(derated) = 0.6 + Max(t_{AC} (max.), t_{AC} (max.) + [t_{CH} (avg)(max.) - 0.5] x t_{CK} (avg)), where:
    t_{CH} (avg)(min.) and t_{CH} (avg)(max.) are the minimum and maximum of t_{CH} (avg) actually measured at the DRAM input balls.
19. t_{WTR} is at lease two clocks (2 x t_{CK} or 2 x nCK) independent of operation frequency.
20. If $t_{CK} < 1.875$ns, the device can not support Write with Auto Precharge function.

ODT DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rtt effective impedance value for 75Ω setting EMRS(1) [A6, A2] = 0, 1	Rtt1(eff)	60	75	90	Ω
Rtt effective impedance value for 150Ω setting EMRS(1) [A6, A2) = 1, 0	Rtt2(eff)	120	150	180	Ω
Rtt effective impedance value for 50Ω setting EMRS(1) [A6, A2] = 1, 1	Rtt3(eff)	40	50	60	Ω
Deviation of VM with respect to V_{DDQ} /2	△VM	-6	-	+6	%

Note:

Measurement Definition for Rtt(eff) :

Rtt(eff) is determined by separately applying V_{IH}(AC) and V_{IL}(AC) to test pin, and then measuring current I(V_{IH}(AC)) and I(V_{IL}(AC)) respectively.

$$Rtt(eff) = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

Measurement Definition for △VM :

Measure voltage (VM) at test pin with no load.

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1\right) \times 100\%$$

OCD Default Characteristics

Parameter	Min.	Typ.	Max.	Unit	Note
Output impedance	12.6	18	23.4	Ω	1
Pull-up and pull-down mismatch	0	-	4	Ω	1,2,3
Output slew rate	1.5	-	5	V/ns	1,4,5

Note:

1. Absolute specifications: the operation range of Voltage and Temperature.
2. Impedance measurement condition for output source DC current: V_{DDQ} = 1.7V; V_{OUT} = 1,420mV; (V_{OUT} - V_{DDQ})/I_{OH} must be less than 23.4Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV. Impedance measurement condition for output sink DC current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-down; both are measured at same temperature and voltage.
4. Slew rate measured from V_{IL} (AC) to V_{IH} (AC).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC.

Clock Jitter [DDR2- 1500, 1333, 1066, 800]

Parameter	Symbol	-1.3		-1.5		-1.8		-2.5		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Average clock period	t_{CK} (avg)	1333	3000	1500	3000	1875	7500	2500	8000	ps	1
Clock period jitter	t_{JIT} (per)	-30	30	-50	50	-90	90	-100	100	ps	5
Clock period jitter during DLL locking period	t_{JIT} (per,lck)	-30	30	-40	40	-80	80	-80	80	ps	5
Cycle to cycle period jitter	t_{JIT} (cc)	-80	80	-130	130	-180	180	-200	200	ps	6
Cycle to cycle clock period jitter During DLL locking period	t_{JIT} (cc, lck)	-70	70	-120	120	-160	160	-160	160	ps	6
Cumulative error across 2 cycles	t_{ERR} (2per)	-50	50	-100	100	-132	132	-150	150	ps	7
Cumulative error across 3 cycles	t_{ERR} (3per)	-50	50	-100	100	-157	157	-175	175	ps	7
Cumulative error across 4 cycles	t_{ERR} (4per)	-50	50	-100	100	-175	175	-200	200	ps	7
Cumulative error across 5 cycles	t_{ERR} (5per)	-50	50	-100	100	-188	188	-200	200	ps	7
Cumulative error across n=6,7,8,9,10 cycles	t_{ERR} (6-10per)	-100	100	-150	150	-250	250	-300	300	ps	7
Cumulative error across n=11,12,….49,50 cycles	t_{ERR} (11-50per)	-100	100	-150	150	-425	425	-450	450	ps	7
Average high pulse width	t_{CH} (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK} (avg)	2
Average low pulse width	t_{CL} (avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK} (avg)	3
Duty cycle jitter	t_{JIT} (duty)	-30	30	-45	45	-75	75	-100	100	ps	4

Note:

1. t_{CK} (avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$t_{CK}(avg) = \left\{ \sum_{j=1}^{N} t_{CKj} \right\} \Big/ N$$

$$N = 200$$

2. t_{CH} (avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$t_{CH}(avg) = \left\{ \sum_{j=1}^{N} t_{CHj} \right\} \Big/ \left(N \times t_{CK}(avg) \right)$$

$$N = 200$$

3. t_{CL} (avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$t_{CL}(avg) = \left\{ \sum_{j=1}^{N} t_{CLj} \right\} \Big/ \left(N \times t_{CK}(avg) \right)$$

$$N = 200$$

4. t_{JIT} (duty) is defined as the cumulative set of t_{CH} jitter and t_{CL} jitter. t_{CH} jitter is the largest deviation of any single t_{CH} from t_{CH} (avg). t_{CL} jitter is the largest deviation of any single t_{CL} from t_{CL} (avg).
   t_{JIT} (duty) is not subject to production test.
   t_{JIT} (duty) = Min./Max. of { t_{JIT} (CH), t_{JIT} (CL)}, where:
   t_{JIT} (CH) = { t_{CH} j - t_{CH} (avg) where j =1 to 200}
   t_{JIT} (CL) = {t_{CL} j - t_{CL} (avg) where j =1 to 200}

5. t_{JIT} (per) is defined as the largest deviation of any single t_{CK} from t_{CK} (avg).
   t_{JIT} (per) = Min./Max. of { t_{CK} j - t_{CK} (avg) where j =1 to 200}
   t_{JIT} (per) defines the single period jitter when the DLL is already locked.
   t_{JIT} (per, lck) uses the same definition for single period jitter, during the DLL locking period only.
   t_{JIT} (per) and t_{JIT} (per, lck) are not subject to production testing.

6. t_{JIT} (cc) is defined as the difference in clock period between two consecutive clock cycles : t_{JIT} (cc) = Max. of | t_{CK} i +1 - t_{CK} i|
   t_{JIT} (cc) defines the cycle to cycle jitter when the DLL is already locked.
   t_{JIT} (cc, lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
   t_{JIT} (cc) and t_{JIT} (cc, lck) are not subject to production testing.

7. t_{ERR} (nper) is defined as the cumulative error across multiple consecutive cycles from t_{CK} (avg).
   t_{ERR} (nper) is not subject to production testing.

$$t_{ERR}(nper) = \left\{ \sum_{j=1}^{N} t_{CKj} \right\} - n \times t_{CK}(avg)$$

$$2 \le n \le 50 \text{ for } t_{ERR}(nper)$$

8. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min. and max. of SPEC values are to be used for calculations in the table below.)

Parameter	Symbol	Min.	Max.	Unit
Absolute clock period	t_{CK} (abs)	t_{CK} (avg)(min.) + t_{JIT} (per)(min.)	t_{CK} (avg)(max.) + t_{JIT} (per)(max.)	ps
Absolute clock high pulse width	t_{CH} (abs)	t_{CH} (avg)(min.) x t_{CK} (avg)(min.) + t_{JIT} (duty)(min.)	t_{CH} (avg)(max.) x t_{CK} (avg)(max.) + t_{JIT} (duty)(max.)	ps
Absolute clock low pulse width	t_{CL} (abs)	t_{CL} (avg)(min.) x t_{CK} (avg)(min.) + t_{JIT} (duty)(min.)	t_{CL} (avg)(max.) x t_{CK} (avg)(max.) + t_{JIT} (duty)(max.)	ps

Example: For DDR2-1066, t_{CH} (abs)(min.) = (0.48 x 1875ps) - 75 ps = 825 ps

Input Slew Rate De-rating

For all input signals the total t_{IS}, t_{DS} (setup time) and t_{IH}, t_{DH} (hold time) required is calculated by adding the data sheet t_{IS} (base), t_{DS} (base) and t_{IH} (base), t_{DH} (base) value to the Δt_{IS}, Δt_{DS} and Δt_{IH}, Δt_{DH} de-rating value respectively.
Example: t_{DS} (total setup time) = t_{DS} (base) + Δt_{DS}.

Setup (t_{IS}, t_{DS}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF} (DC) and the first crossing of V_{IH} (AC)(min.). Setup (t_{IS}, t_{DS}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF} (DC) and the first crossing of V_{IL} (AC)(max.). If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{REF} (DC) to AC region', use nominal slew rate for de-rating value (See the figure of Slew Rate Definition Nominal).
If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{REF} (DC) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for de-rating value (see the figure of Slew Rate Definition Tangent).

Hold (t_{IH}, t_{DH}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL} (DC)(max.) and the first crossing of V_{REF} (DC). Hold (t_{IH}, t_{DH}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH} (DC)(min.) and the first crossing of V_{REF} (DC). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to V_{REF} (DC) region', use nominal slew rate for de-rating value (See the figure of Slew Rate Definition Nominal).
If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to V_{REF} (DC) region', the slew rate of a tangent line to the actual signal from the DC level to V_{REF} (DC) level is used for de-rating value (see the figure of Slew Rate Definition Tangent).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached V_{IH} / V_{IL} (AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach V_{IH} / V_{IL} (AC).

For slew rates in between the values listed in the tables below, the de-rating values may be obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

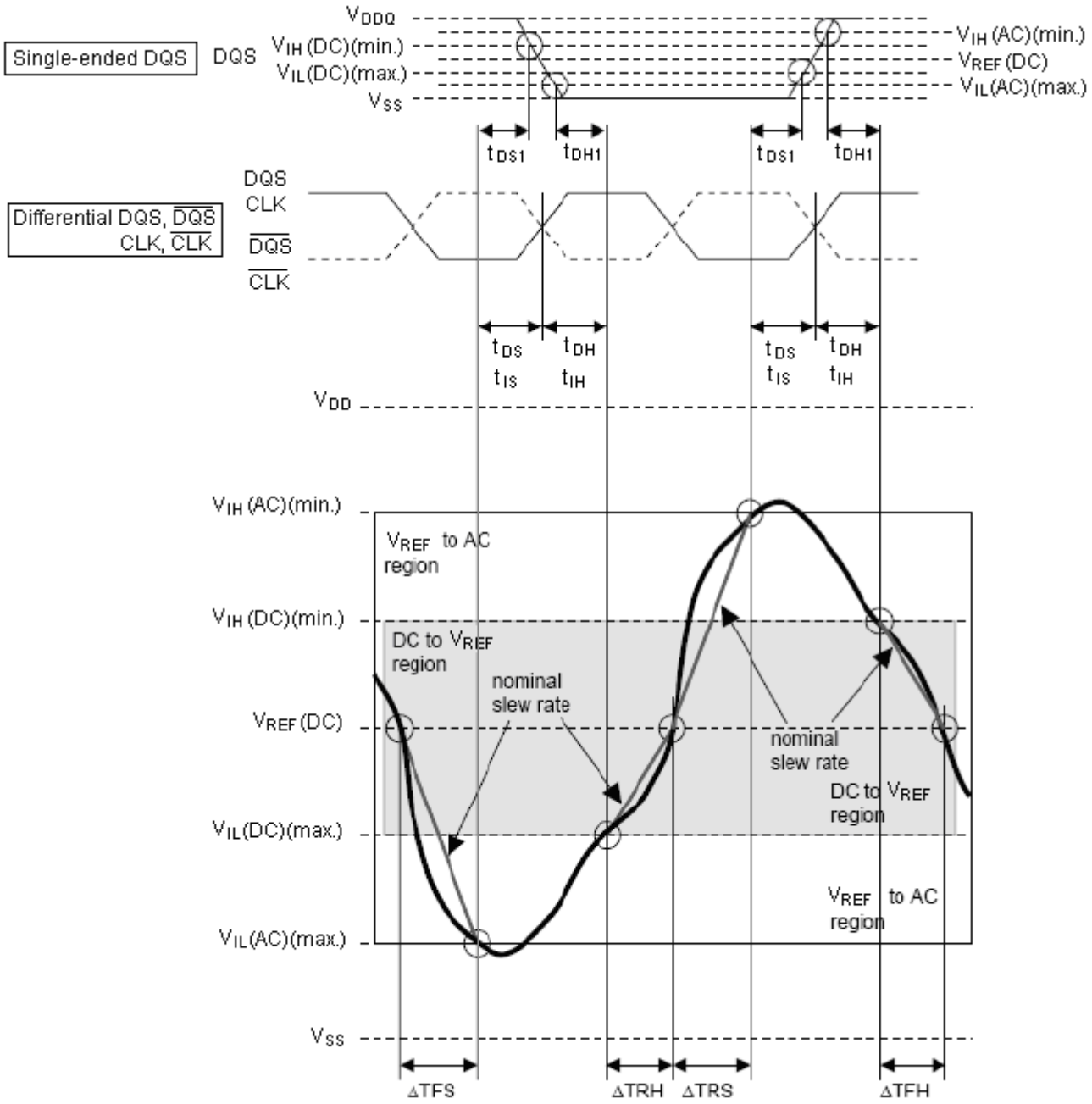
De-rating Value of t_{DS}/t_{DH} with Differential DQS(DDR2-800, 1066, 1333, 1500)

		DQS, $\overline{DQS}$ differential slew rate																		
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		Unit
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	
DQ slew rate (V/ns)	2.0	+100	+45	+100	+45	+100	+45	-	-	-	-	-	-	-	-	-	-	-	-	ps
	1.5	+67	+21	+67	+21	+67	+21	+79	+33	-	-	-	-	-	-	-	-	-	-	ps
	1.0	0	0	0	0	0	0	+12	+12	+24	+24	-	-	-	-	-	-	-	-	ps
	0.9	-	-	-5	-14	-5	-14	+7	-2	+19	+10	+31	+22	-	-	-	-	-	-	ps
	0.8	-	-	-	-	-13	-31	-1	-19	+11	-7	+23	+5	+35	+17	-	-	-	-	ps
	0.7	-	-	-	-	-	-	-10	-42	+2	-30	+14	-18	+26	-6	+38	+6	-	-	ps
	0.6	-	-	-	-	-	-	-	-	-10	-59	+2	-47	+14	-35	+26	-23	+38	-11	ps
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	+12	-53	ps
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116	ps

De-rating Value of t_{IS}/t_{IH} (DDR2-800, 1066, 1333, 1500)

		CLK, $\overline{CLK}$ differential slew rate						
		2.0 V/ns		1.5 V/ns		1.0 V/ns		Unit
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	
Command / Address slew rate (V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps
	3.5	+143	+89	+173	+119	+203	+149	ps
	3.0	+133	+83	+163	+113	+193	+143	ps
	2.5	+120	+75	+150	+105	+180	+135	ps
	2.0	+100	+45	+130	+75	+160	+105	ps
	1.5	+67	+21	+97	+51	+127	+81	ps
	1.0	0	0	+30	+30	+60	+60	ps
	0.9	-5	-14	+25	+16	+55	+46	ps
	0.8	-13	-31	+17	-1	+47	+29	ps
	0.7	-22	-54	+8	-24	+38	+6	ps
	0.6	-34	-83	-4	-53	+26	-23	ps
	0.5	-60	-125	-30	-95	0	-65	ps
	0.4	-100	-188	-70	-158	-40	-128	ps
	0.3	-168	-292	-138	-262	-108	-232	ps
	0.25	-200	-375	-170	-345	-140	-315	ps
	0.2	-325	-500	-295	-470	-265	-440	ps
	0.15	-517	-708	-487	-678	-457	-648	ps
	0.1	-1000	-1125	-970	-1095	-940	-1065	ps

Slew Rate Definition Nominal



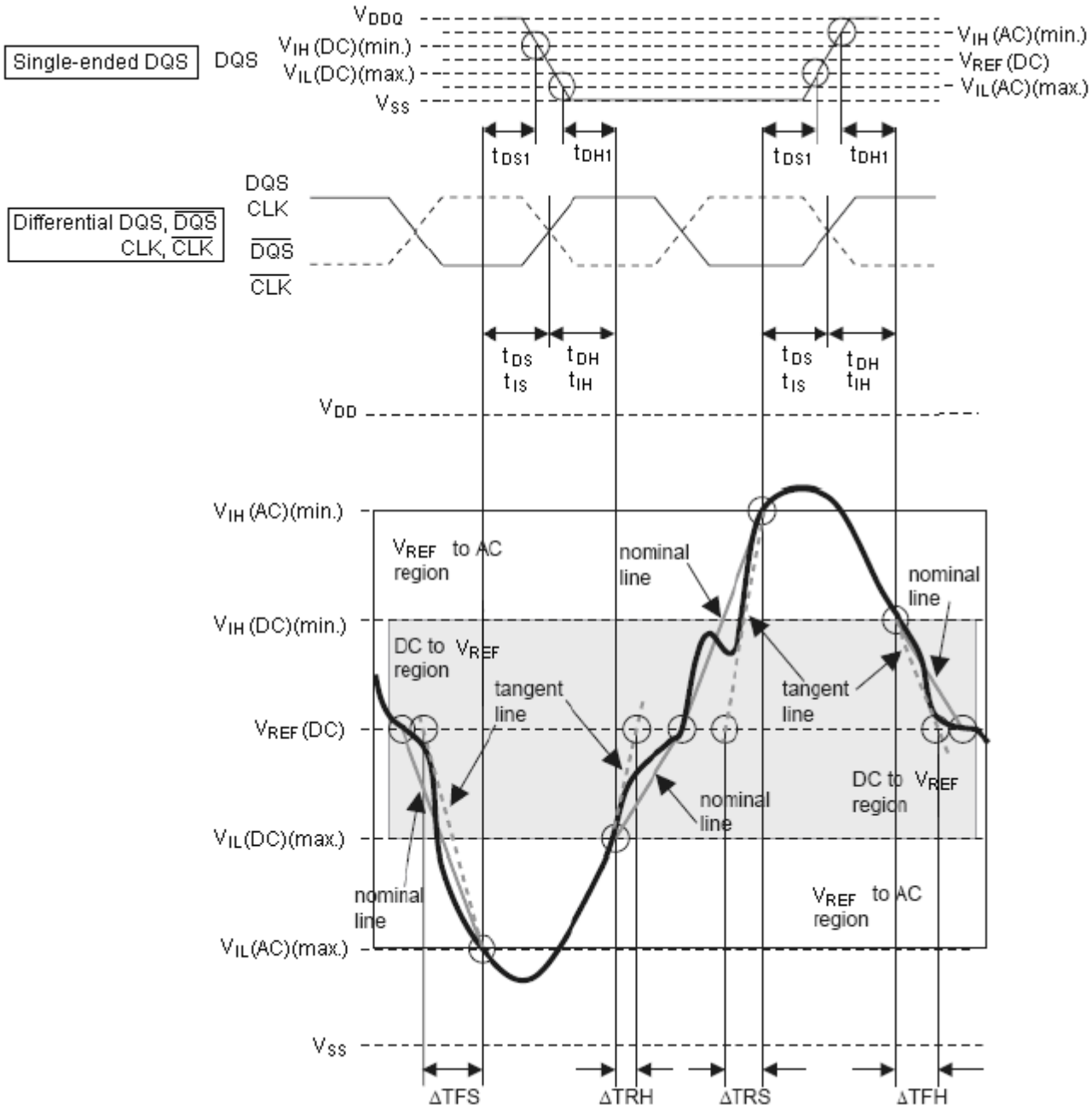
$$\text{Setup slew rate Falling signal} = \frac{V_{REF}(DC) - V_{IL}(AC)(max.)}{\Delta TFS}$$

$$\text{Setup slew rate Rising signal} = \frac{V_{IH}(AC)(min.) - V_{REF}(DC)}{\Delta TRS}$$

$$\text{Hold slew rate Rising signal} = \frac{V_{REF}(DC) - V_{IL}(DC)(max.)}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{V_{IH}(DC)(min.) - V_{REF}(DC)}{\Delta TFH}$$

Slew Rate Definition Tangent



$$\text{Setup slew rate Falling signal} = \frac{\text{tangent line } [V_{REF}(DC) - V_{IL}(AC)(max.)]}{\Delta TFS}$$

$$\text{Setup slew rate Rising signal} = \frac{\text{tangent line } [V_{IH}(AC)(min.) - V_{REF}(DC)]}{\Delta TRS}$$

$$\text{Hold slew rate Rising signal} = \frac{\text{tangent line } [V_{REF}(DC) - V_{IL}(DC)(max.)]}{\Delta TRH}$$

$$\text{Hold slew rate Falling signal} = \frac{\text{tangent line } [V_{IH}(DC)(min.) - V_{REF}(DC)]}{\Delta TFH}$$

Command Truth Table

COMMAND			Note 7 CKE(n-1)	Note 7 CKE(n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA0,1	A10/AP	A12~A11, A9~A0	Note
(Extended) Mode Register Set			H	H	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			
	Self Refresh	Entry		L									10,12
		Exit	L	H	L	H	H	H	X	X			6,9, 12
					H	X	X	X					
Bank Active			H	H	L	L	H	H	X	V	Row Address		
Read	Auto Precharge Disable		H	H	L	H	L	H	X	V	L	Column Address (A9~A0)	1,3
	Auto Precharge Enable										H		
Write	Auto Precharge Disable		H	H	L	H	L	L	X	V	L	Column Address (A9~A0)	1,3,17
	Auto Precharge Enable										H		
Precharge	Bank Selection		H	H	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Active Power-Down		Entry	H	L	H	X	X	X	X	X			4,11, 12,15
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				4,8, 12,15
					L	H	H	H					
Precharge Power-Down		Entry	H	L	H	X	X	X	X	X			4,11, 12,15
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				4,8, 12,15
					L	H	H	H					
DM			H	H	X				V	X			16
Device Deselect			H	X	H	X	X	X	X	X			
No Operation			H	X	L	H	H	H	X	X			

(OP code = Operand Code, V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

Note:

1. BA during a MRS/EMRS command selects which mode register is programmed.
2. MRS/EMRS can be issued only at all bank Precharge state.
3. Burst Reads or Writes at BL = 4 cannot be terminated or interrupted.
4. The Power-Down mode does not perform any Refresh operations. The duration of Power-Down is limited by the Refresh requirements. Need one clock delay to entry and exit mode.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. Self Refresh Exit is asynchronous.
7. CKE (n) is the logic state of CKE at clock edge n; CKE (n–1) was the state of CKE at the previous clock edge.
8. All states not shown are illegal or reserved unless explicitly described elsewhere in this document.
9. On Self Refresh, Exit Deselect or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} is satisfied.
10. Self Refresh mode can only be entered from all banks Idle state.
11. Power-Down and Self Refresh can not be entered while Read or Write operations, MRS/EMRS operations or Precharge operations are in progress.
12. Minimum CKE HIGH / LOW time is t_{CKE} (min).
13. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
14. CKE must be maintained HIGH while the device is in OCD calibration mode.
15. ODT must be driven HIGH or LOW in Power-Down if the ODT function is enabled.
16. Used to mask write data, provided coincident with the corresponding data.
17. If $t_{CK} < 1.875$ns, the device can not support Write with Auto Precharge function.

Power On and Initialization

DDR2 SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power-Up and Initialization Sequence

The following sequence is required for Power-Up and Initialization.

1. Apply power and attempt to maintain CKE below 0.2 x V_{DDQ} and ODT (*1) at a low state (all other inputs may be undefined).
   - V_{DD}(*2), V_{DDL}(*2) and V_{DDQ} are driven from a single power converter output, AND
   - V_{TT} is limited to 0.95V max, AND
   - V_{REF} tracks V_{DDQ} /2.

   or
   - Apply V_{DD}(*2) before or at the same time as V_{DDL}.
   - Apply V_{DDL}(*2) before or at the same time as V_{DDQ}.
   - Apply V_{DDQ} before or at the same time as V_{TT} and V_{REF}.

   at least one of these two sets of conditions must be met.
2. Start clock and maintain stable condition.
3. For the minimum of 200us after stable power and clock (CLK, $\overline{CLK}$), then apply NOP or Deselect and take CKE High.
4. Waiting minimum of 400ns then issue Precharge commands for all banks of the device. NOP or Deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “LOW” to BA0, “HIGH” to BA1.)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “HIGH” to BA0 and BA1.)
7. Issue EMRS(1) to enable DLL. (To issue "DLL Enable" command, provide "LOW" to A0, "HIGH" to BA0 and "LOW" to BA1.)
8. Issue a Mode Register Set command for “DLL reset” (*3).
   (To issue DLL reset command, provide “HIGH” to A8 and “LOW” to BA0-1)
9. Issue Precharge commands for all banks of the device.
10. Issue 2 or more Auto Refresh commands.
11. Issue a Mode Register Set command with LOW to A8 to initialize device operation. (To program operation parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD calibration (Off Chip Driver impedance adjustment).
    If OCD calibration is not used, EMRS(1) OCD default command (A9=A8= A7=1) followed by EMRS(1) OCD calibration mode exit command (A9=A8=A7=0) must be issued with other operating parameters of EMRS(1).
13. The DDR2 SDRAM is now ready for normal operation.

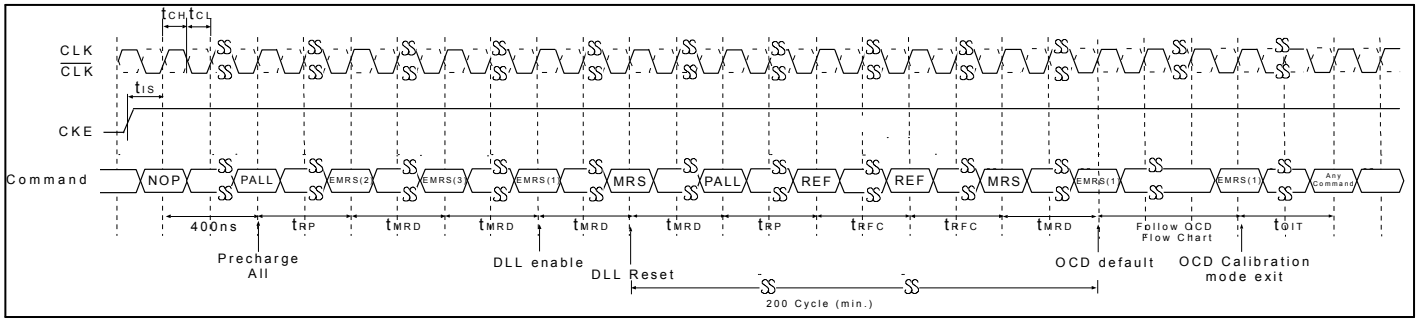
Note :

*1) To guarantee ODT off, V_{REF} must be valid and a low level must be applied to the ODT pin.

*2) If DC voltage level of V_{DDL} or V_{DD} is intentionally changed during normal operation, (for example, for the purpose of V_{DD} corner test, or power saving) “DLL Reset” must be executed.

*3) Every “DLL enable” command resets DLL. Therefore sequence 8 can be skipped during power up. Instead of it, the additional 200 cycles of clock input is required to lock the DLL after enabling DLL.

Initialization Sequence after Power-UP

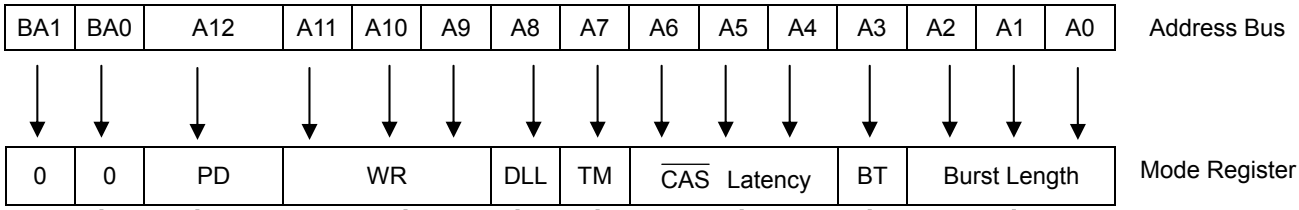


Mode Register Definition

Mode Register Set [MRS]

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs $\overline{CAS}$ latency, burst length, burst type, test mode, DLL reset, WR and various vendor specific options to make the device useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after Power-Up for proper operation. The mode register is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1 (The device should be in all bank Precharge with CKE already high prior to writing into the mode register). The state of address pins A0~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1 going LOW are written in the mode register.

The t_{MRD} time is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length is defined by A0 ~ A2. Burst address sequence type is defined by A3, CAS latency (read latency from column address) is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time WR is defined by A9 ~ A11. Refer to the table for specific codes.



Active Power down exit timing

A12	PD
0	Fast Exit (normal)
1	Slow Exit (low power)

A7	Mode
0	No
1	Yes

A3	Burst Type
0	Sequential
1	Interleave

BA1	BA0	Mode Register
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3) : Reserved

A8	DLL reset
0	No
1	Yes

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Write recovery for Auto Precharge

A11	A10	A9	WR(cycles)*1	
0	0	0	Reserved*2	
0	0	1	2	DDR2-800
0	1	0	3	DDR2-800
0	1	1	4	DDR2-800
1	0	0	5	DDR2-800
1	0	1	6	DDR2-800
1	1	0	7	DDR2-800
1	1	1	8	DDR2-800

$\overline{CAS}$ Latency

A6	A5	A4	Latency	
0	0	0	Reserved	
0	0	1	Reserved	
0	1	0	Reserved	
0	1	1	3	DDR2-1066
1	0	0	4	DDR2-1066
1	0	1	5	DDR2-1066
1	1	0	6	DDR2-1066
1	1	1	7	DDR2-1066

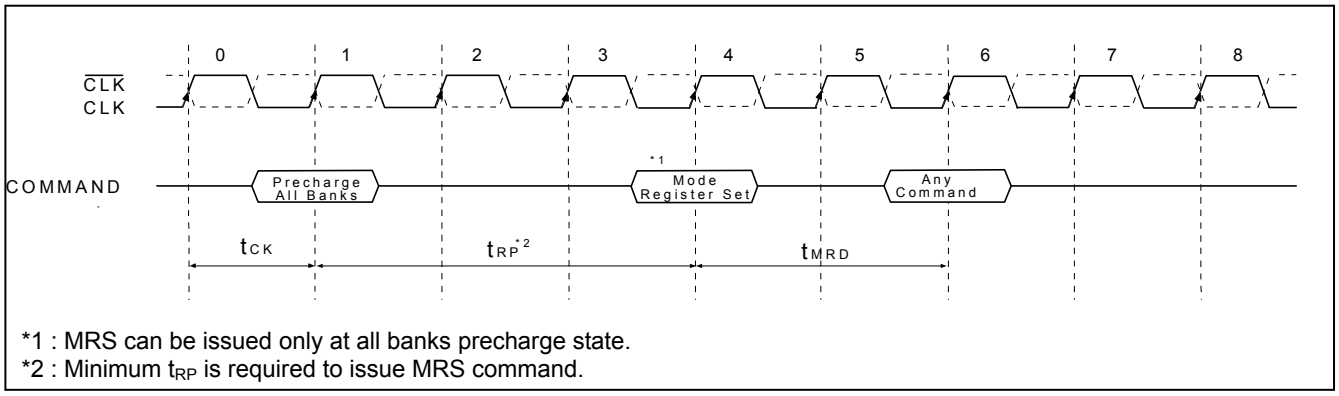
Note:

1. WR(min.) (write recovery for Auto Precharge) is determined by t_{CK} (max.) and WR(max.) is determined by t_{CK} (min.) WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up a non-integer value to the next integer (WR[cycles] = t_{WR} (ns)/ t_{CK} (ns)). The mode register must be programmed to this value. This is also used with t_{RP} to determine t_{DAL}.
2. If t_{CK} < 1.875ns, the device can not support Write with Auto Precharge function. WR must be set A11~A9 to 000.

Burst Address Ordering for Burst Length

Burst Length	Starting Column Address (A2, A1,A0)	Sequential Mode	Interleave Mode
4	000	0, 1, 2, 3	0, 1, 2, 3
	001	1, 2, 3, 0	1, 0, 3, 2
	010	2, 3, 0, 1	2, 3, 0, 1
	011	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Mode Register Set



*1 : MRS can be issued only at all banks precharge state.
*2 : Minimum t_{RP} is required to issue MRS command.

DLL Enable / Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having the DLL disabled for the purpose of debug or evaluation (upon exiting Self Refresh Mode, the DLL is enabled automatically). Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

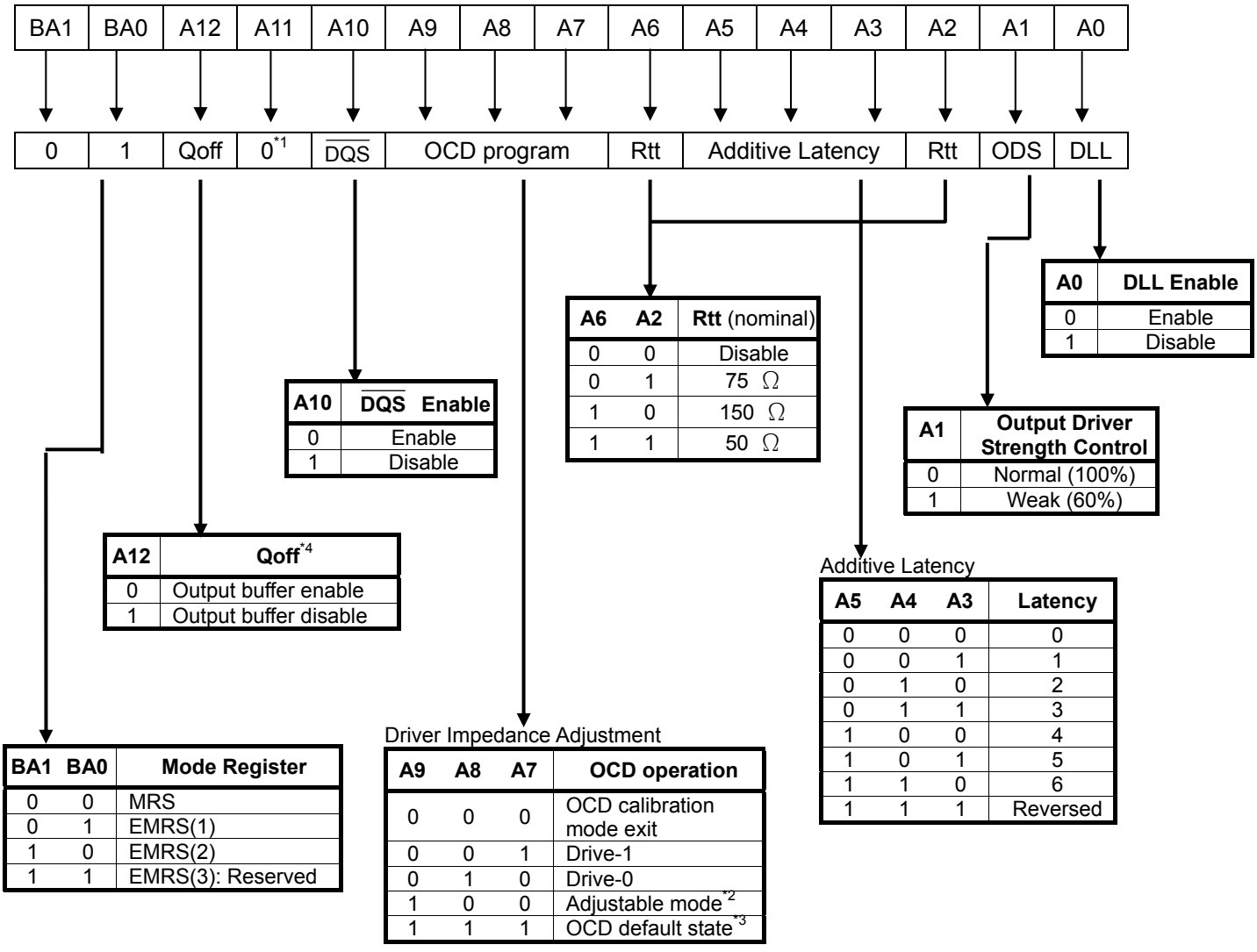
The normal drive strength for all outputs is specified to be SSTL_18. The device also supports a weak drive strength option, intended for lighter load and/or point-to-point environments.

Extended Mode Register Set-1 [EMRS(1)]

The EMRS(1) stores the data for enabling or disabling DLL, output driver strength, additive latency, ODT, disable $\overline{DQS}$, OCD program. The default value of the EMRS(1) is not defined, therefore EMRS(1) must be written after power up for proper operation. The EMRS(1) is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and HIGH on BA0 (The device should be in all bank Precharge with CKE already high prior to writing into EMRS(1)). The state of address pins A0~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA1 going LOW and BA0 going HIGH are written in the EMRS(1).

The t_{MRD} time is required to complete the write operation to the EMRS(1). The EMRS(1) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. A1 is used for reducing output driver strength. The additive latency is defined by A3~A5. A7~A9 are used for OCD control. A10 is used for $\overline{DQS}$ disable. ODT setting is defined by A2 and A6.

In single ended mode, the $\overline{DQS}$ signals are internally disabled and don't care.



A0	DLL Enable
0	Enable
1	Disable

A6	A2	Rtt (nominal)
0	0	Disable
0	1	75 Ω
1	0	150 Ω
1	1	50 Ω

A10	DQS Enable
0	Enable
1	Disable

A1	Output Driver Strength Control
0	Normal (100%)
1	Weak (60%)

A12	Qoff*4
0	Output buffer enable
1	Output buffer disable

Additive Latency

A5	A4	A3	Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	Reversed

BA1	BA0	Mode Register
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3): Reserved

Driver Impedance Adjustment

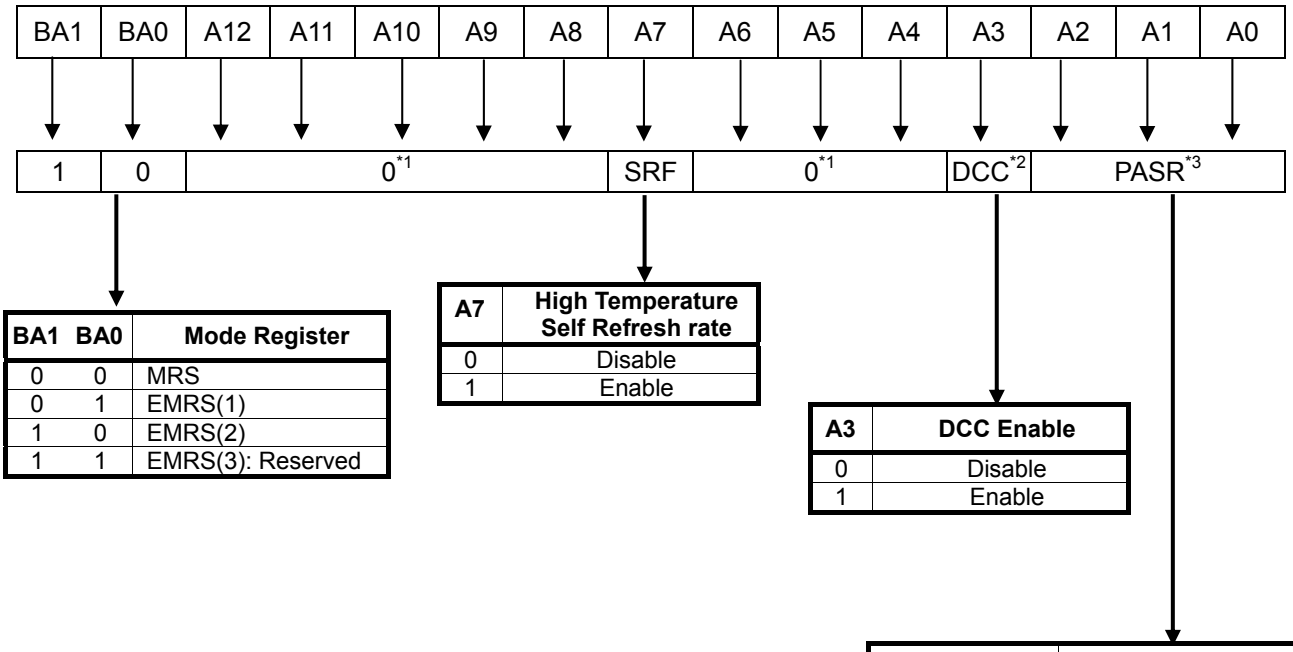
A9	A8	A7	OCD operation
0	0	0	OCD calibration mode exit
0	0	1	Drive-1
0	1	0	Drive-0
1	0	0	Adjustable mode*2
1	1	1	OCD default state*3

Note:

1. A11 is reserved for future use and must be set to 0.
2. When adjustable mode of driver impedance is issued, the previously set value of AL must be applied.
3. After setting to default state of driver impedance, OCD calibration mode needs to be exited by setting A9~A7 to 000.
4. Output disabled - DQs, DQSs, $\overline{DQS}$ s. This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.

Extended Mode Register Set-2 [EMRS(2)]

The EMRS(2) stores the data for enabling or disabling high temperature self refresh rate. The default value of the EMRS(2) is not defined, therefore EMRS(2) must be written after power up for proper operation. The EMRS(2) is written by asserting LOW on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and HIGH on BA1 (The device should be in all bank Precharge with CKE already high prior to writing into EMRS(2)). The state of address pins A0~A12 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 going LOW and BA1 going HIGH are written in the EMRS(2).
The t_{MRD} time is required to complete the write operation to the EMRS(2). The EMRS(2) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the idle state. A7 is used for high temperature self refresh rate enable or disable.



BA1	BA0	Mode Register
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3): Reserved

A7	High Temperature Self Refresh rate
0	Disable
1	Enable

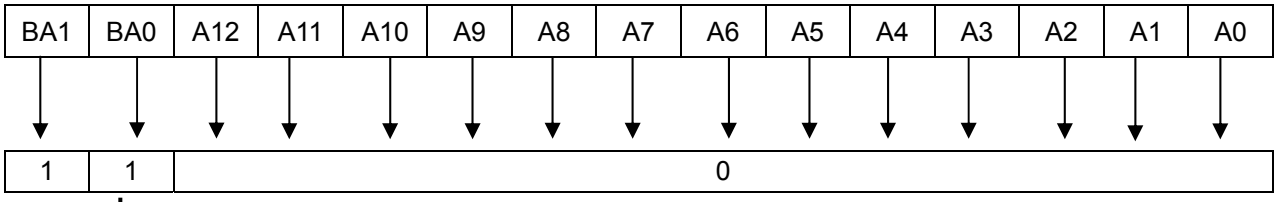
A3	DCC Enable
0	Disable
1	Enable

A2	A1	A0	Partial Array Self Refresh
0	0	0	Full Array
0	0	1	Half Array (BA[1:0]=00&01)
0	1	0	Quarter Array (BA[1:0]=00)
0	1	1	Not defined
1	0	0	3/4 Array (BA[1:0]=01, 10&11)
1	0	1	Half Array (BA[1:0]=10&11)
1	1	0	Quarter Array (BA[1:0]=11)
1	1	1	Not defined

***Note:**

1. A0~A2, A4~A6 and A8~A12 are reserved for future use and must be set to 0.
2. User may enable or disable the DCC (Duty Cycle Corrector) by programming A3 bit accordingly.
3. If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self refresh is entered. Data integrity will be maintained if t_{REF} conditions are met and no Self Refresh command is issued. If the PASR feature is not supported, EMRS(2)[A0-A2] must be set to 000 when programming EMRS(2).

Extended Mode Register Set-3 [EMRS(3)]



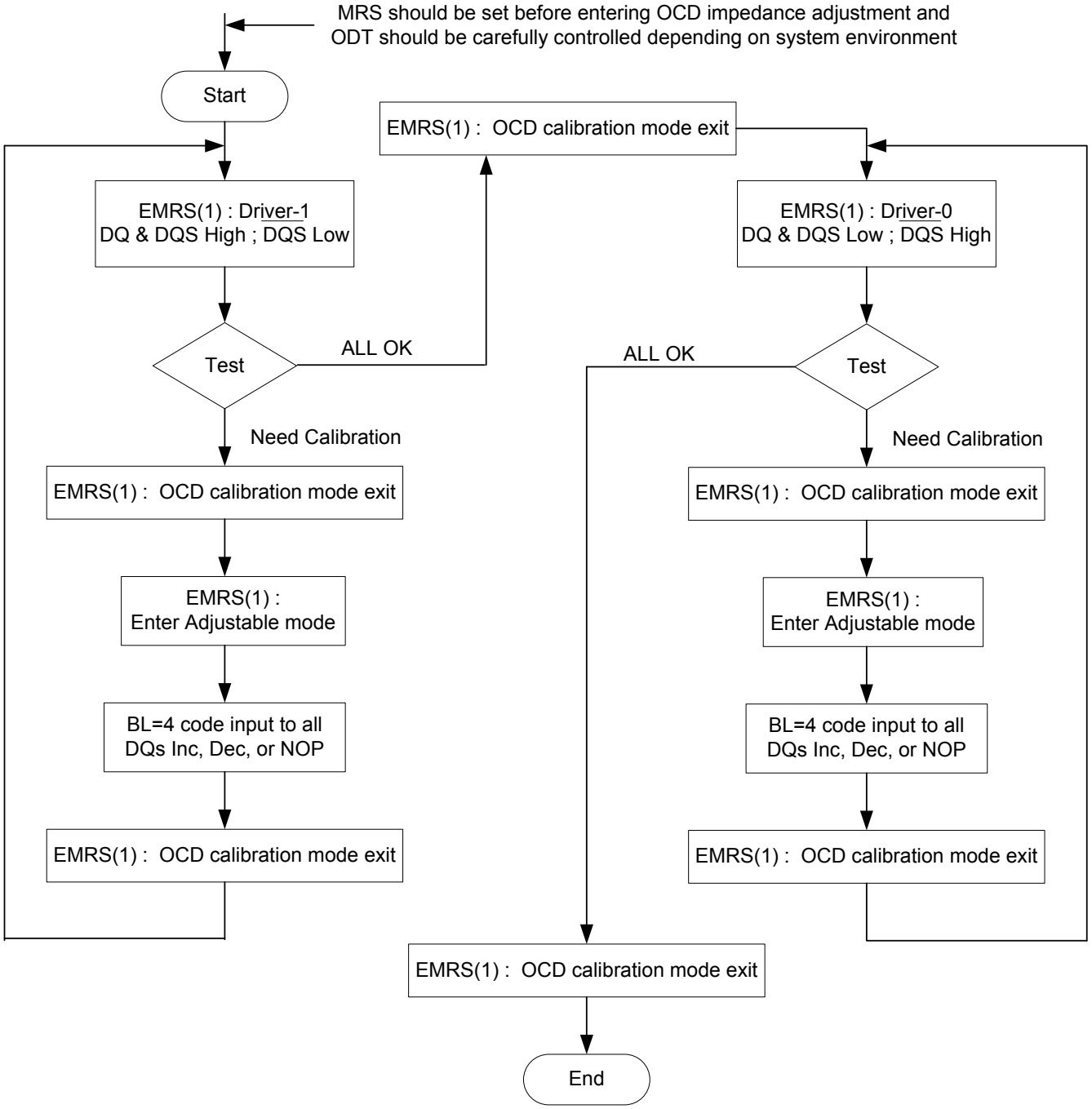
BA1	BA0	Mode Register
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2)
1	1	EMRS(3): Reserved

Note: EMRS(3) is reserved for future. All bits except BA0 and BA1 are reserved for future use and must be set to 0 when setting to mode register during initialization.

Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.

OCD Flow Chart



EMRS(1) for OCD Impedance Adjustment

OCD impedance adjustment can be done using the following EMRS(1) mode. In drive mode, all outputs are driven out by DDR2 SDRAM. In Drive-1mode, all DQ, DQS signals are driven HIGH and all $\overline{DQS}$ signals are driven LOW. In Drive-0 mode, all DQ, DQS signals are driven LOW and all $\overline{DQS}$ signals are driven HIGH. In adjustable mode, BL = 4 of operation code data must be used. In case of OCD default state, output driver characteristics have a nominal impedance value of 18 Ω during nominal temperature and voltage conditions. Output driver characteristics for OCD default state are specified in OCD default characteristics table. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if weak strength is set or adjustable mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS(1) commands not intended to adjust OCD characteristics must specify A9-A7 as '000' in order to maintain the default or calibrated value.

Driver Impedance Adjustment Mode

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Device-1: DQ,DQS High and $\overline{DQS}$ Low
0	1	0	Device-0: DQ,DQS Low and $\overline{DQS}$ High
1	0	0	Adjustable mode
1	1	1	OCD default state

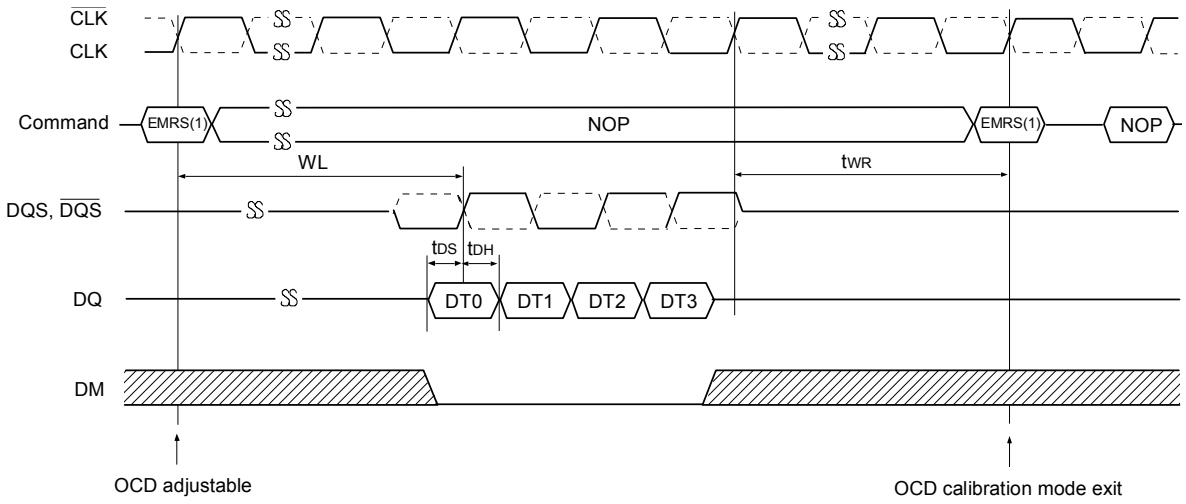
Adjust OCD Impedance

To adjust output driver impedance, controllers must issue EMRS(1) command for adjustable mode along with a 4bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in the following table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DQs simultaneously and after OCD calibration, all DQs of a given device will be adjusted to the same driver strength setting.
The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjustable mode command is issued, AL from previously set value must be applied.

OCD Adjustment Table

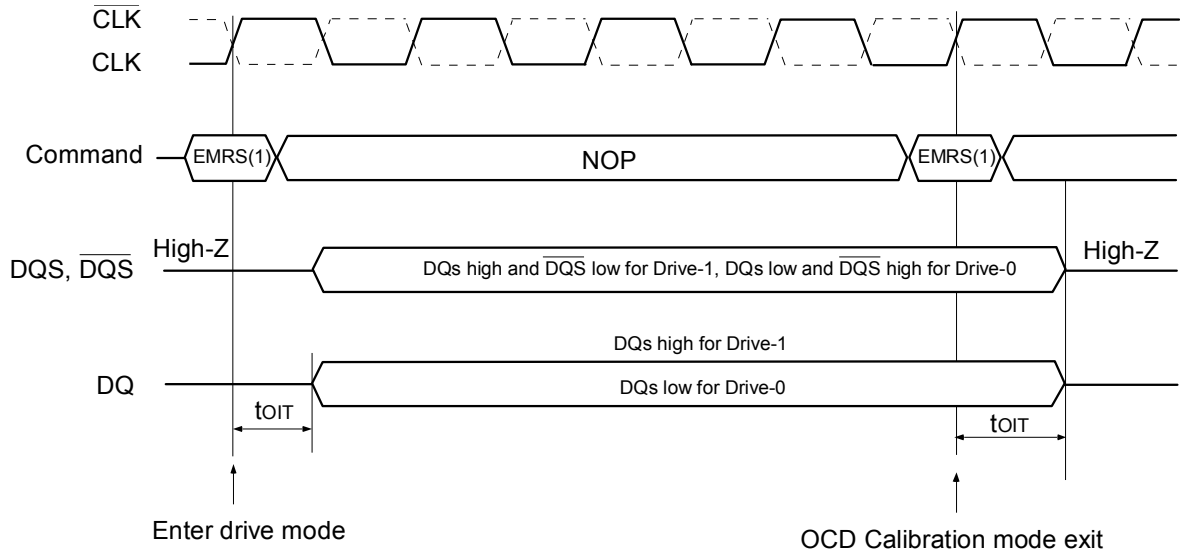
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP	NOP
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Others				Reserve	Reserve

OCD Adjustable Mode



Note: For proper operation of adjustable mode, WL = RL - 1 = AL + CL - 1 clocks and t_{DS} / t_{DH} should be met as the above timing diagram. For input data pattern for adjustment, DT0 - DT3 is a fixed order and "not affected by MRS addressing mode (ie. sequential or interleave).

OCD Driver Mode

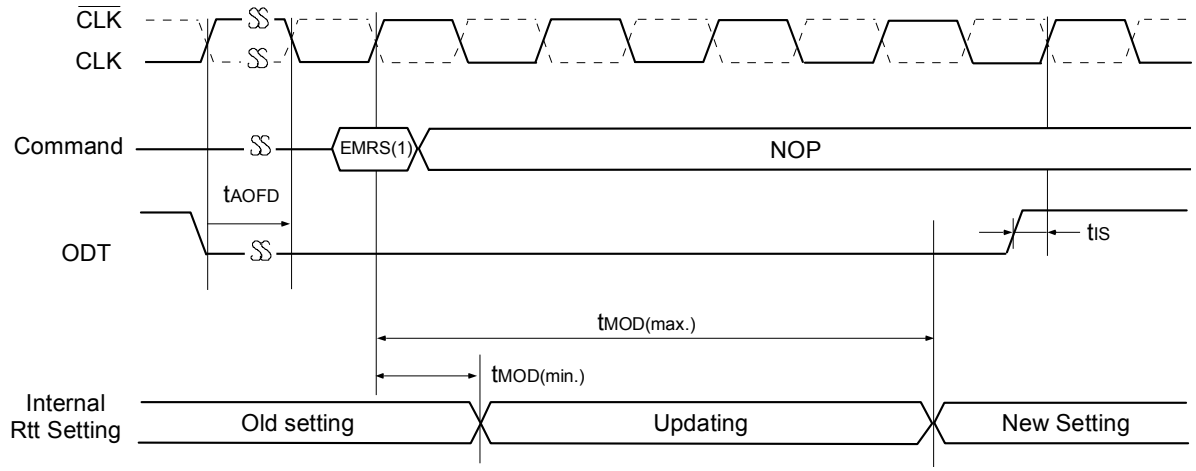


Note: Drive mode, both Drive-1 and Drive-0, is used for controllers to measure DDR2 SDRAM driver impedance. In this mode, all outputs are driven out t_{OIT} after "enter drive mode" command and all output drivers are turned-off t_{OIT} after "OCD calibration mode exit" command as the above timing diagram.

ODT (On Die Termination)

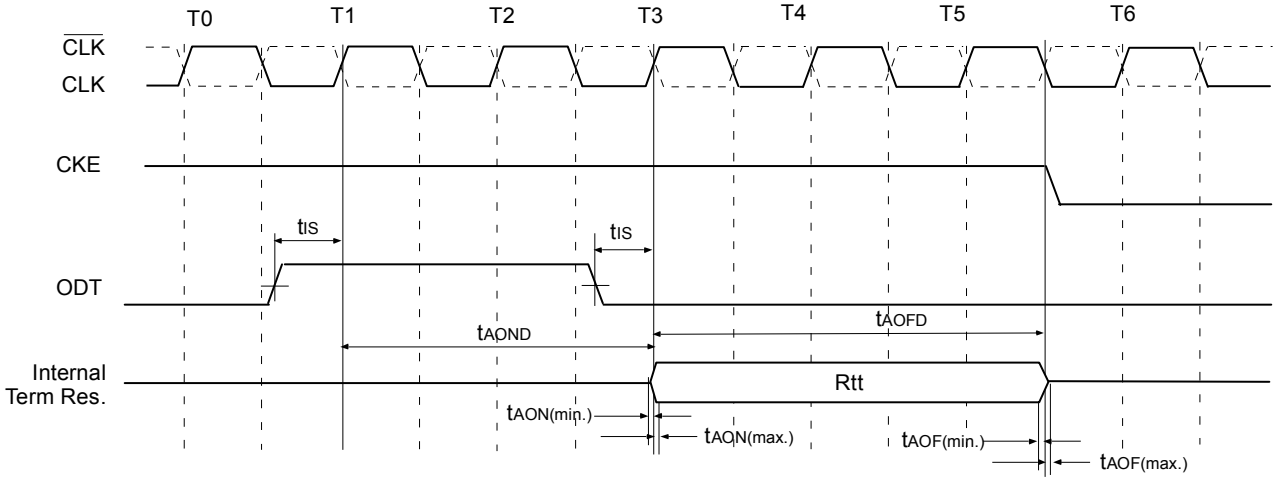
On Die Termination (ODT) is a feature that allows a DDR2 SDRAM to turn on/off termination resistance for each DQ, all DQS/$\overline{\text{DQS}}$, and all DM signals via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all devices.
The ODT function is supported for Active and Standby modes. ODT is turned off and not supported in Self Refresh mode.

Timing for ODT Update Delay

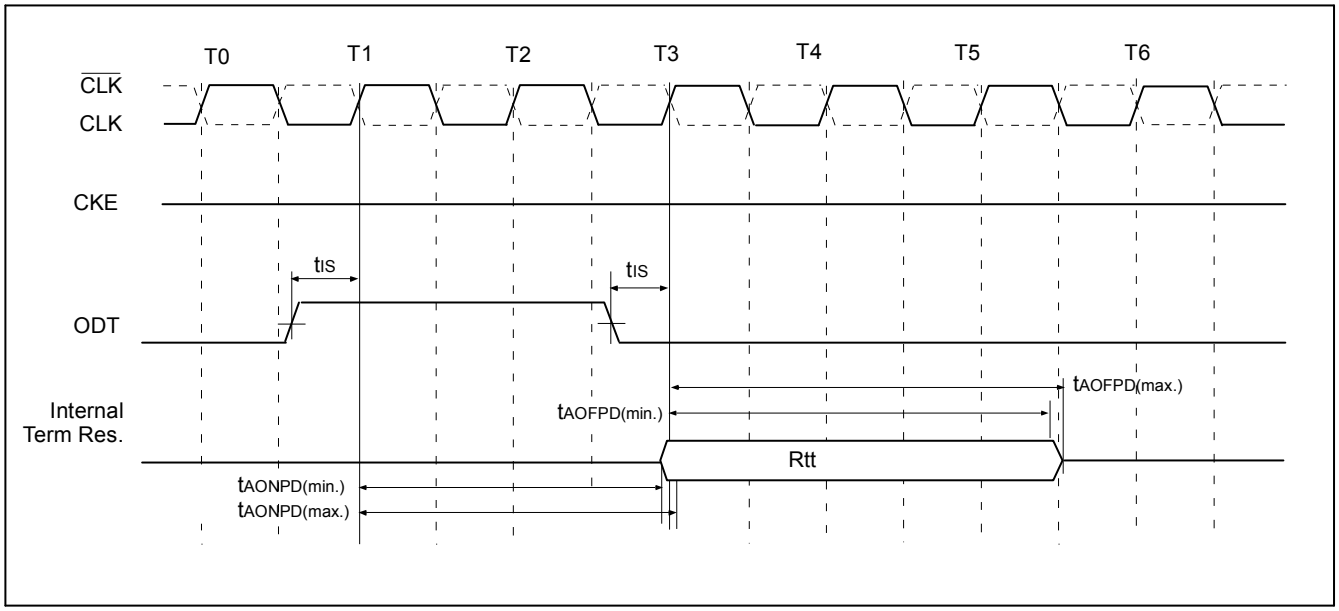


Note: t_{AOFD} must be met before issuing EMRS(1) command. ODT must remain low for the entire duration of t_{MOD} window.

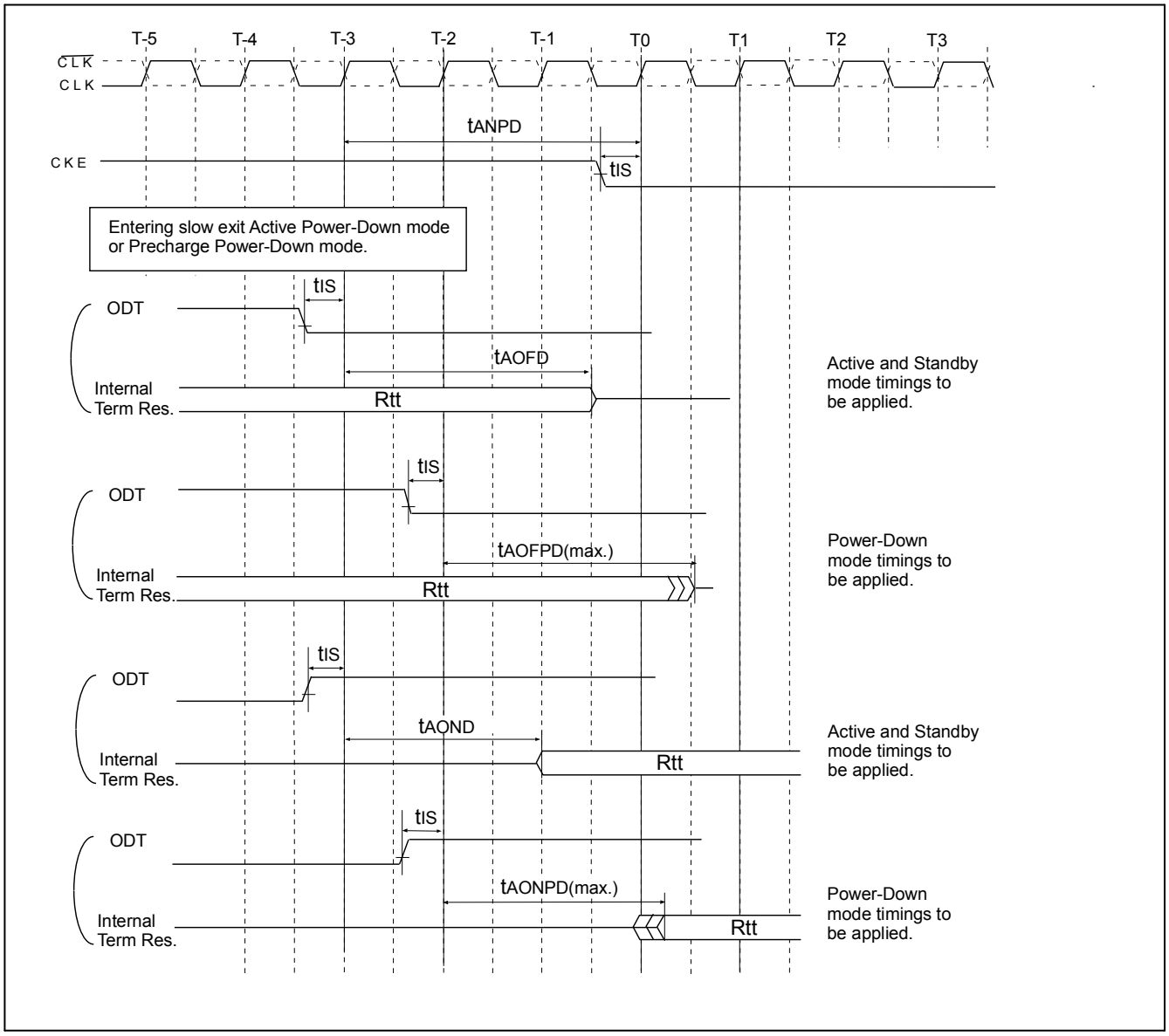
ODT Timing for Active and Standby Mode



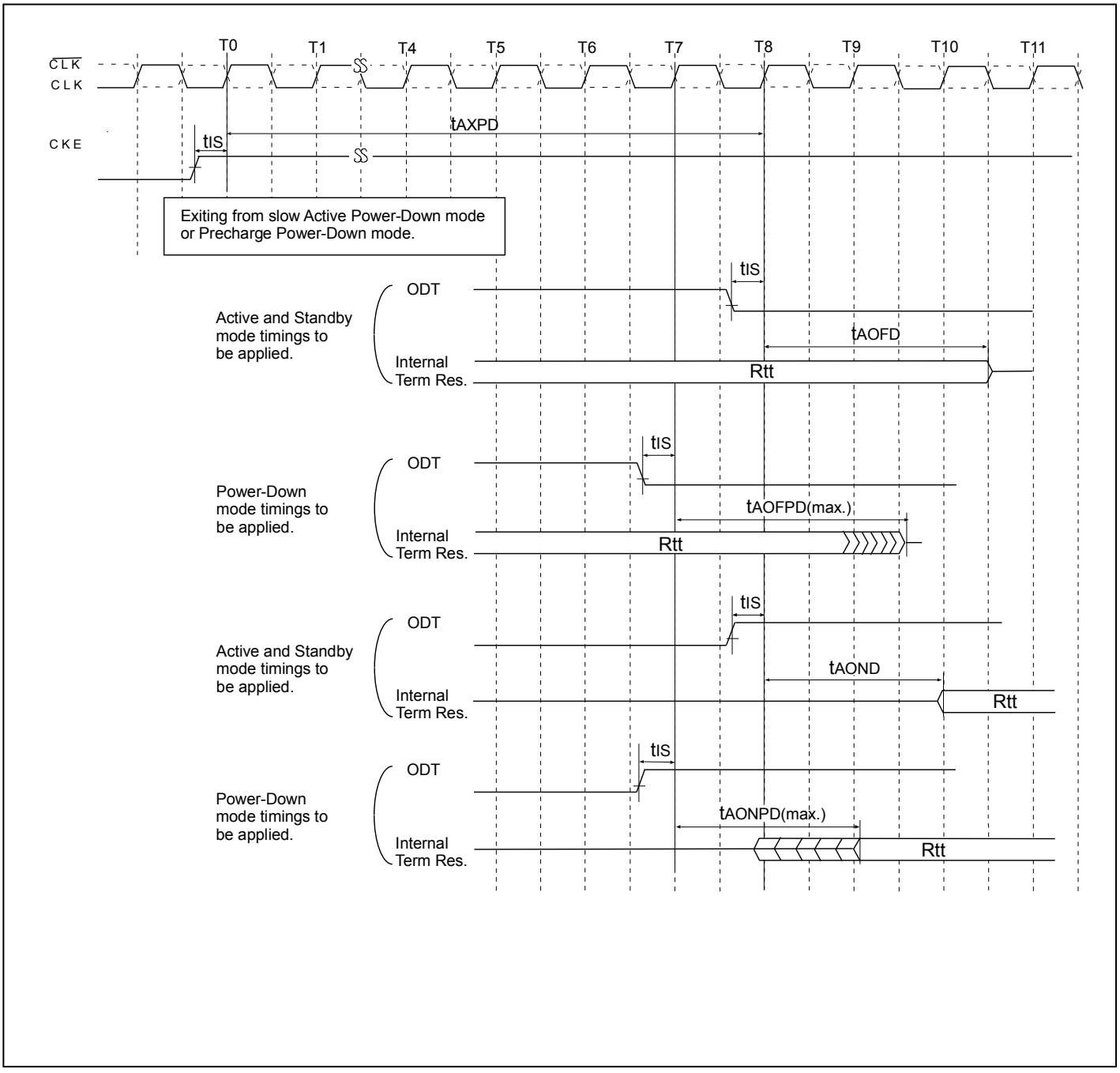
ODT Timing for Power-Down Mode



ODT Timing Mode Switch at Entering Power-Down Mode



ODT Timing Mode Switch at Exiting Power-Down Mode



Precharge

The Precharge command is used to precharge or close a bank that has activated. The command is issued when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are LOW and $\overline{CAS}$ is HIGH at the rising edge of the clock. The Precharge command can be used to precharge each bank respectively or all banks simultaneously. The bank select addresses (BA0, BA1) and A10 are used to define which bank is precharged when the command is initiated. For write cycle, t_{WR}(min.) must be satisfied until the Precharge command can be issued. After t_{RP} from the precharge, a Bank Active command to the same bank can be initiated.

Bank Selection for Precharge by Address bits

A10/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	1	0	Bank B Only
0	0	1	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

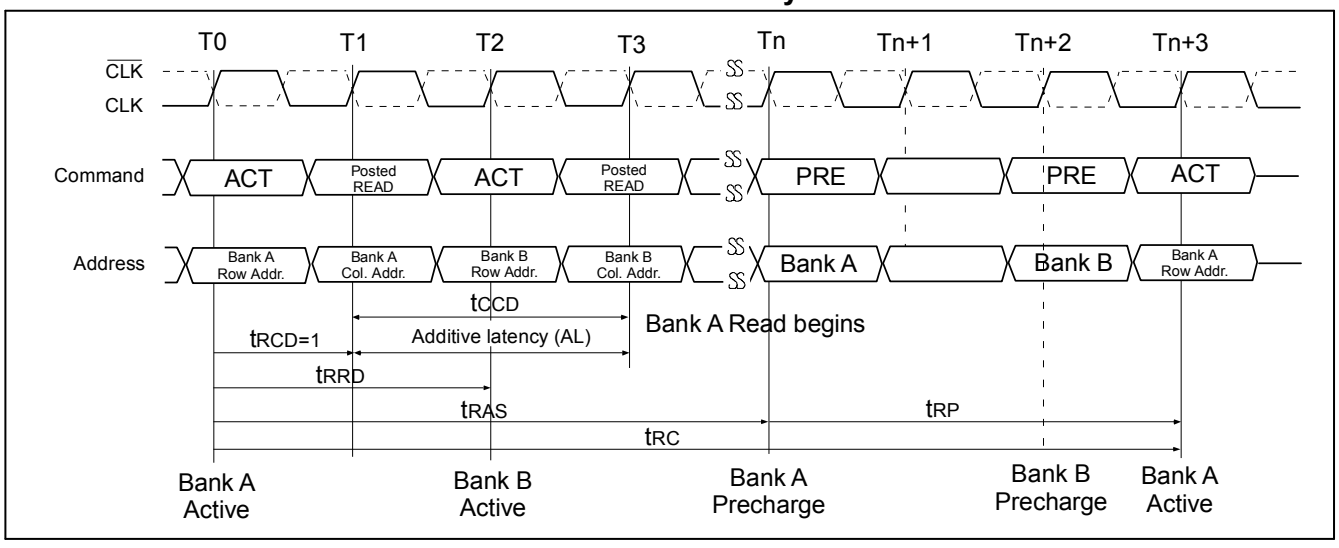
NOP & Device Deselect

The device should be deselected by deactivating the $\overline{CS}$ signal. In this mode, DDR2 SDRAM would ignore all the control inputs. The DDR2 SDRAM are put in NOP mode when $\overline{CS}$ is active and by deactivating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP, the device should finish the current operation when this command is issued.

Bank Active

The Bank Active command is issued by holding $\overline{CAS}$ and $\overline{WE}$ HIGH with $\overline{CS}$ and $\overline{RAS}$ LOW at the rising edge of the clock (CLK). The DDR2 SDRAM has four independent banks, so two Bank Select addresses (BA0, BA1) are required. The Bank Active command to the first Read or Write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD}(min.)). Once a bank has been activated, it must be precharged before another Bank Active command can be applied to the same bank. The minimum time interval between interleaved Bank Active command (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD} min).

Bank Active Command Cycle



Read Bank

This command is used after the Bank Active command to initiate the burst read of data. The Read command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the $\overline{CAS}$ latency time will be determined by the values programmed during the MRS command.

Write Bank

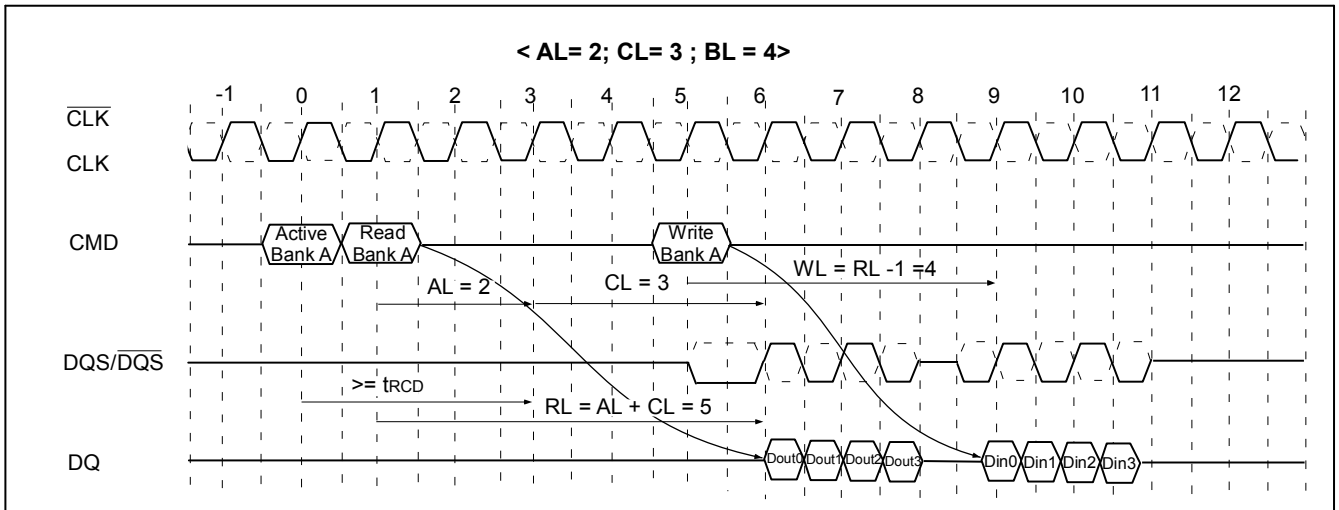
This command is used after the Bank Active command to initiate the burst write of data. The Write command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ at the same clock sampling (rising) edge as describe in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Posted $\overline{CAS}$

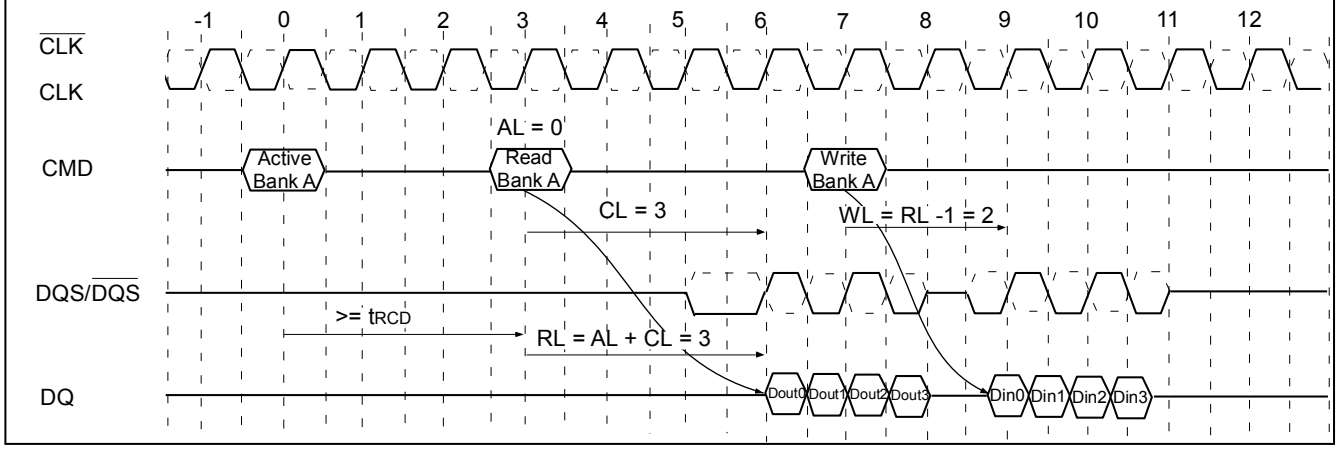
Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the Bank Active command (or any time during the t_{RRD} period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a R/W command before the t_{RCD}(min), then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus $\overline{CAS}$ latency (RL=AL+CL). Read or Write operations using AL allow seamless bursts.

Read followed by a Write to the Same Bank

< AL= 2; CL= 3 ; BL = 4>



< AL= 0; CL= 3; BL = 4 >



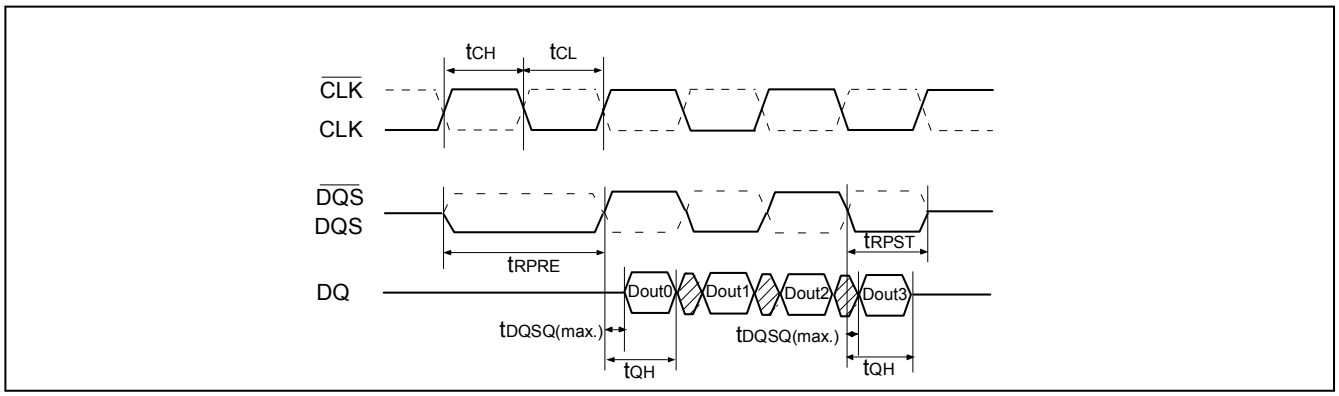
Essential Functionality for DDR2 SDRAM

Burst Read Operation

The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ LOW while holding $\overline{RAS}$ and $\overline{WE}$ HIGH at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The DQS is driven LOW 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of DQS. Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner.

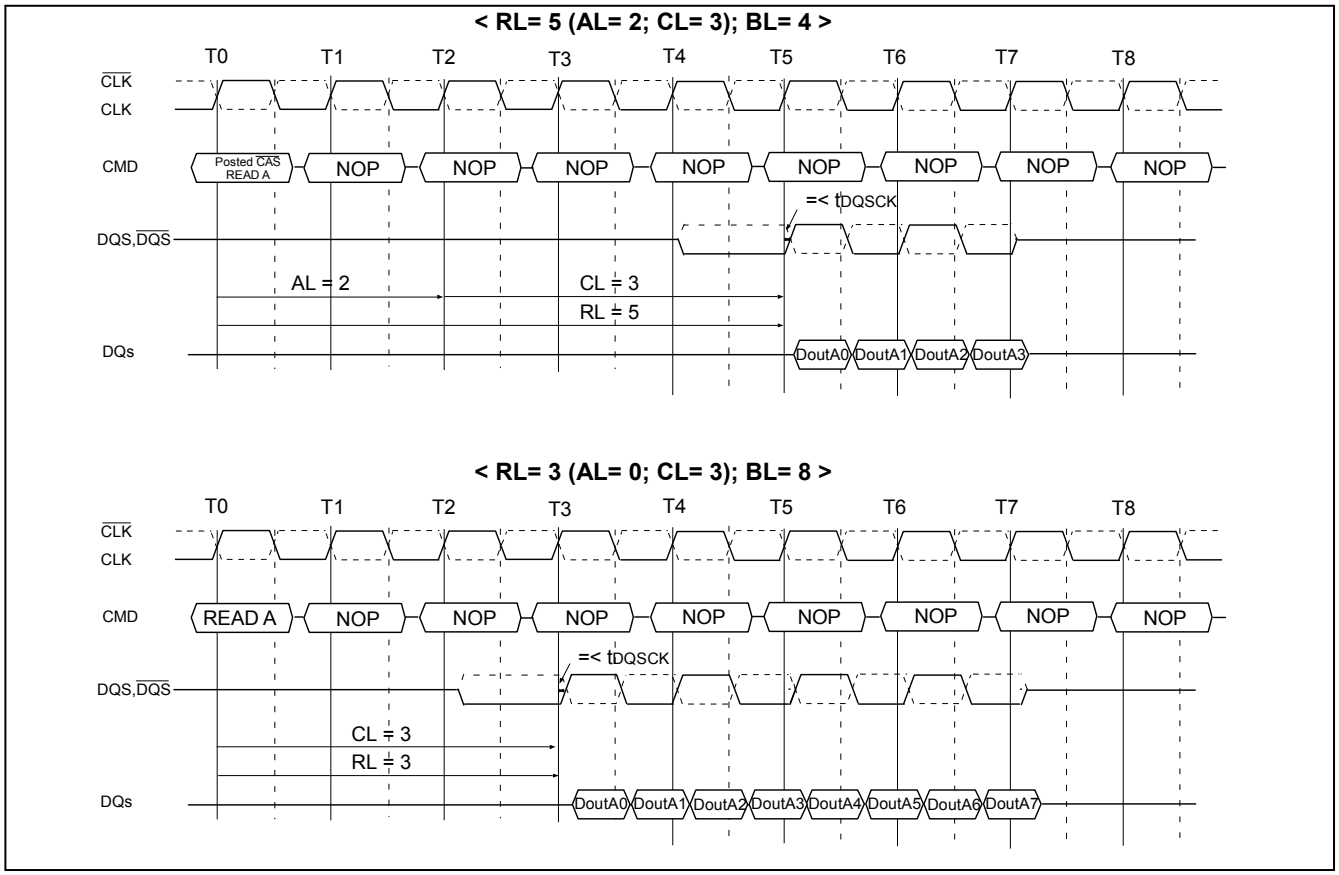
The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the MRS and the AL is defined by the EMRS(1).

Read (Data Output) Timing



Burst Read

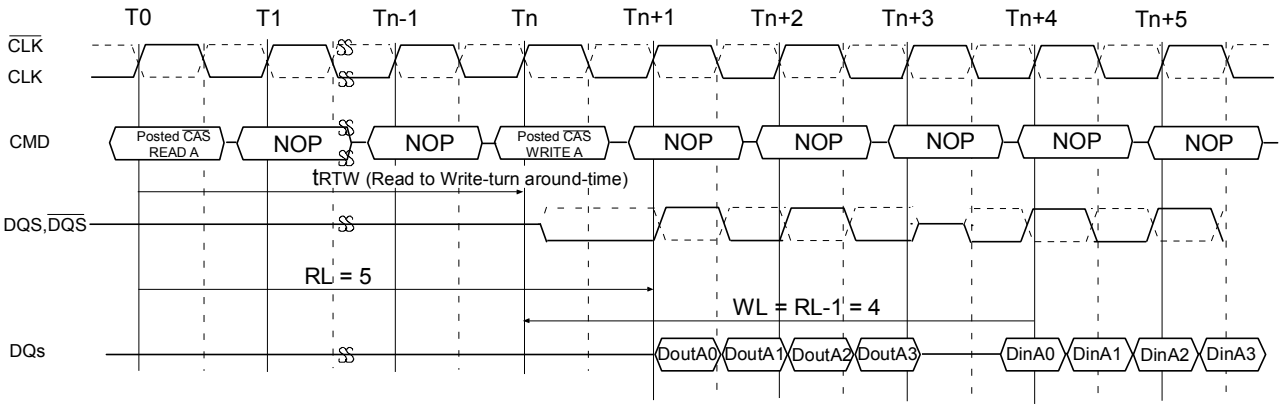
< RL= 5 (AL= 2; CL= 3); BL= 4 >



< RL= 3 (AL= 0; CL= 3); BL= 8 >

Burst Read followed by Burst Write

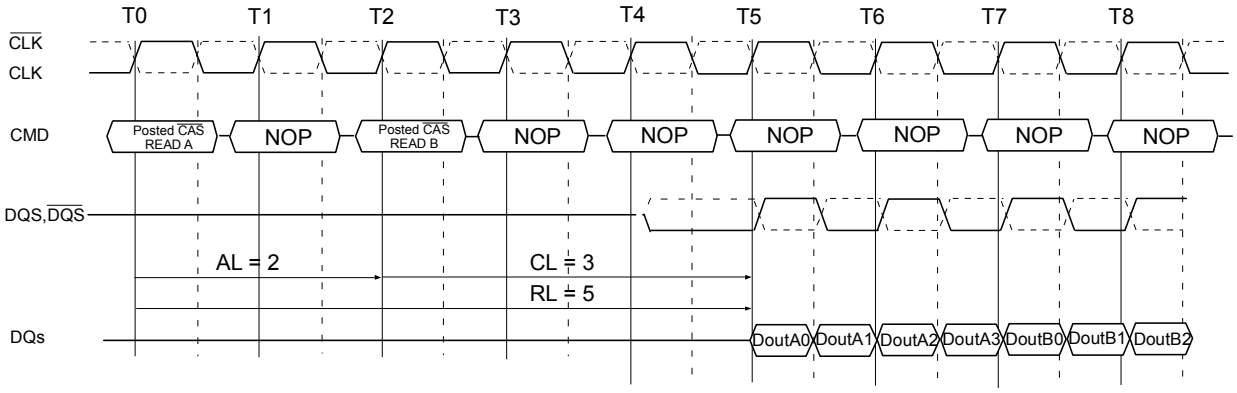
< RL= 5; WL= (RL-1) = 4; BL= 4 >



Note: The minimum time from the Burst Read command to the Burst Write command is defined by a read to write-turn around-time(t_{RTW}), which is 4 clocks in case of BL = 4 operation, 6 clocks in case of BL = 8 operation (8 clocks in case of BL = 4 operation, 16 clocks in case of BL = 8 operation for speed grade -1.3).

Seamless Burst Read

< RL= 5; AL= 2; CL= 3; BL = 4 >

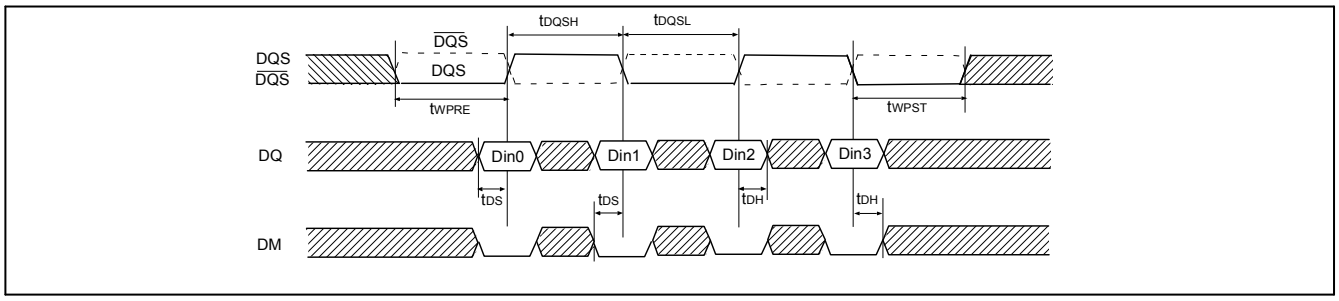


Note: The seamless burst read operation is supported by enabling a Read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

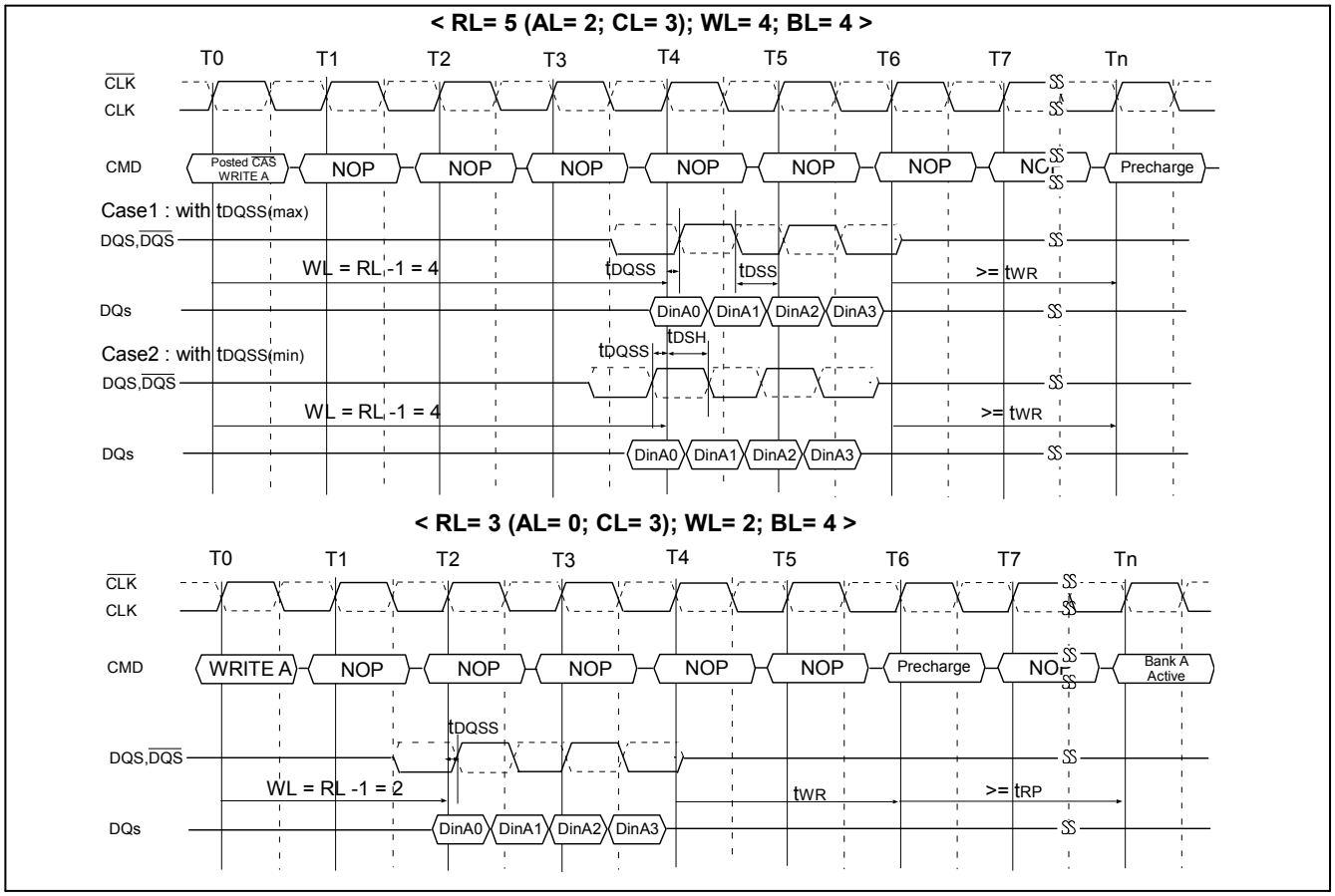
Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ LOW while holding $\overline{RAS}$ HIGH at the rising edge of the clock (CLK). The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (t_{WR}).

Write (Data Input) Timing

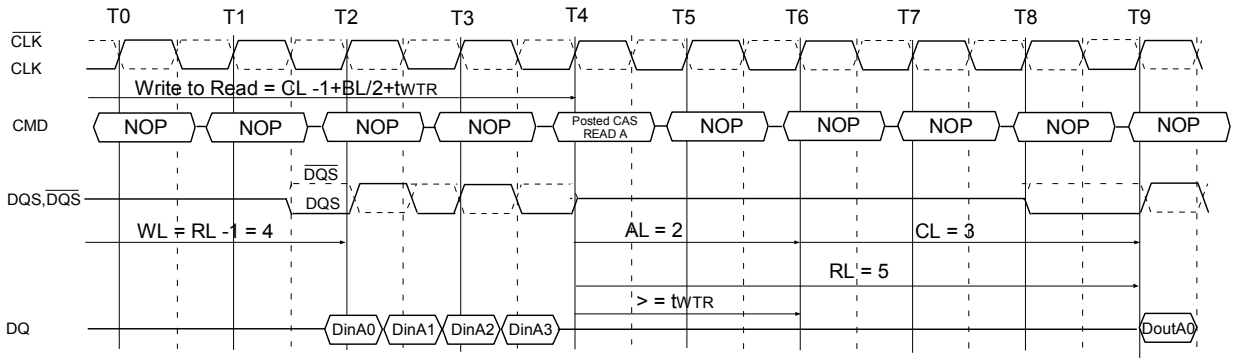


Burst Write



Burst Write followed by Burst Read

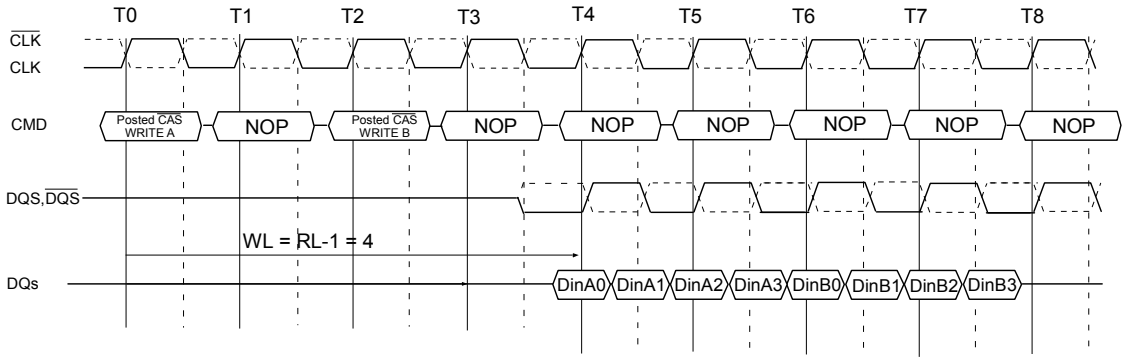
< RL= 5 (AL= 2; CL= 3); WL= 4; BL= 4 >



Note: The minimum number of clock from the Burst Write command to the Burst Read command is [CL - 1 + BL/2 + t_{WTR}]. This t_{WTR} is not a write recovery time (WR) but the time required to transfer the 4 bit write data from the input buffer into sense amplifiers in the array.

Seamless Burst Write

< RL= 5; WL= 4; BL= 4 >

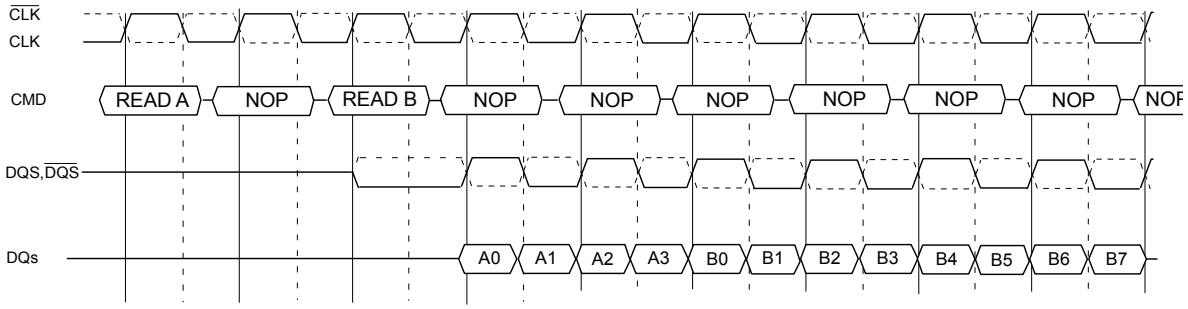


Note: The seamless burst write operation is supported by enabling a Write command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Read Interrupted by a Read

Burst Read can only be interrupted by another read with 4 bit burst boundary. Any other case of read interrupt is not allowed.

< CL= 3; AL= 0; RL= 3; BL= 8 >



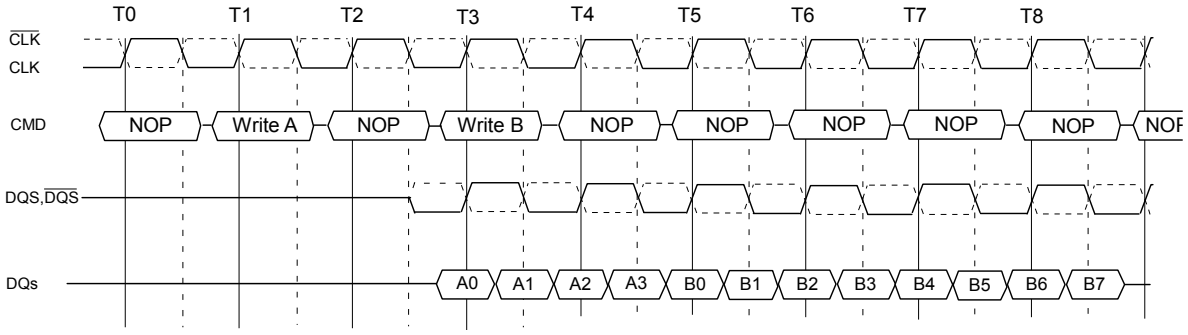
Note:

1. Read burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write command or Precharge command is prohibited.
3. Read burst interrupt must occur exactly two clocks after previous Read command. Any other Read burst interrupt timings are prohibited.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto Precharge enabled is not allowed to interrupt.
6. Read burst interruption is allowed by another Read with Auto Precharge command.
7. All command timings are referenced to burst length set in the mode register. They are not referenced to actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the MRS and not the actual burst (which is shorter because of interrupt).

Write Interrupted by a Write

Burst Wirte can only be interrupted by another Write with 4 bit burst boundary. Any other case of Write interrupt is not allowed.

< CL= 3; AL= 0; RL= 3; WL= 2; BL= 8 >



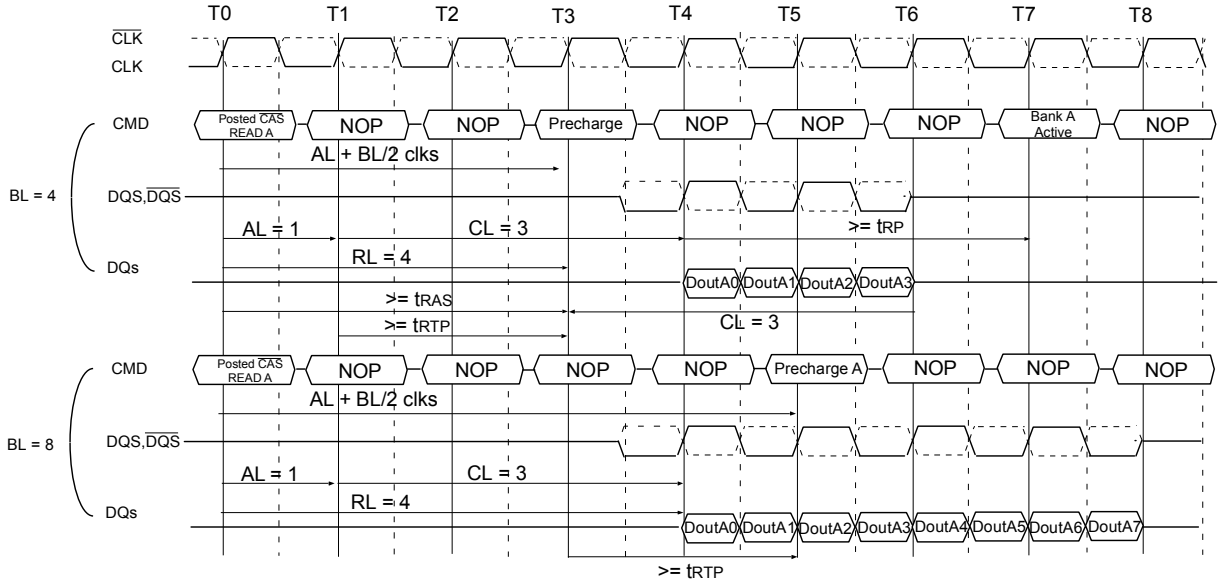
Note:

1. Write burst interrupt function is only allowed on burst of 8. Burst interrupt of 4 is prohibited.
2. Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read command or Precharge command is prohibited.
3. Write burst interrupt must occur exactly two clocks after previous Write command. Any other Write burst interrupt timings are prohibited.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto Precharge enabled is not allowed to interrupt.
6. Write burst interruption is allowed by another Write with Auto Precharge command.
7. All command timings are referenced to burst length set in the MRS. They are not referenced to actual burst. For example, minimum Write to Precharge timing is WL+BL/2+ t_{WR} where t_{WR} starts with the rising clock after the un-interrupted burst end and not from the end of actual burst end.

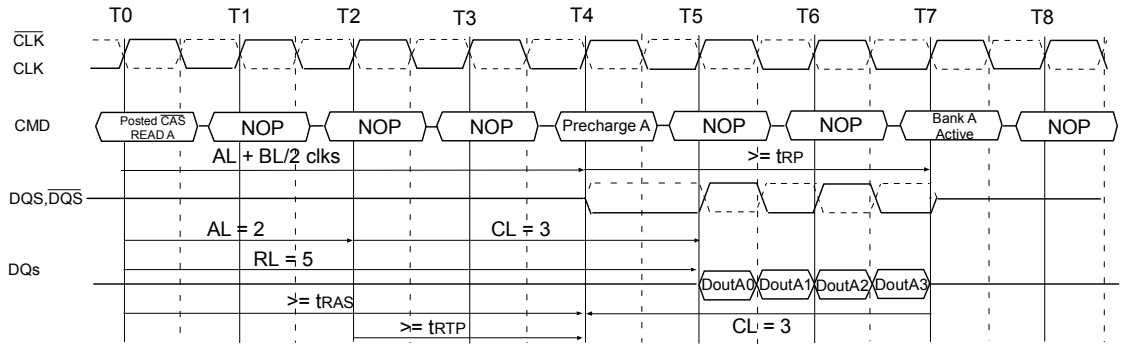
Burst Read Followed by Precharge

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 + max(t_{RTP}, 2) - 2 clocks.
For the earliest possible Precharge, the Precharge command may be issued on the rising edge which is "Additive latency (AL) + BL/2 clocks" after a Read command. A new Bank Active command may be issued to the same bank after the Precharge time (t_{RP}). A Precharge command cannot be issued until t_{RAS} is satisfied.
The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called t_{RTP} (Read to Precharge). For BL = 4, this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8, this is the time from AL + 2 clocks after the Read to the Precharge command.

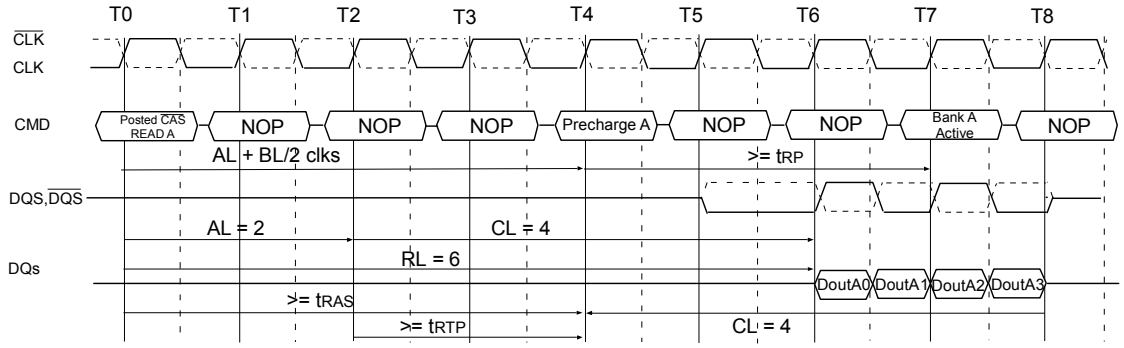
< RL= 4 (AL= 1; CL= 3) >

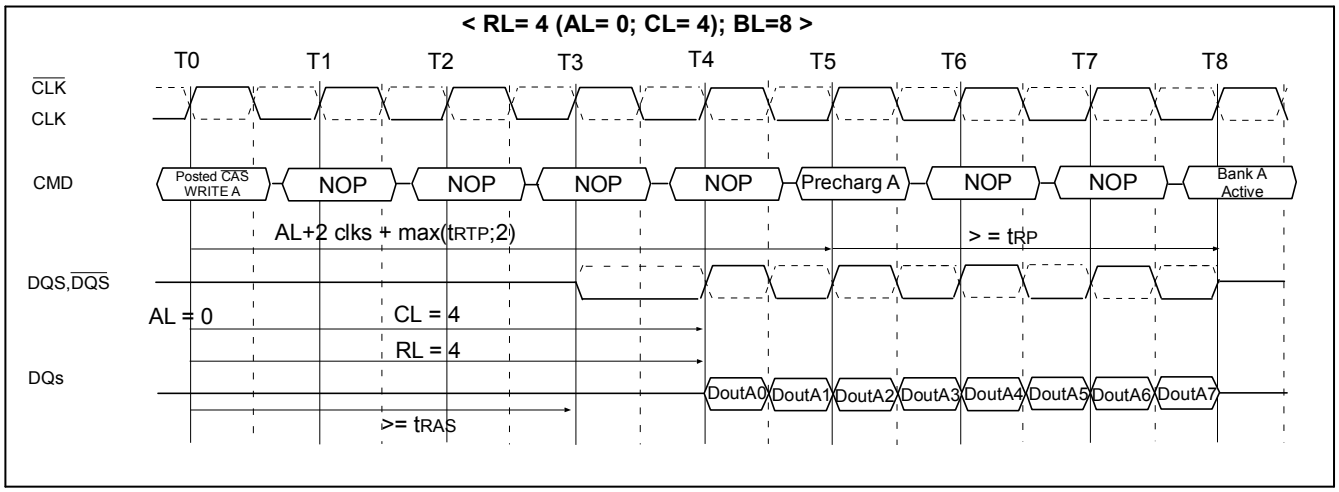


< RL= 5 (AL= 2; CL= 3); BL= 4 >



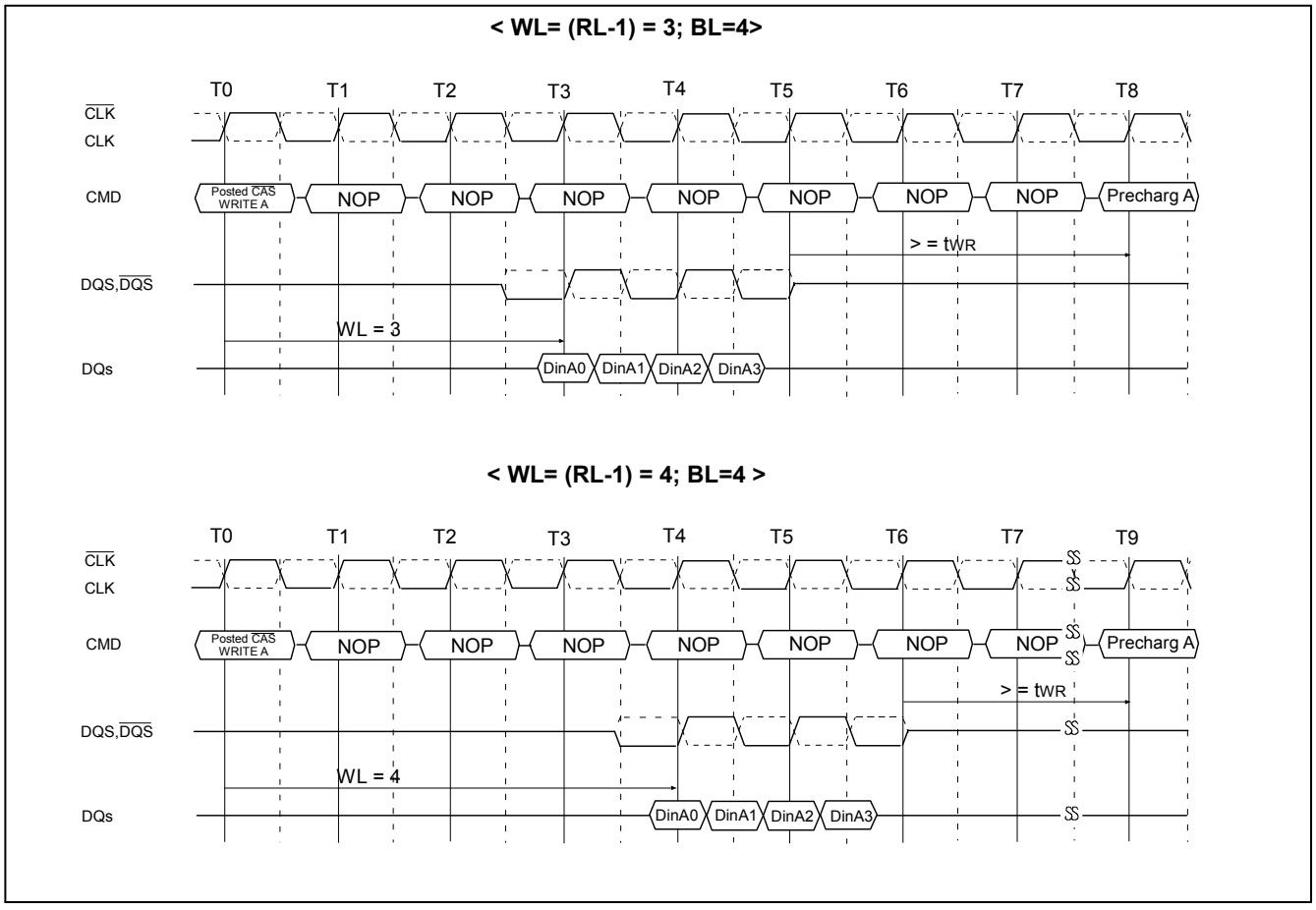
< RL= 6 (AL= 2; CL= 4); BL= 4 >





Burst Write Followed by Precharge

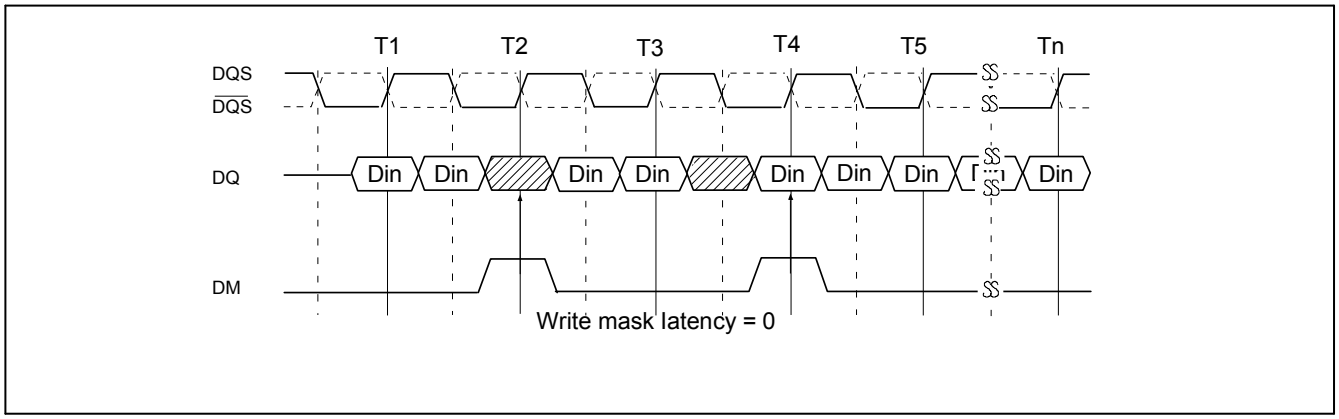
Minimum Write to Precharge command spacing to the same bank = WL + BL/2 clocks + t_{WR}.
For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t_{WR}) referenced from the completion of the Burst Write to the Precharge command. No Precharge command should be issued prior to the t_{WR} delay.

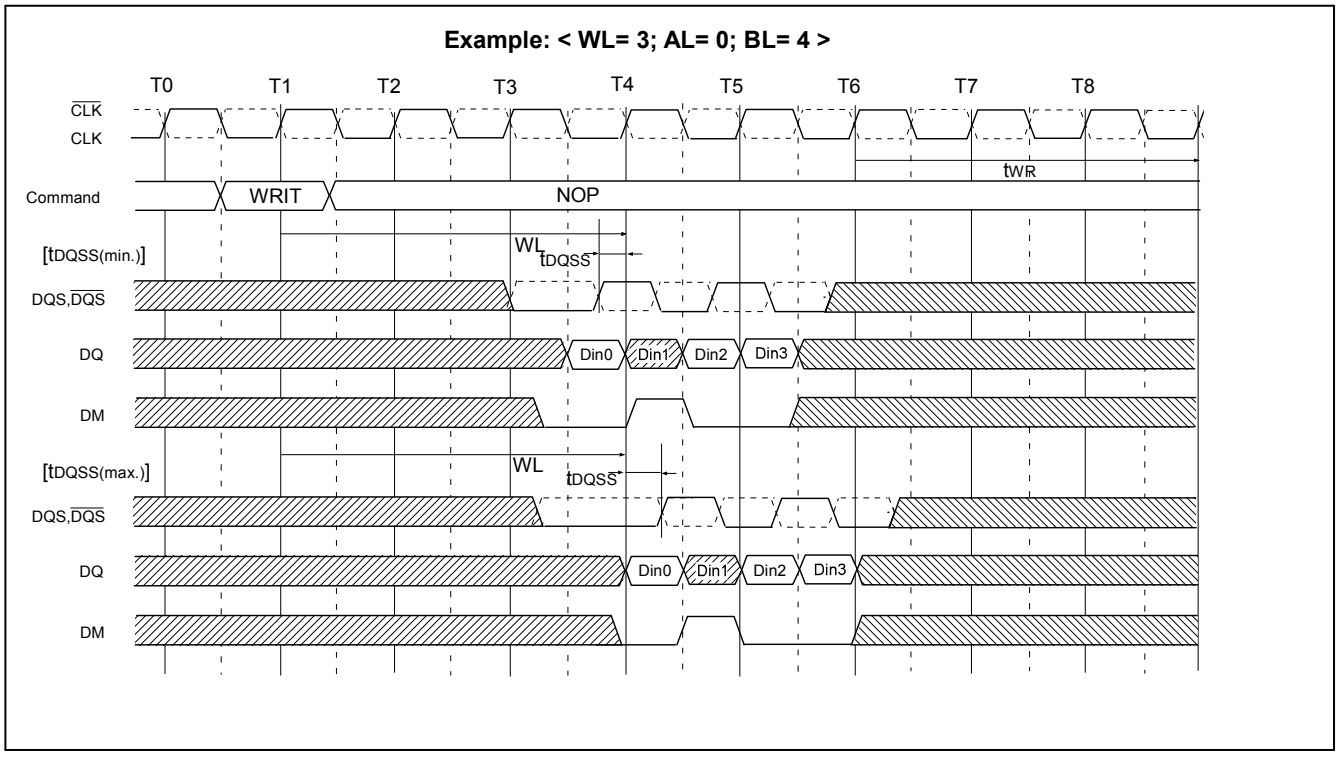


Write data mask by DM

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAM, Consistent with the implementation on DDR2 SDRAM. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM is not used during read cycles.

Data Mask Timing



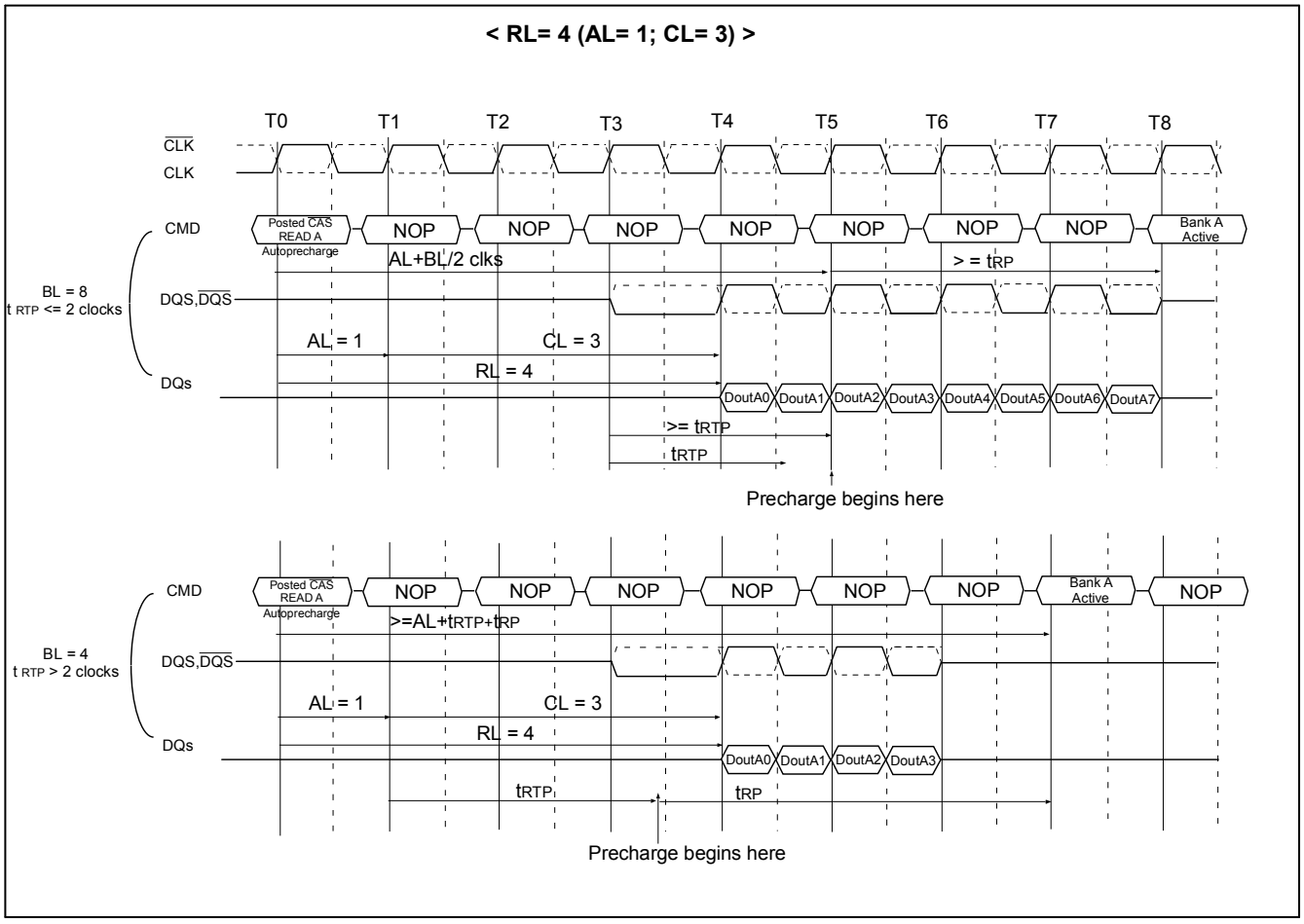


Read with Auto Precharge

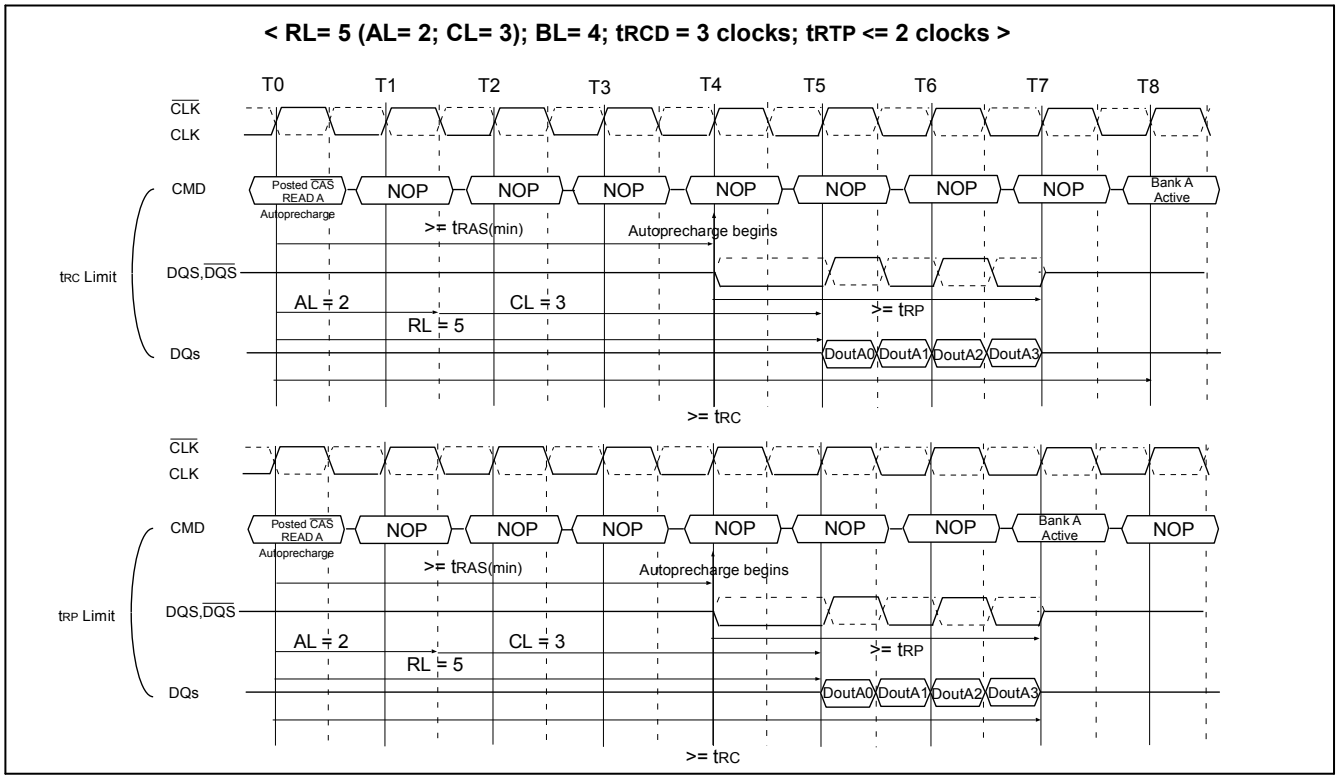
If A10 is HIGH when a Read command is issued, the Read with Auto Precharge function is engaged. The device starts an Auto Precharge operation on the rising edge which is (AL + BL/2) cycles later than the Read with AP command if t_{RAS} (min) and t_{RTP}(min) are satisfied.

If t_{RAS}(min) is not satisfied at the edge, the start point of Auto Precharge operation will be delayed until t_{RAS}(min) is satisfied.
If t_{RTP} (min) is not satisfied at the edge, the start point of Auto Precharge operation will be delayed until t_{RTP} (min) is satisfied.

In case the internal precharge is pushed out by t_{RTP}, t_{RP} starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4, the minimum time from Read_AP to the next Bank Active command becomes AL + (t_{RTP} + t_{RP})*. For BL = 8, the time from Read_AP to the next Bank Active command is AL + 2 + (t_{RTP} + t_{RP})*. (Note: "*" means "rouded up to the next integer").

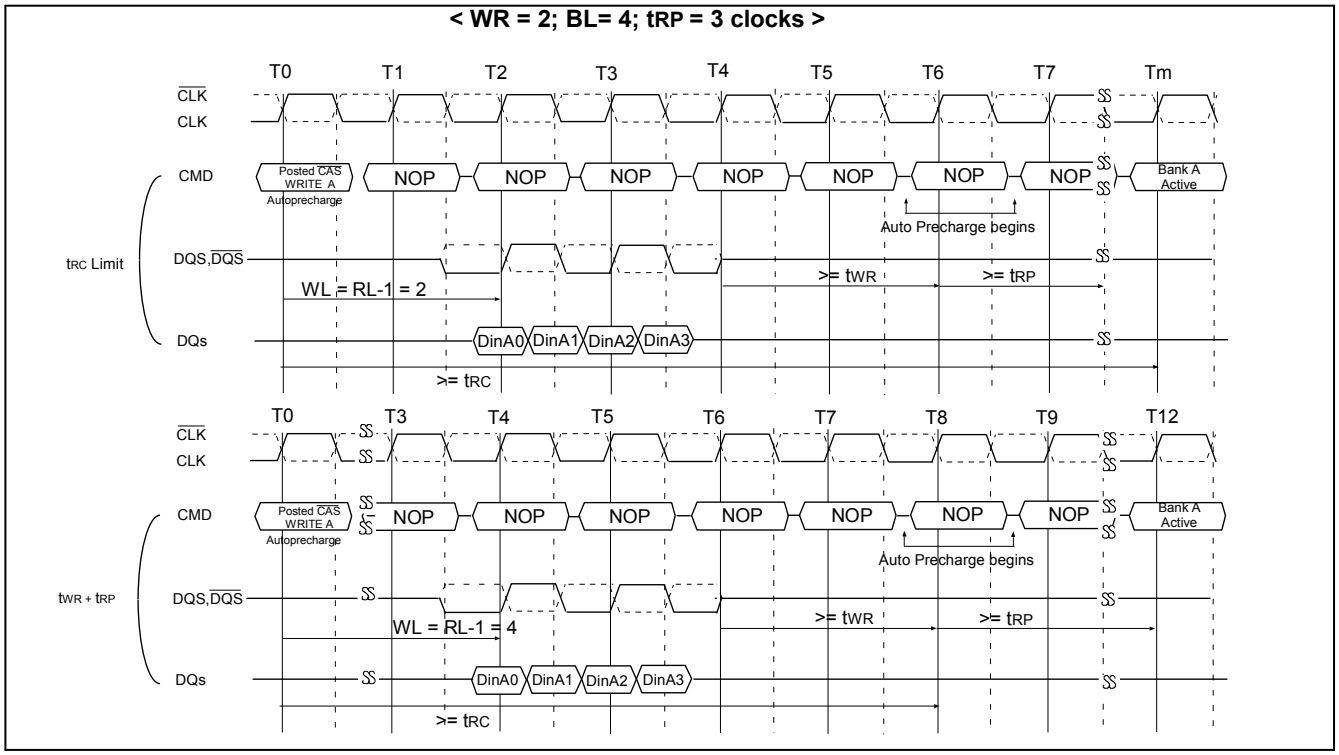


A new Bank Active command may be issued to the same bank if the following two conditions are satisfied simultaneously.
(1) The Precharge time (t_{RP}) has been satisfied from the clock at which the Auto Precharge begins.
(2) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.



Write with Auto Precharge

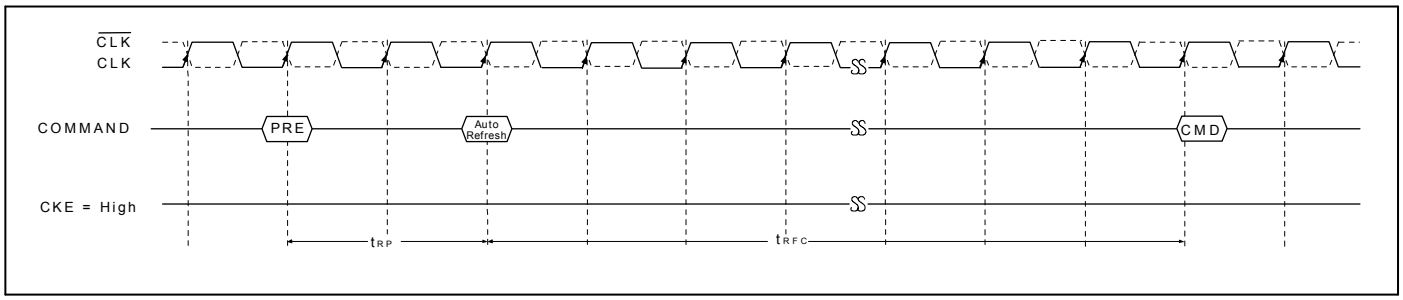
If A10 is HIGH when a Write command is issued, the Write with Auto Precharge function is engaged (If t_{CK} < 1.875ns, the device can not support Write with Auto Precharge function). The device automatically begins precharge operation after the completion of the burst write plus write recovery time (t_{WR}). The Bank Active command undergoing Auto Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.
(1) The data-in to bank activate delay time (t_{WR} + t_{RP}) has been satisfied.
(2) The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.



Auto Refresh & Self Refresh

Auto Refresh

An Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held LOW with CKE and $\overline{WE}$ HIGH at the rising edge of the clock(CLK). All banks must be precharged and idle for t_{RP}(min) before the Auto Refresh command is applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Bank Active command or subsequent Auto Refresh command must be greater than or equal to the t_{RFC}(min).To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x t_{REFI}.

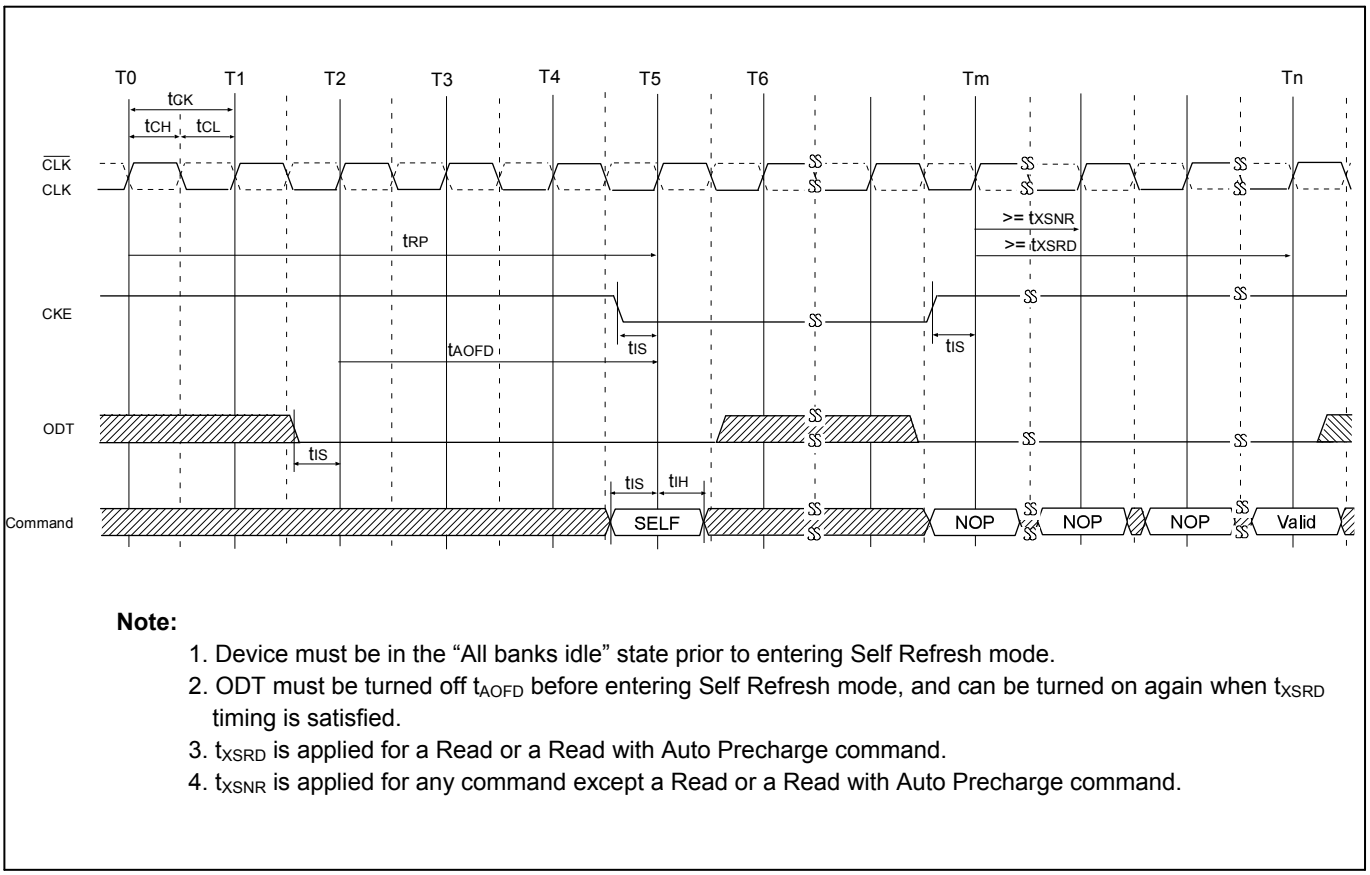


Self Refresh

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held LOW with $\overline{WE}$ HIGH at the rising edge of the clock (CLK). ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS(1) command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the device has entered Self Refresh mode, all of the external signals except CKE, are "don't care".

For proper Self Refresh operation all power supply pins (V_{DD}, V_{DDQ}, V_{DDL} and V_{REF}) must be at valid levels. The device initiates a minimum of one refresh command internally within t_{CKE} period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh operation to save power. Self Refresh mode must be remained t_{CKE} (min).

The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self Refresh operation. The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of t_{XSRD}(min) must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period t_{XSRD} for proper operation except for Self Refresh re-entry. Upon exit from Self Refresh, the device can be put back into Self Refresh mode after waiting t_{XSNR}(min) and issuing one Refresh command. NOP or deselect commands must be registered on each positive clock edge during the Self Refresh exit interval t_{XSNR}. ODT should be turned off during t_{XSRD}. The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the device requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

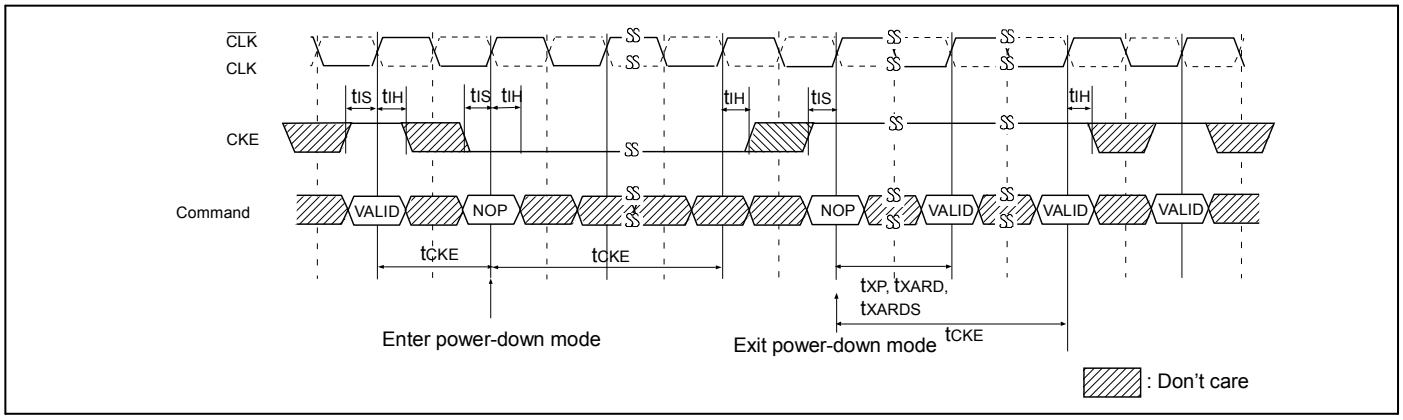


Note:

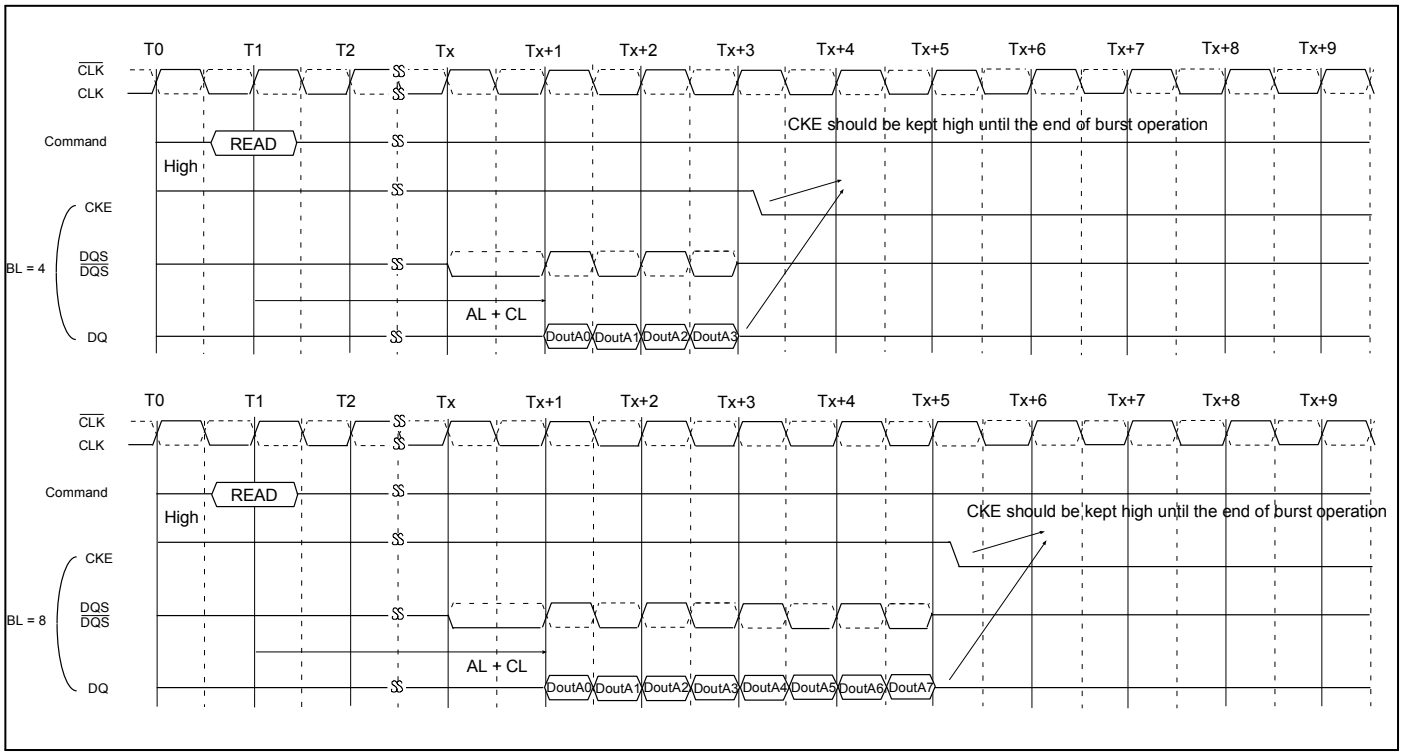
1. Device must be in the "All banks idle" state prior to entering Self Refresh mode.
2. ODT must be turned off t_{AOFD} before entering Self Refresh mode, and can be turned on again when t_{XSRD} timing is satisfied.
3. t_{XSRD} is applied for a Read or a Read with Auto Precharge command.
4. t_{XSNR} is applied for any command except a Read or a Read with Auto Precharge command.

Power-Down

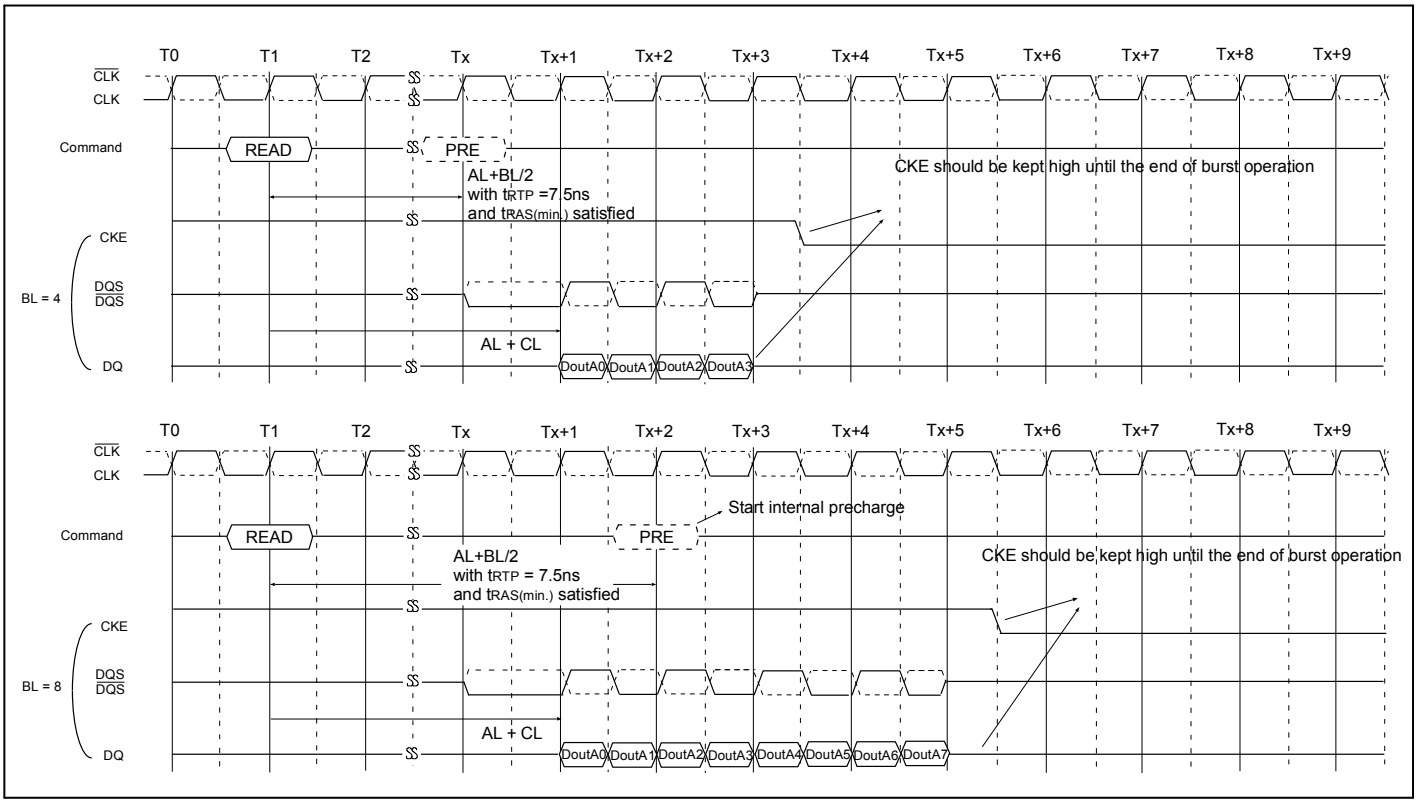
Power-Down is synchronously entered when CKE is registered LOW (no accesses can be in progress). CKE is not allowed to go LOW while MRS or EMRS command time, or read or write operation is in progress. CKE is allowed to go LOW while any of other operations such as Bank Active, Precharge or Auto Precharge, or Auto Refresh is in progress. The DLL should be in a locked state when Power-Down is entered. Otherwise DLL should be reset after exiting Power-Down mode for proper read operation.
If Power-Down occurs when all banks are idle, this mode is referred to as Precharge Power-Down; if Power-Down occurs when there is a Bank Active command in any bank, this mode is referred to as Active Power-Down. Entering Power-Down deactivates the input and output buffers, excluding CLK, $\overline{CLK}$, ODT and CKE. Also the DLL is disabled upon entering Precharge Power-Down or slow exit Active Power-Down, but the DLL is kept enabled during fast exit Active Power-Down. In Power-Down mode, CKE LOW and a stable clock signal must be maintained at the inputs of the device, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE LOW must be maintained until t_{CKE} has been satisfied. Power-Down duration is limited by 9 times t_{REFI} of the device.
The Power-Down state is synchronously exited when CKE is registered HIGH (along with a NOP or DESELECT command). CKE HIGH must be maintained until t_{CKE} has been satisfied. A valid, executable command can be applied with Power-Down exit latency, t_{XP}, t_{XARD}, or t_{XARDS}, after CKE goes HIGH.



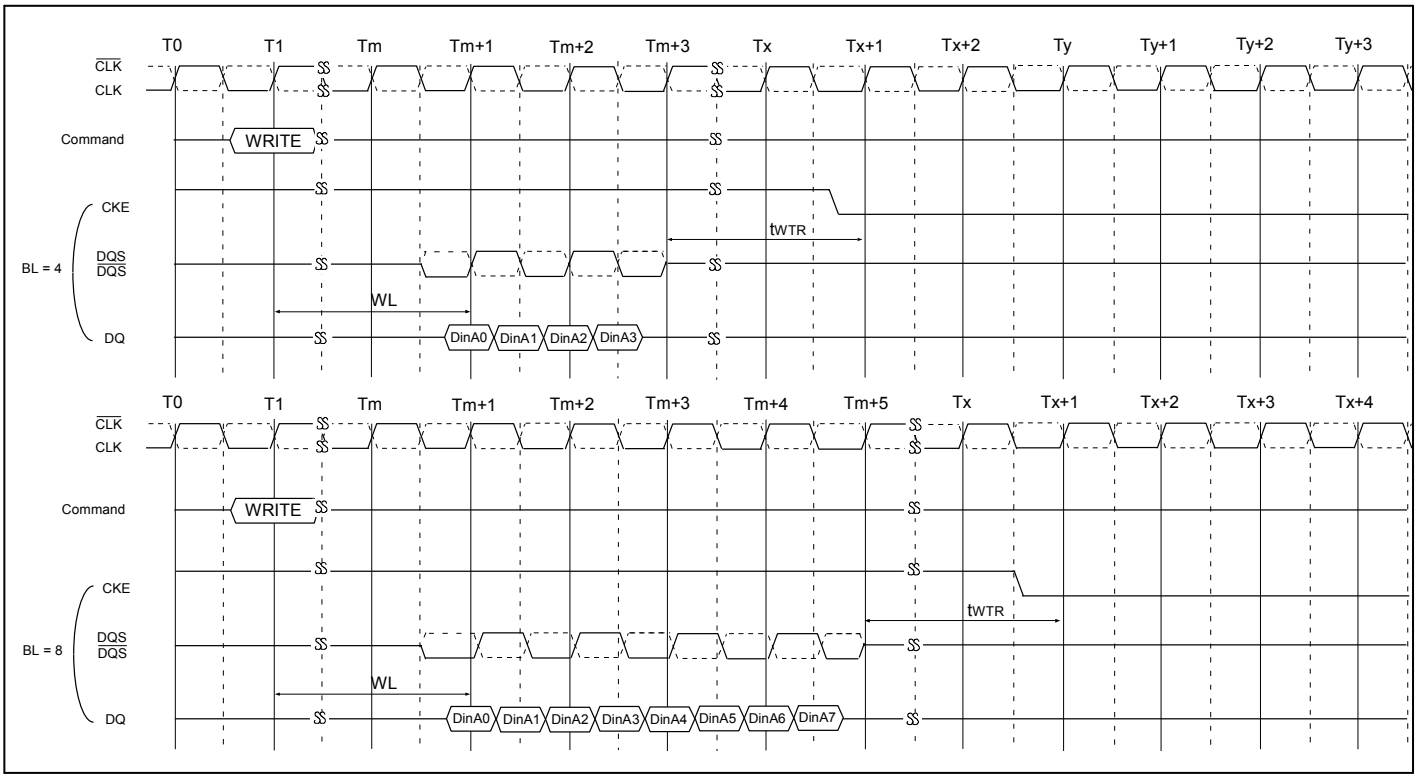
Read to Power-Down Entry



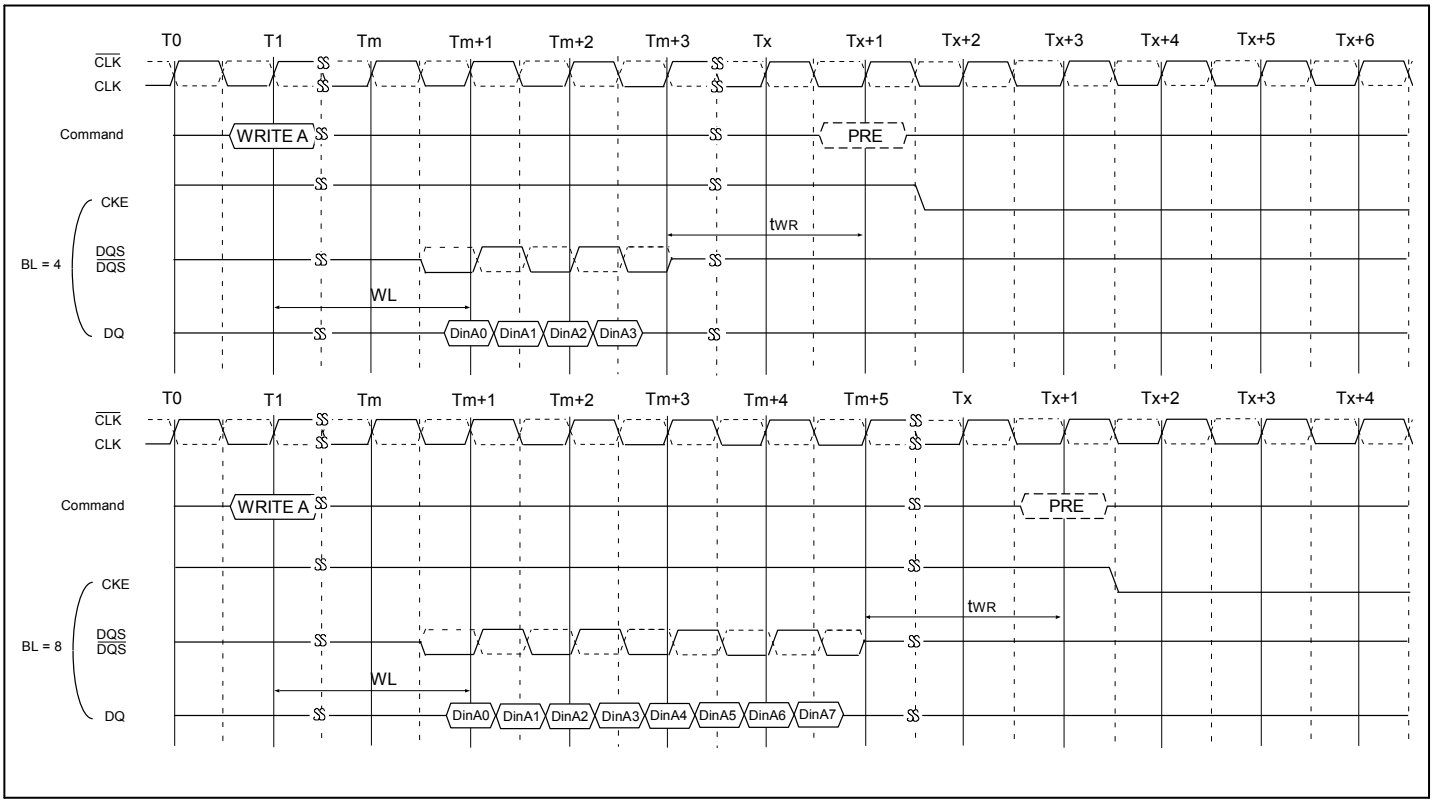
Read with Auto Precharge to Power-Down Entry



Write to Power-Down Entry

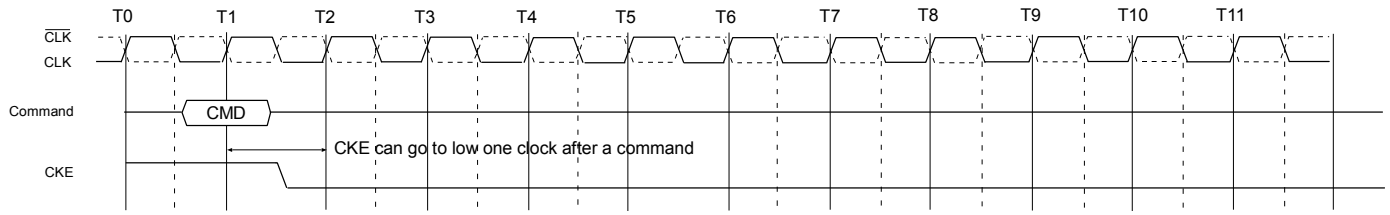


Write with Auto Precharge to Power-Down Entry



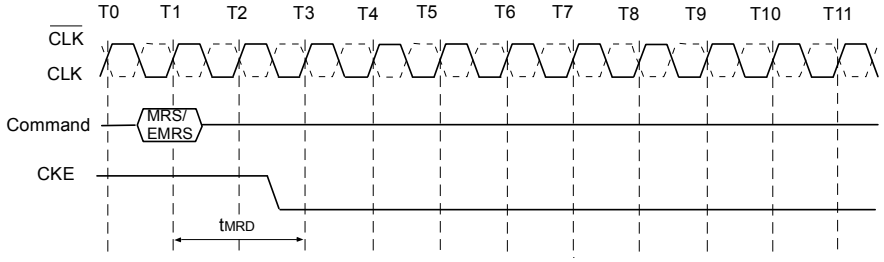
Note: If t_{CK} < 1.875ns, the device can not support Write with Auto Precharge function.

Auto Refresh/ Bank Active/ Precharge to Power-Down Entry



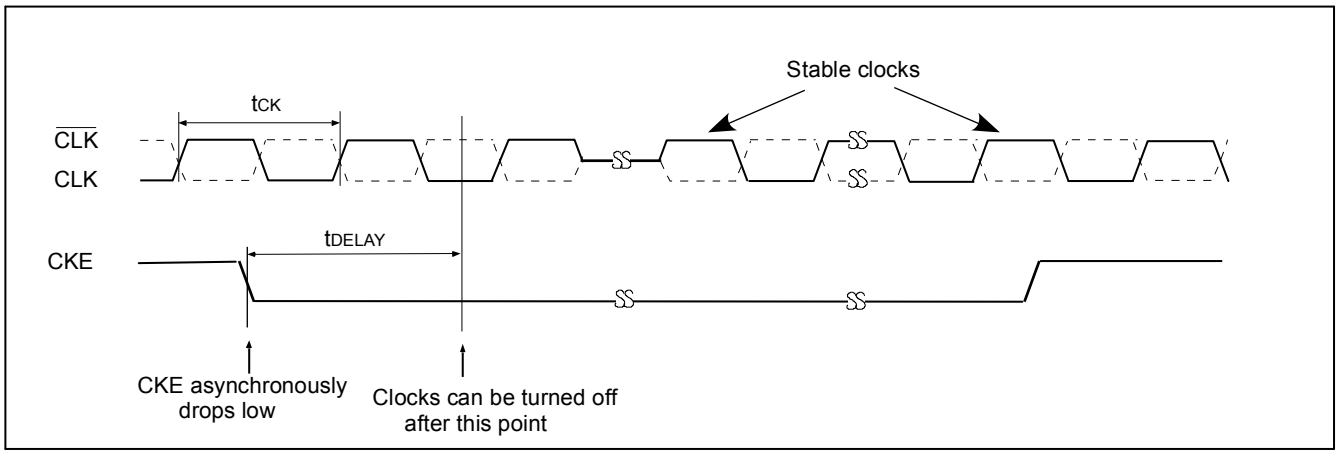
Note: CMD could be Auto Refresh/ Bank Active/ Precharge command.

MRS/EMRS to Power-Down Entry



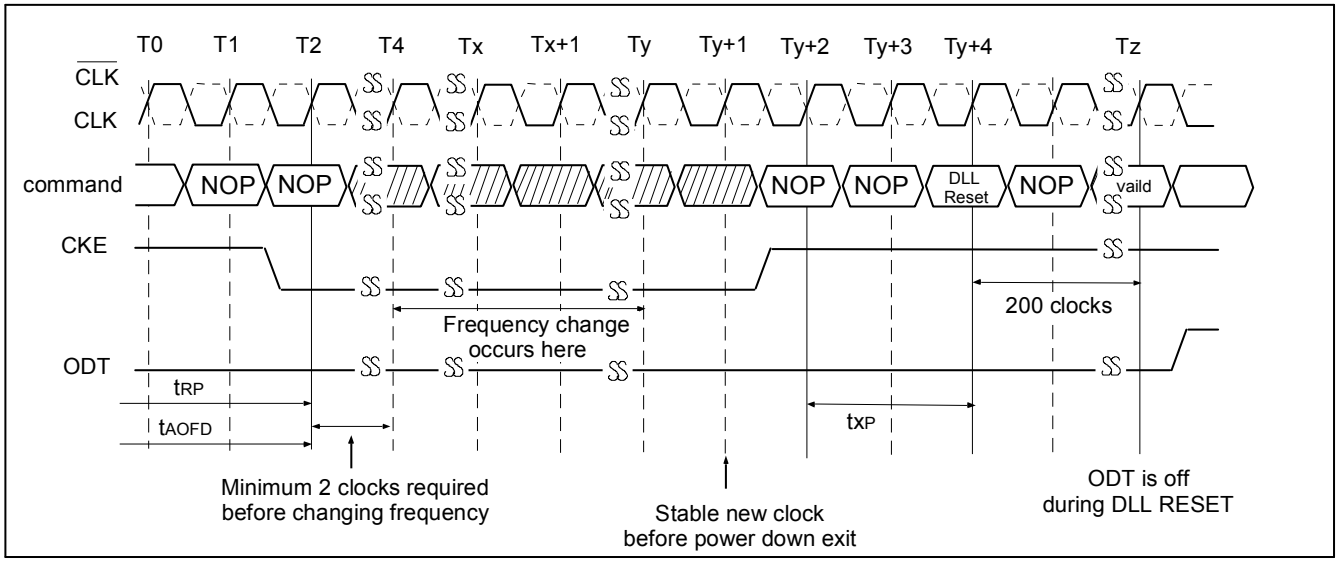
Asynchronous CKE Low event

DDR2 SDRAM requires CKE to be maintained “HIGH” for all valid operations as defined in this data sheet. If CKE asynchronously drops “LOW” during any valid operation, the device is not guaranteed to preserve the contents of array. If this event occurs, memory controller must satisfy t_{DELAY} before turning off the clocks. Stable clocks must exist at the input of device before CKE is raised “HIGH” again. The device must be fully re-initialized (steps 4 ~ 13) as described in initialization sequence. The device is ready for normal operation after the initialization sequence.



Clock Frequency change in Precharge Power-Down mode

DDR2 SDRAM input clock frequency can be changed under following condition:
The device is in Precharge Power-Down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. The device input clock frequency is allowed to change only between t_{CK} (min) and t_{CK} (max). During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once input clock frequency is changed, stable new clocks must be provided before Precharge Power-Down may be exited and DLL must be RESET via MRS after Precharge Power-Down exit. Depending on new clock frequency an additional MRS command may need to be issued to appropriately set the WR, CL etc.. During DLL re-lock period, ODT must remain off. After the DLL lock time, the device is ready to operate with new clock frequency.



Functional Truth Table [*7]

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP or Power-Down
	L	H	H	H	X	NOP	NOP or Power-Down
	L	H	L	X	BA, CA, A10	READ / READA / WRITE / WRITEA	ILLEGAL (*1)
	L	L	H	H	BA, RA	Active	Bank Active, Latch RA
	L	L	H	L	BA, A10 / A10	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	Refresh	Refresh (*2)
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	Mode Register setting / Extended Mode Register setting (*2)
BANK ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto Precharge
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto Precharge
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 /A10	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto Precharge (*1, 4)
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL (*1)
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL (*1) / ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to end)
	L	H	H	H	X	NOP	NOP (Continue Burst to end)
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL (*1)
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge (*1, 4)
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL (*1) / ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to end)
	L	H	H	H	X	NOP	NOP (Continue Burst to end)
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL (*1)
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL (*1)
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL (*1) / ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL (*1)
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL (*1)
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL (*1) / ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
PRE-CHARGING	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})
	L	H	L	X	BA, CA, A10	READ / READA / WRITE / WRITEA	ILLEGAL (*1)
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 / A10	PRE / PREA	NOP (Idle after t_{RP})
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Bank Active after t_{RCD})
	L	H	H	H	X	NOP	NOP (Bank Active after t_{RCD})
	L	H	L	X	BA, CA, A10	READ / READA / WRITE / WRITEA	ILLEGAL (*1, 5)
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL

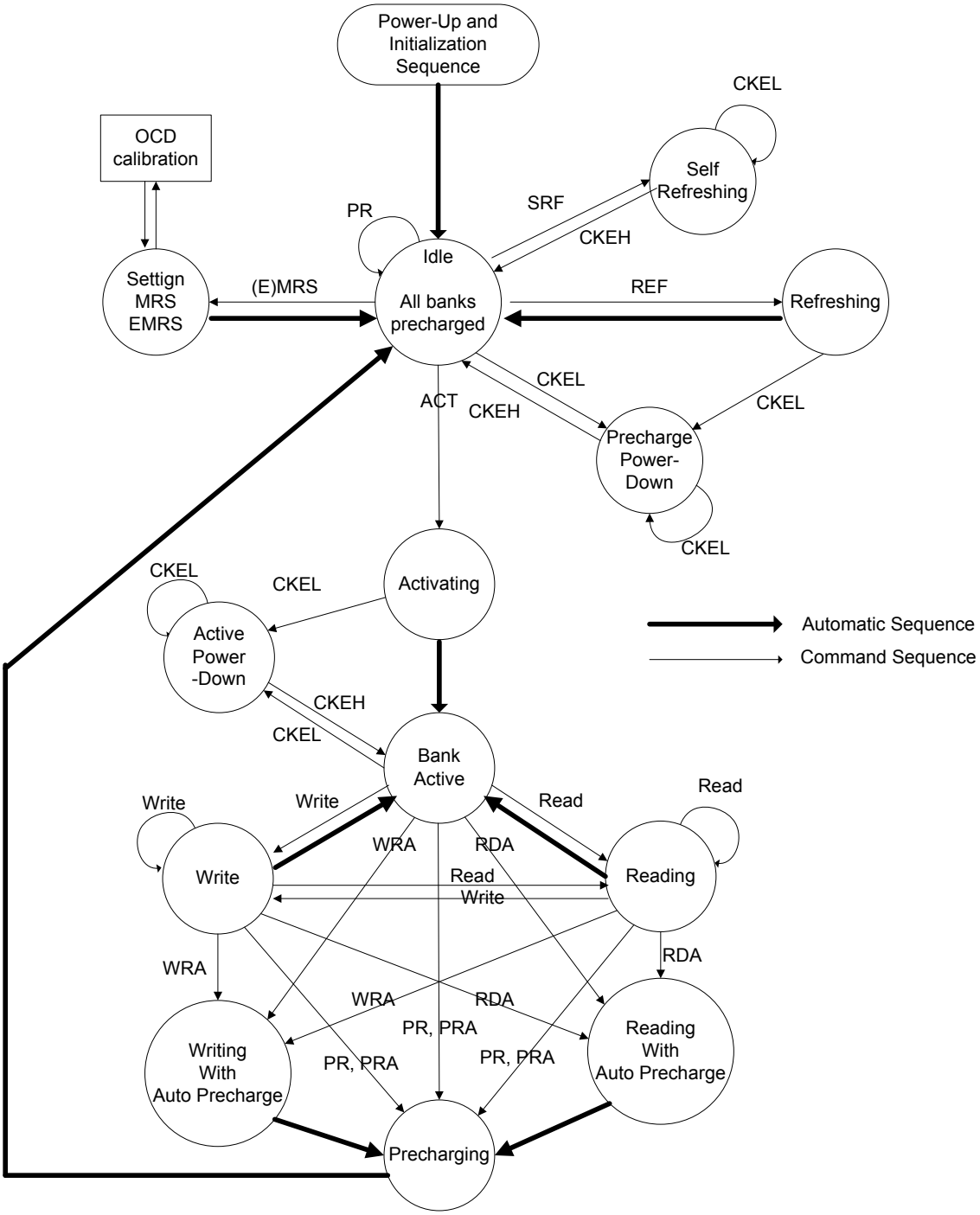
Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP (Bank Active after t_{WR})
	L	H	H	H	X	NOP	NOP (Bank Active after t_{WR})
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL (*1, 6)
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	WRITE / WRITEA
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL (*1) / ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
WRITE RECOVERING with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Bank Active after t_{WR})
	L	H	H	H	X	NOP	NOP (Bank Active after t_{WR})
	L	H	L	X	BA, CA, A10	READ / READA / WRITE / WRITEA	ILLEGAL (*1)
	L	L	H	H	BA, RA	Active	ILLEGAL (*1)
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL (*1) / ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
REFRESH	H	X	X	X	X	DESEL	NOP (Idle after t_{RFC})
	L	H	H	H	X	NOP	NOP (Idle after t_{RFC})
	L	H	L	X	BA, CA, A10	READ / READA / WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL
(Extended) MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after t_{MRD})
	L	H	H	H	X	NOP	NOP (Idle after t_{MRD})
	L	H	L	X	BA, CA, A10	READ / READA / WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	Active	ILLEGAL
	L	L	H	L	BA, A10 / A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	Refresh	ILLEGAL
	L	L	L	L	Op-Code Mode-Add	MRS / EMRS	ILLEGAL

H = High Level, L = Low level, X = Don't Care
BA = Bank Address, RA =Row Address, CA = Column Address, NOP = No Operation
ILLEGAL = Device operation and / or data integrity are not guaranteed.

Note:

1. This command may be issued for other banks, depending on the state of the banks.
2. All banks must be in "IDLE".
3. All AC timing specs must be met.
4. Only allowed at the boundary of 4 bits burst. Burst interruption at other timings is illegal.
5. Available in case t_{RCD} is satisfied by AL setting.
6. Available in case t_{WTR} is satisfied.
7. If t_{CK} < 1.875ns, the device can not support Write with Auto Precharge function.

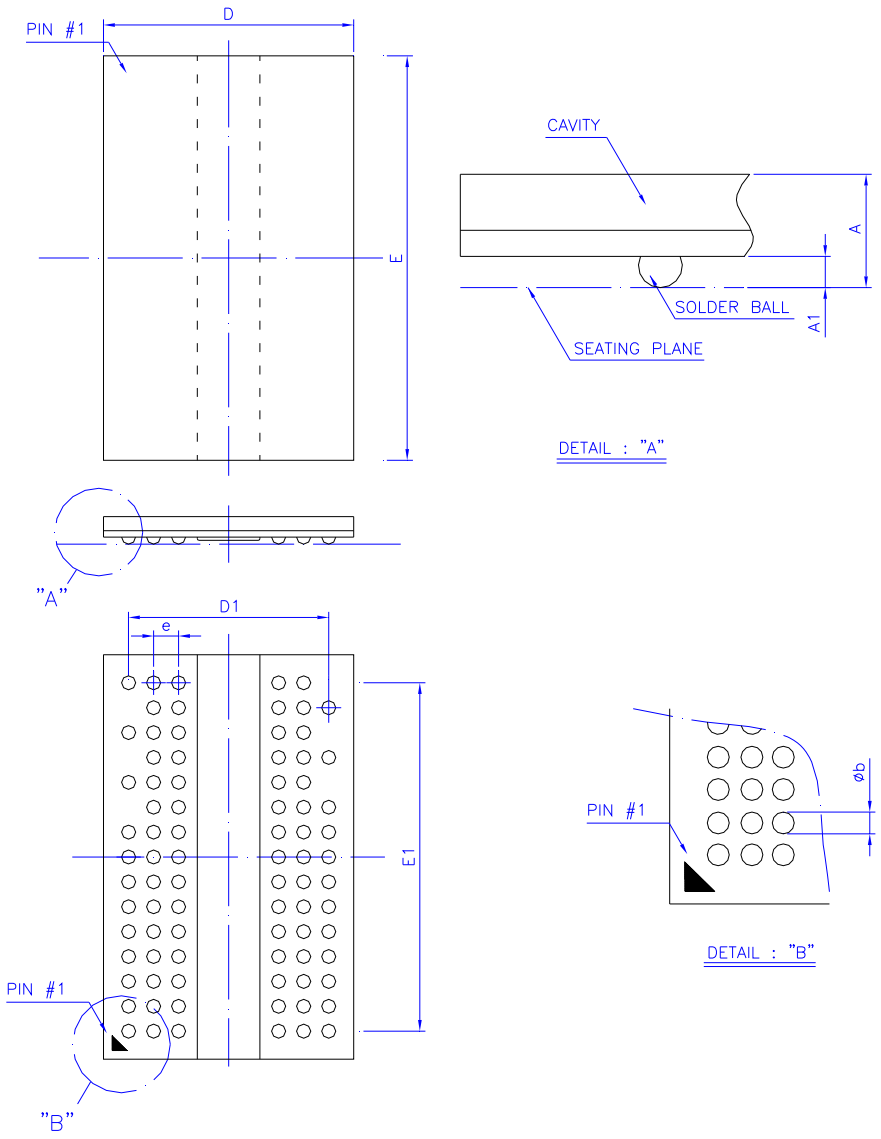
Simplified States Diagram



CKEL = CKE LOW
CKEH = CKE HIGH
ACT = Activate
WR(A) = Write (with Auto Precharge)
RD(A) = Read (with Auto Precharge)
PR(A) = Precharge (All)
(E)MRS = (Extended) Mode Register Set
SRF = Enter Self Refresh
REF = Auto Refresh

PACKING DIMENSIONS

84-BALL DDRII SDRAM (8x12.5x1.2 mm)

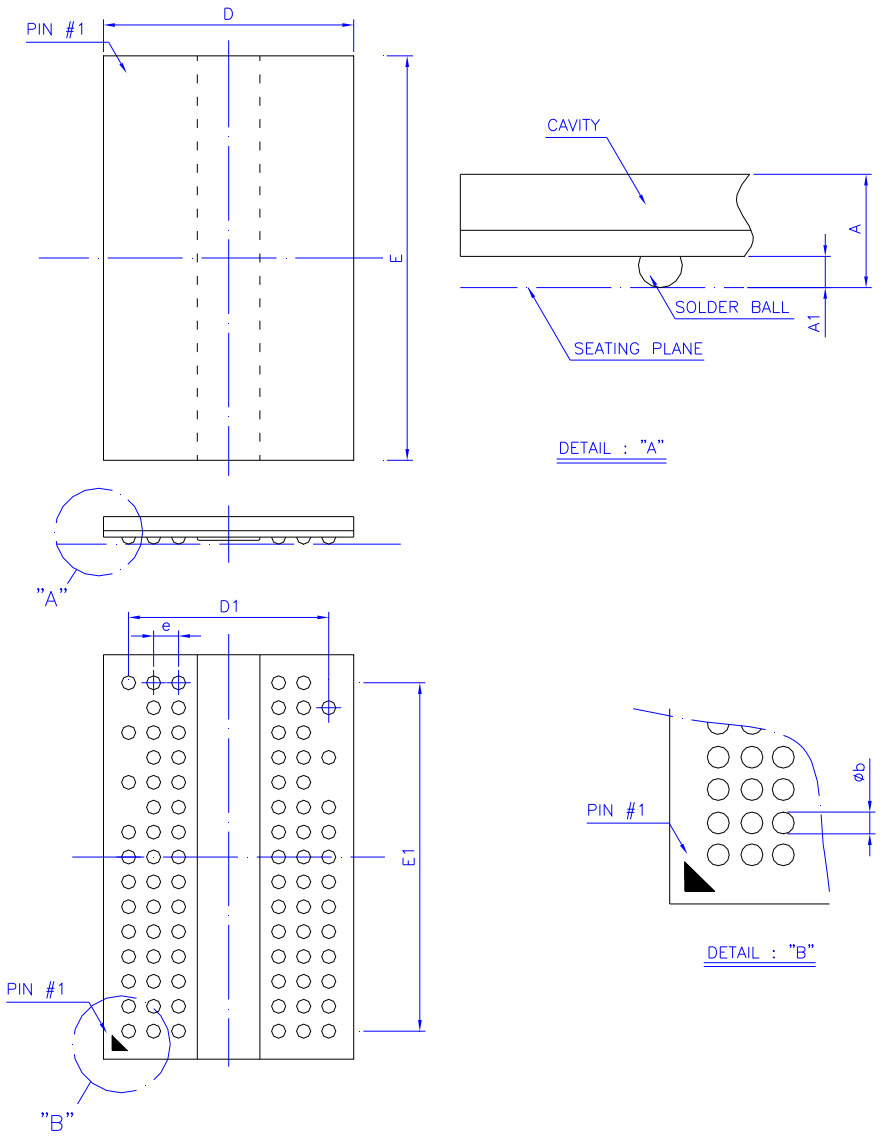


Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A			1.20			0.047
A_1	0.25	0.30	0.40	0.010	0.012	0.016
Φ_b	0.37	0.45	0.50	0.015	0.018	0.020
D	7.90	8.00	8.10	0.311	0.315	0.319
E	12.40	12.50	12.60	0.488	0.492	0.496
D_1	6.40 BSC			0.252 BSC		
E_1	11.20 BSC			0.441 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter.

PACKING DIMENSIONS

84-BALL DDRII SDRAM (8x12.5x1.0 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A			1.00			0.039
A_1	0.25	0.30	0.40	0.010	0.012	0.016
Φ_b	0.37	0.45	0.50	0.015	0.018	0.020
D	7.90	8.00	8.10	0.311	0.315	0.319
E	12.40	12.50	12.60	0.488	0.492	0.496
D_1	6.40 BSC			0.252 BSC		
E_1	11.20 BSC			0.441 BSC		
e	0.80 BSC			0.031 BSC		

Controlling dimension : Millimeter.

Revision History

Revision	Date	Description
0.1	2013.03.11	Original
0.2	2013.06.26	1. Modify the specification of I_{DD} 2. Add a note for t_{WTR}
0.3	2013.09.10	1. Delete speed grade -3 2. Correct the figure of AC Input Test Signal Waveforms
1.0	2013.10.17	1. Delete "Preliminary" 2. Modify Input / Output Capacitance
1.1	2013.12.12	1. Add a description into EMRS (1) 2. Correct the specification of tCK (max) 3. Delete tFAW
1.2	2014.01.17	Add speed grade -1.5
1.3	2014.03.20	Modify the voltage for speed grade -1.5
1.4	2014.05.30	1. Add speed grade -1.3 2. Modify WR setting of MRS for speed grade -1.5

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