KP3500A Phase Control Thyristor

Feature

- ■ Full diffusion process,capsule type ceramic package
- ■ Amplifying gates
- ■ Double sided cooling

Typical Application

- ■ High power transmission
- ■ DC and AC motor control,Controlied rectifier
- ■ AC DC switch,phase-controlied rectifying
- ■ Active and reactive invresion

$I_{T(AV)}$	3500A
V_{DRM}/V_{RRM}	100-6500V
I_{TSM}	44KA
I^2t	18000 10^3a^2s

SYMBOL	CHARCTERISTIC	TEST CONDITIONS	T_J (℃)	VALUE Min	VALUE Max	UNIT
$I_{T(AV)}$	Mean on-state current	180° half sine wawe 50Hz Double side cooled, THS=97℃	125		3500	A
$I_{T(AV)}$	Mean on-state current	180° half sine wawe 50Hz Double side cooled, THS=55℃	125		4093	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repettive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&$V_{RSM=}V_{DRM}$&$V_{RRM+100V}$	125	100	6500	V
I_{DRM} I_{RRM}	Repetitive peak current	$V_{DM}=V_{DRM}$ $V_{RM=}V_{RRM}$	125		250	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125		44	KA
I^2t	I^2t for fusing coordination				1800	A^{2S}*10
V_{TO}	Threshold voltage		125		0.85	V
r_T	On-state slop resistance				0.07	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=5000A,F=15KN	25		2.2	V
dv/dt	Critical rate of rise of-state voltage	V_{DM}=0.67V_{DRM}	125		1000	V/us
di/dt	Critical rate of rise of on-state current	V_{DM}=67％V_{DRM} TO 1000A, Gate pulse tr≤0.5us I_{GM}=1.5A	125		250	A/us
I_{TM}	Reverse recovery current	I_{TM}=5000A，tq=1000us Di/dt=-20A/us. V_r=50V	125		220	A
t_{rr}	Reverse recovery time				22	us
Q_{rr}	Recovery charge				2420	uC
I_{GT}	Gate trigger current		25	40	300	mA
V_{GT}	Gate trigger voltage	V_A=12V,I_A=1A	25	0.8	3.0	V
I_H	Holding current			20	300	mA
V_{GD}	Npn-trigger gate voltage	V_{DM}=0.67V_{DRM}	125	0.3		V
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At180° sine double side cooled Clamping force 5.0kn			0.001	℃/W
F_M	Mounting force			70	85	KN
T_{stq}	Stored temperature			-40	140	℃
W_t	Weight					g
Outline						

HUAJING

Peak On-state Voltage Vs. Peak On-state Current

Fig.1

Max. junction To heatsink Thermal Impedance Vs. Time

Fig.2

Max. Power Dissipation Vs. Mean On-state Current

Fig.3

Max. heatsink Temperature Vs. Mean On-state Current

Fig.4

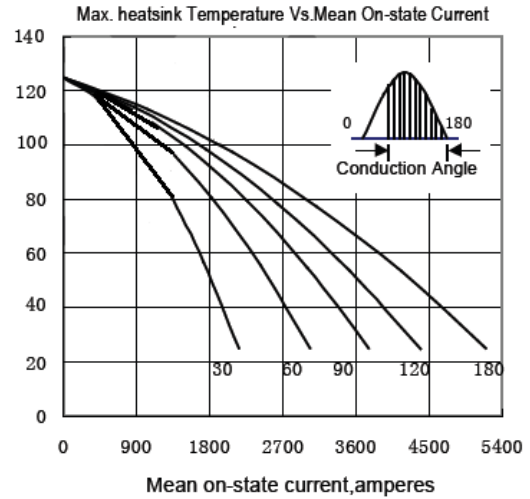Max. Power Dissipation Vs. Mean On-state Current
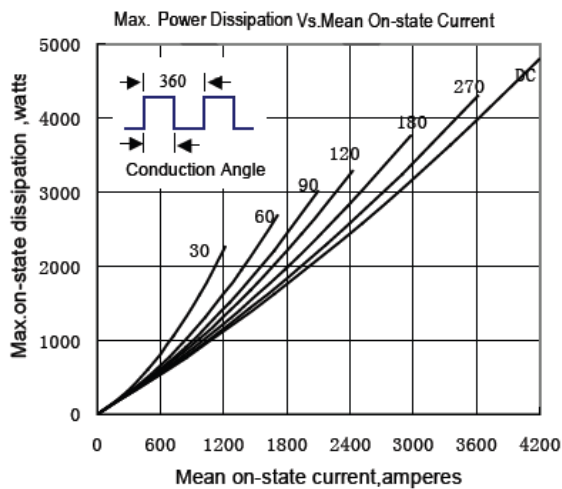
Fig.5
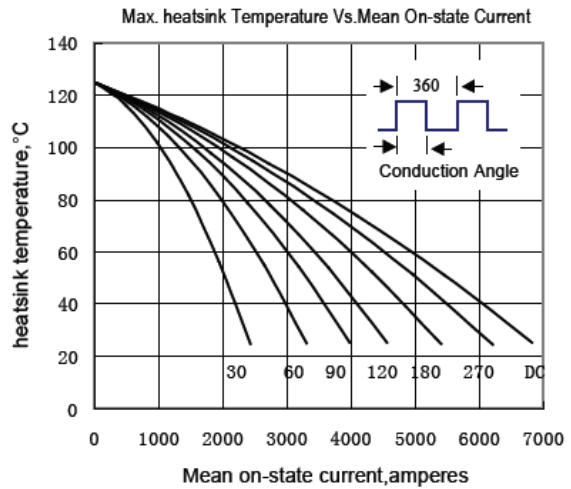
Max. heatsink Temperature Vs. Mean On-state Current
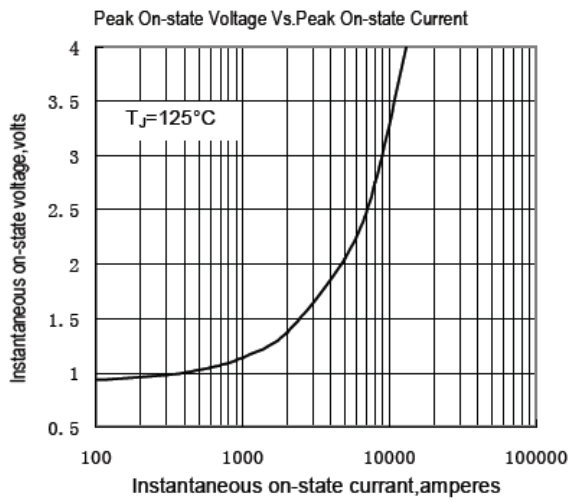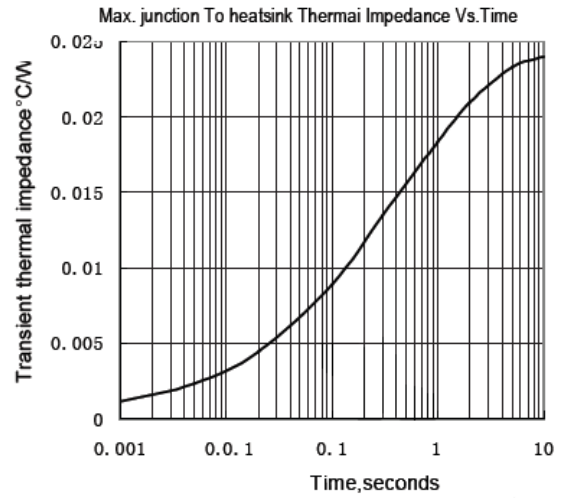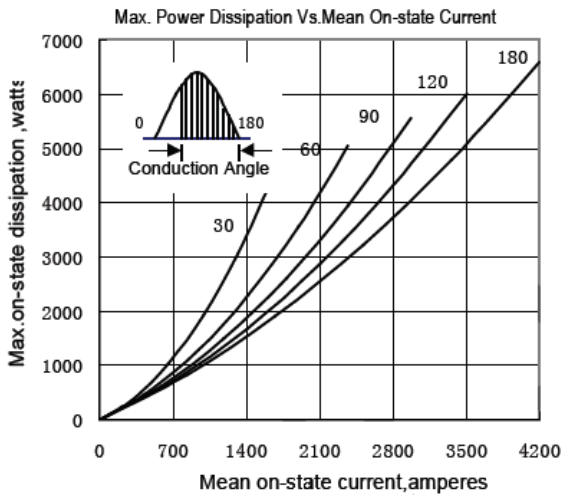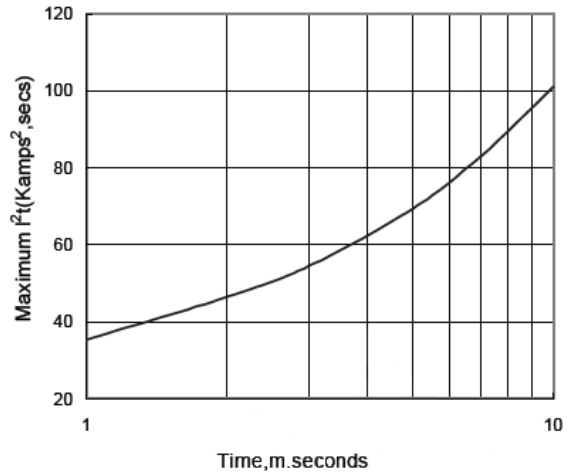
Fig.6

Surge Current Vs.Cycles
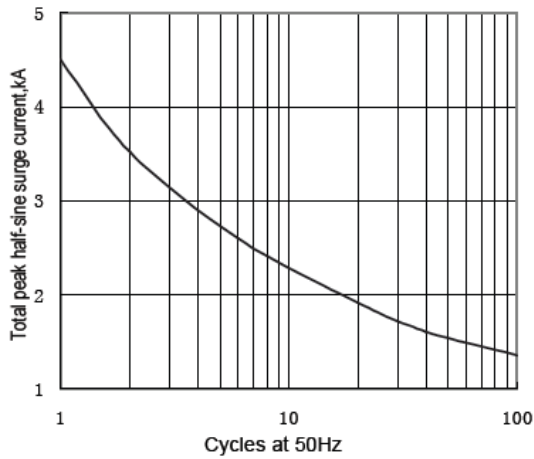
Fig.7

I^2t Vs.Time

Fig.8

Gate characteristic at 25°C junction temperature

$P_{GM}=100W$
(100μs spulse)
max.
min.
P_G2W
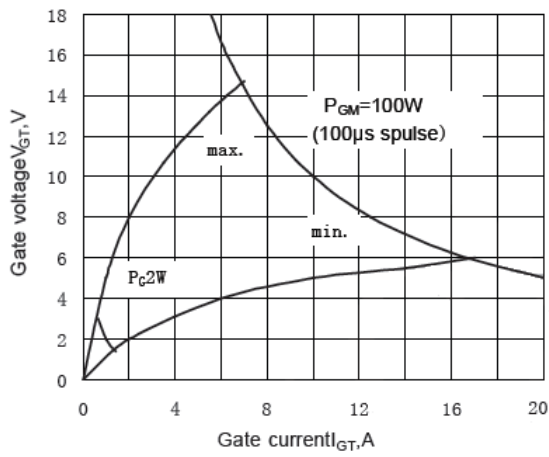
Fig.9

Gate Trigger Zone at varies temperature

-30°C
-10°C
25°C
125°C

Fig.10

Outline: