HARRIS

IRF360
IRF362

N-Channel Power MOSFETs
Avalanche-Energy Rated

August 1991

Features

- 25A and 22A, 400V
- $r_{DS}(on)$ = 0.20Ω and 0.25Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

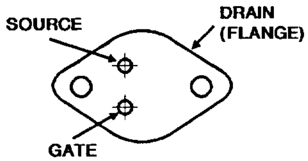
Description

The IRF360 and IRF362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

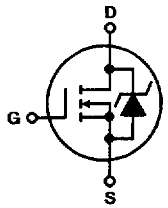
Package

TO-204AE
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

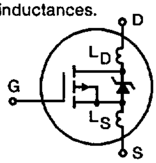
		IRF360	IRF362	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	25	22	A
T_C = +100°C	I_D	16	14	A
Pulsed Drain Current (1)	I_{DM}	100	88	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	300	300	W
Linear Derating Factor		2.4	2.4	W/°C
Single Pulse Avalanche Energy Rating (2) See Figure 14	E_{AS}	980	980	mj
Avalanche Current, Repetitive or Non-repetitive (1)	I_{AR}	25	25	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:
1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 2.8mH, R_{GS} = 25Ω, Peak I_L = 25A.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

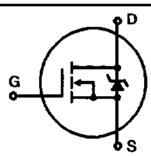
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2276.1**

Electrical Characteristics $T_C = 25^oC$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	400	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = 20V$	-	-	100	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = -20V$	-	-	-100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, $V_{GS} = 0V$	-	-	250	µA
		V_{DS} = Max Rating x 0.8, $V_{GS} = 0V$, $T_J = +125^oC$	-	-	1000	µA
On-State Drain Current (Note 3) IRF360	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} Max$, $V_{GS} = 10V$	25	-	-	A
IRF362			22	-	-	A
Static Drain-Source On-State Resistance (Note 3) IRF360	$r_{DS(ON)}$	$V_{GS} = 10V, I_D = 14A$	-	0.18	0.20	Ω
IRF362			-	0.20	0.25	Ω
Forward Transconductance (Note 3)	g_{fs}	$I_{DS} = 14A, V_{DS} \geq 50V$	14	21	-	S(℧)
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = 25V$, f = 1.0MHz See Figure 10	-	4000	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	97	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 200V, I_D = 25A, R_G = 4.3\Omega$ $R_D = 7.5\Omega$. (MOSFET switching times are essentially independent of operating temperature)	-	22	33	ns
Rise Time	t_r		-	94	140	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	120	ns
Fall Time	t_f		-	66	99	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = 10V, I_D = 25A, V_{DS} = 0.8V$ x Max Rating. See Figure 16 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	120	170	nC
Gate-Source Charge	Q_{gs}		-	19	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	60	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of die. / Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	13	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.42	$^oC/W$
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	$^oC/W$
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	$^oC/W$

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	25	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	100	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_J = +25^oC, I_S = 25A, V_{GS} = 0V$	-	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = +25^oC, I_F = 25A, dI_F/dt = 100A/\mu s$	200	460	1000	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +25^oC, I_F = 25A, dI_F/dt = 100A/\mu s$	3.1	7.1	16	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.	-	-	-	-

NOTES:
1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. $V_{DD} = 50V$, Starting $T_J = +25^oC$, L = 2.8mH, $I_L = 25A$
3. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$

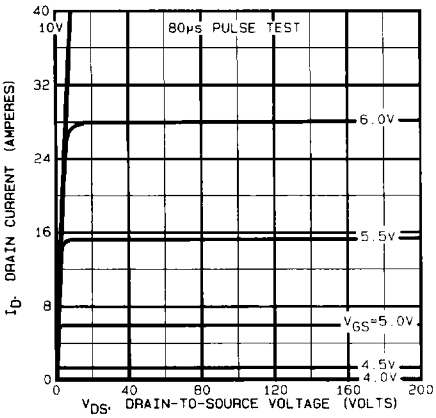


Fig. 1 - Typical output characteristics.

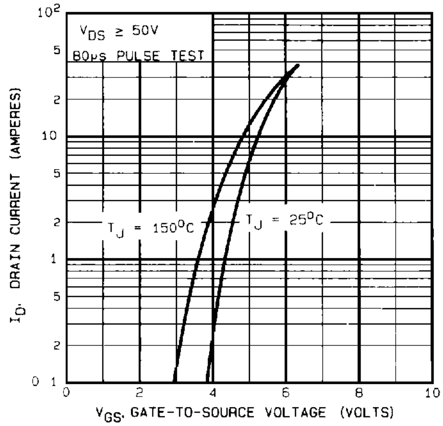


Fig. 2 - Typical transfer characteristics.

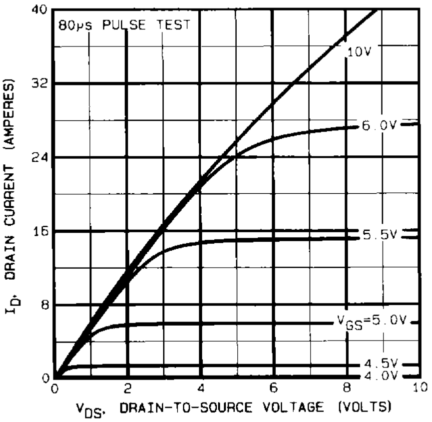


Fig. 3 - Typical saturation characteristics.

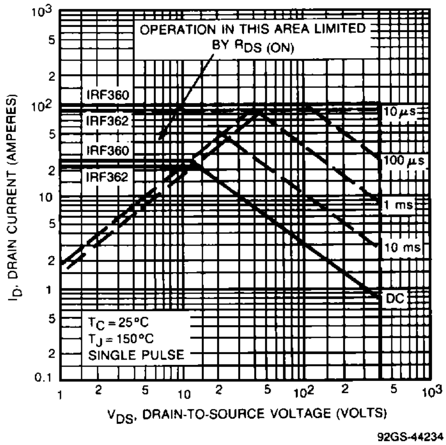
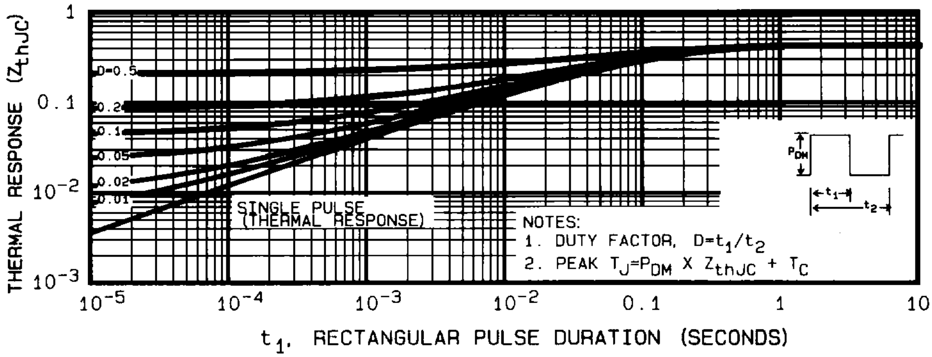


Fig. 4 - Maximum safe operating area.



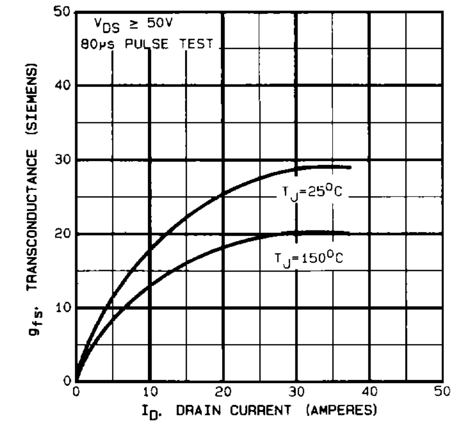


Fig. 6 - Typical transconductance vs. drain current.

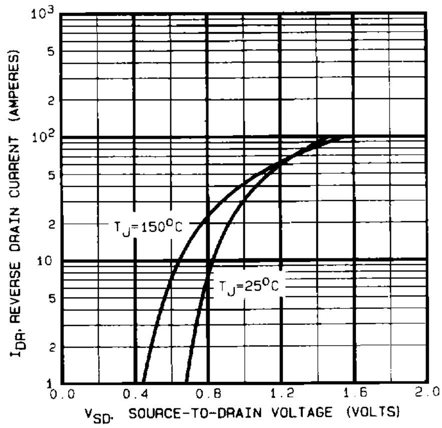


Fig. 7 - Typical source-drain diode forward voltage.

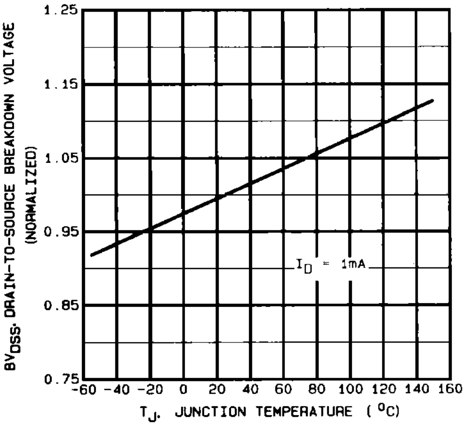


Fig. 8 - Breakdown voltage vs. temperature.

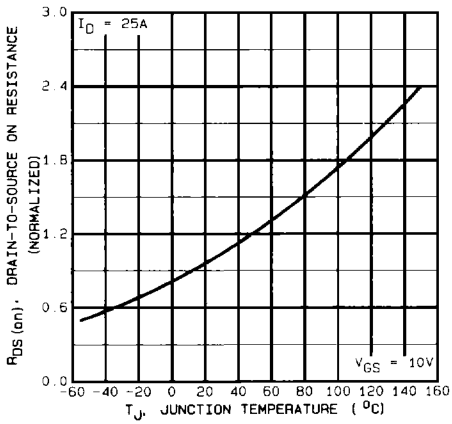


Fig. 9 - Normalized on-resistance vs. temperature.

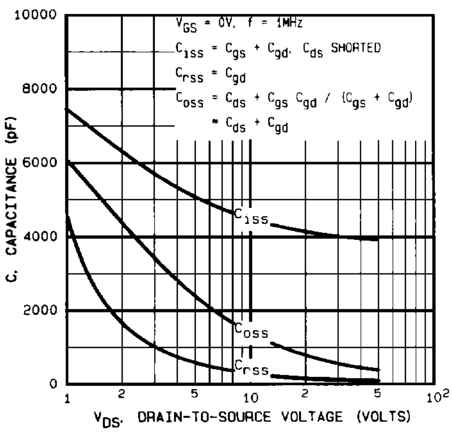


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

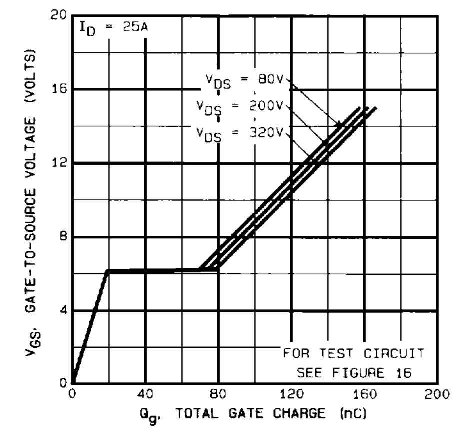


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

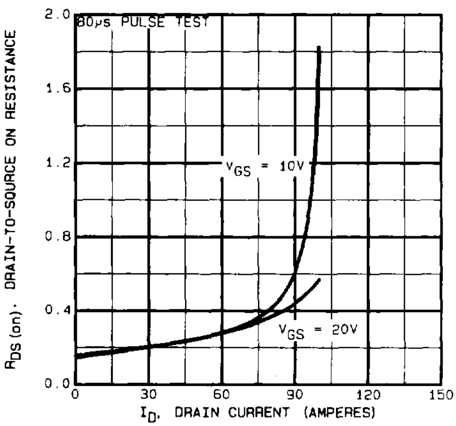


Fig. 12 - Typical on-resistance vs. drain current.

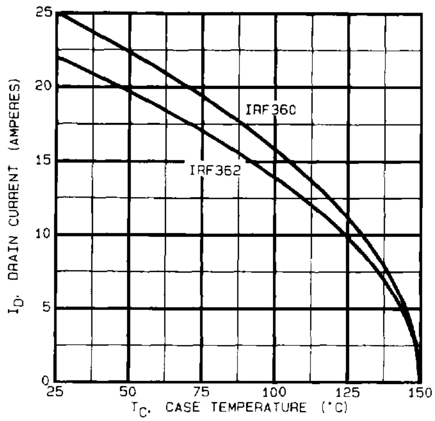


Fig. 13 - Maximum drain current vs. case temperature.

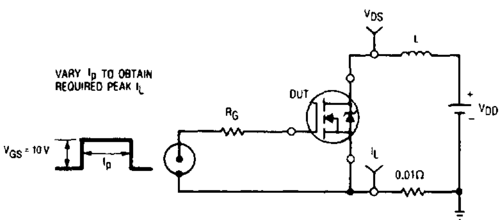


Fig. 14a - Unclamped inductive test circuit.

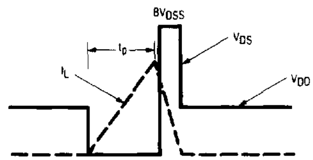


Fig. 14b - Unclamped inductive waveforms.

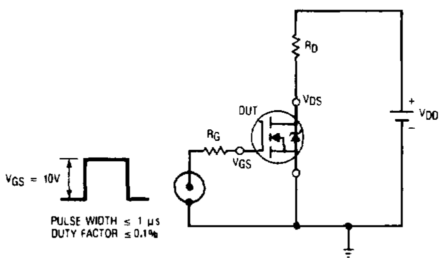


Fig. 15a - Switching time test circuit.

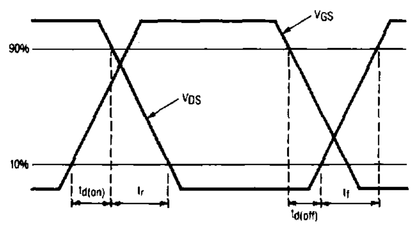


Fig. 15b - Switching time waveforms.

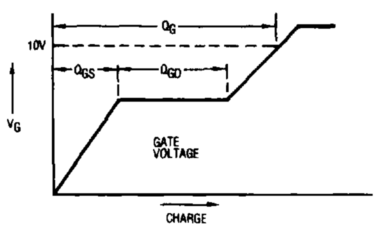


Fig. 16a - Basic gate charge waveform.

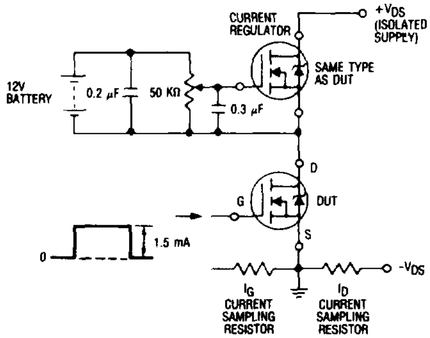


Fig. 16b - Gate charge test circuit.