PRELIMINARY

1Mx1 Static RAM CMOS, High Speed Module

The EDI8M11024C is an extremely high density, 1024Kx1 bit, high speed Static RAM module constructed using four 256Kx1 Static RAMs in leadless chip carriers on a multi-layered ceramic substrate. Functional equivalence to the megabit monolithic is achieved by utilization of an on-board decoder that interprets the higher order of address A18 and A19 to select one of the four 256Kx1 RAMs.

The EDI8M11024C has separate input and output lines to provide fast read and write access to all memory locations.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply, simplifying system design.

All EDI military modules are constructed with semiconductor components processed to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

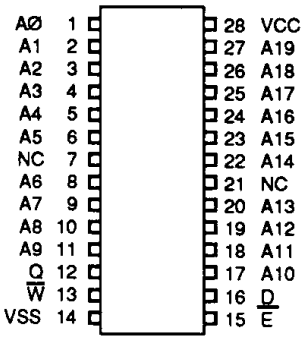
Features

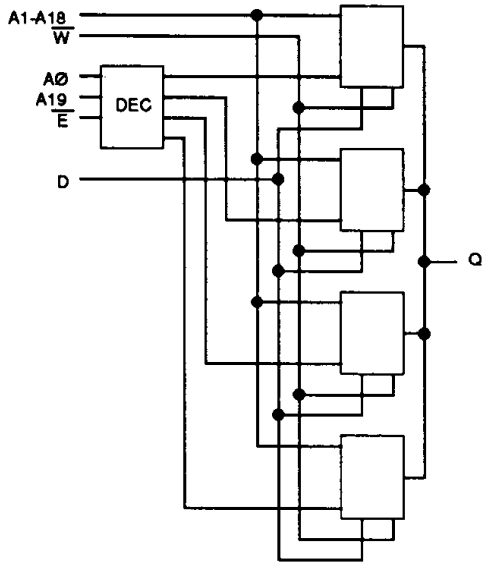
1024Kx1 bit CMOS Static Random Access Memory
- Access Times 35, 45, 55 and 70ns
- Fully Static, No Clocks
- Separate I/O Lines
- Inputs and Outputs Directly TTL Compatible
- Low Power Consumption

Jedec Approved Pinout
- 28 Pin Ceramic DIP, 400 mils wide, No. 121

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A19	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Military ..... -55°C to +125°C
Storage Temperature, Ceramic ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current. ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	110	210	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$≥ VIH, VIN ≤ VIL or VIN ≥ VIH	--	80	160	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-0.2V VIN ≥VCC-0.2V or VIN≤0.2V	--	10	30	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±5	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±5	µA
Output High Voltage	VOH	IOH= -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL= 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	40	pF
Capacitance Control (DQ Pins)	CD/Q	18	pF

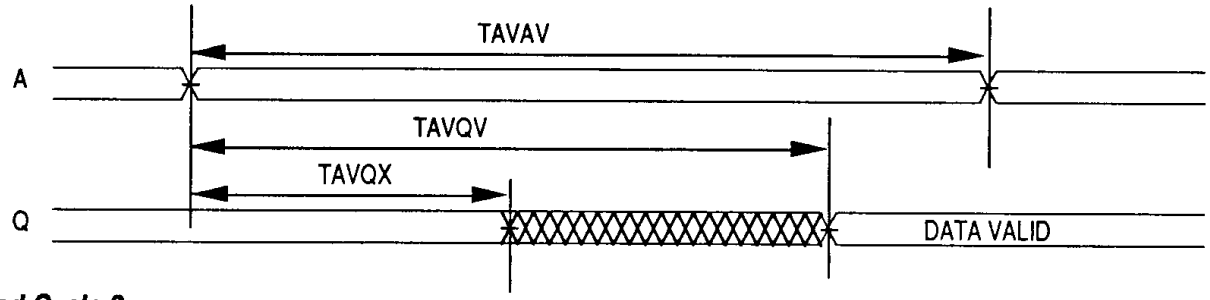
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

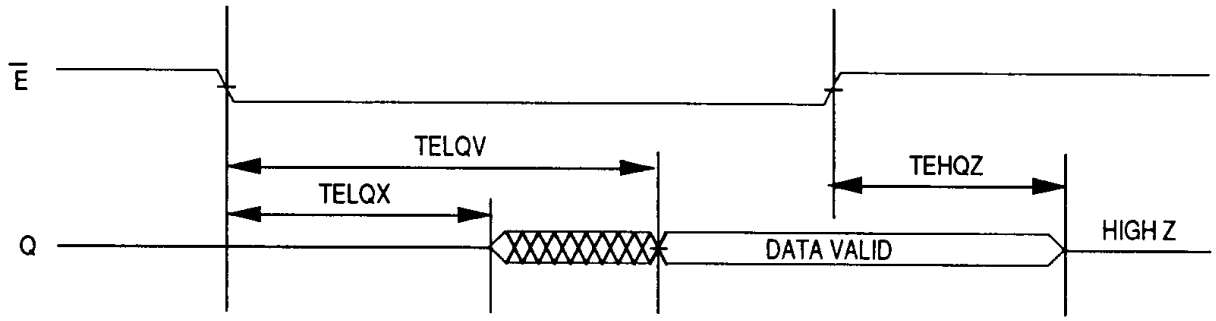
Parameter	Symbol	35ns		45ns		55ns		70ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		70		ns
Address Access Time	TAVQV		35		45		55		70	ns
Chip Enable Access Time	TELQV		35		45		55		70	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	25	0	30	0	30	0	30	ns
Output Hold from Address Change	TAVQX	5		5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		0		ns
Chip Disable to Power Down (1)	TPD	0	35	0	45	0	55	0	70	ns

Note 1: Parameter guaranteed, but not tested.

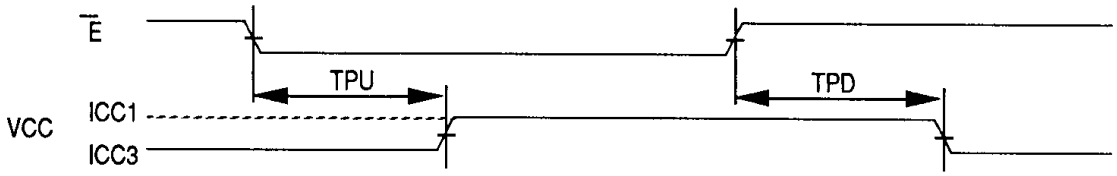
Read Cycle 1
$\overline{W}$ High (continuously selected, $\overline{E}$ Low)



Read Cycle 2
$\overline{E}$ Low, $\overline{W}$ High



$\overline{E}$ Power Down Function

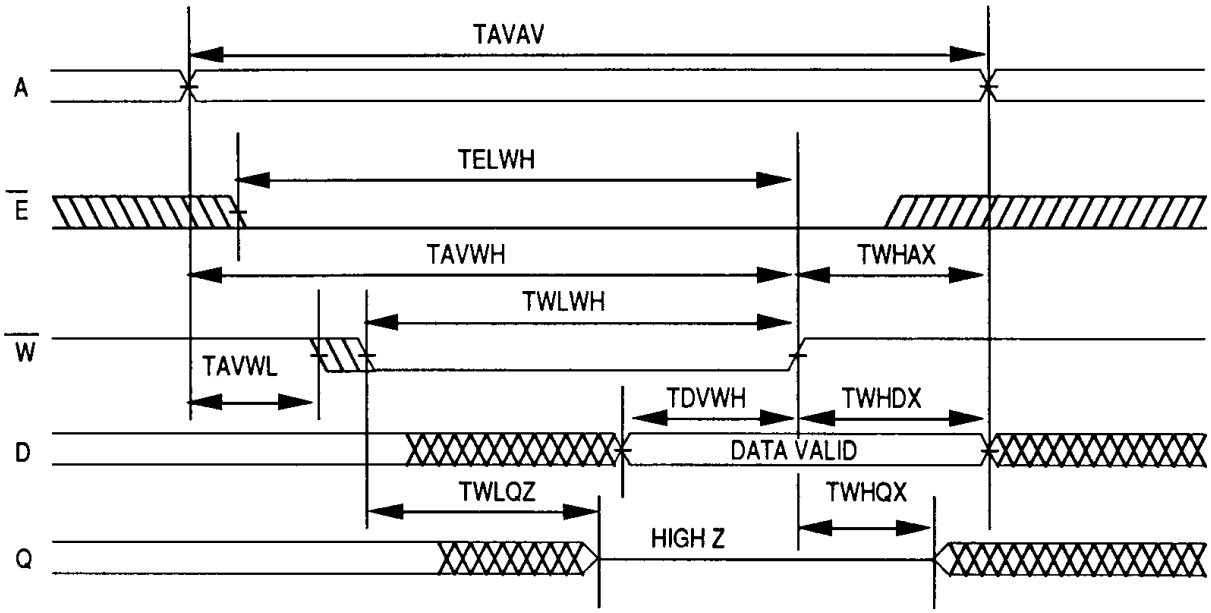


AC Characteristics
Write Cycle

Parameter	Symbol		35ns		45ns		55ns		70ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		70		ns
Chip Enable to	TELWH	$\overline{W}$	30		35		40		50		ns
End of Write	TWLEH	$\overline{E}$	30		35		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$	5		10		10		10		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		35		40		50		ns
End of Write	TAVEH	$\overline{E}$	30		35		40		50		ns
Write Pulse Width	TWLWH	$\overline{W}$	25		30		35		45		ns
	TELEH	$\overline{E}$	25		30		35		45		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	20	0	25	0	30	0	40	ns
Data to Write Time	TDVWH	$\overline{W}$	20		25		25		30		ns
	TDVEH	$\overline{E}$	20		25		25		30		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled