14+1 Channels Voltage Buffer with OTP/OCP for TFT LCD

EC5575A

FEATURES

• Supply Voltage Range：6V ~ 18V
• Rail-to-Rail Output Voltage Swing
• High Slew Rate：
  --- Vcom Buffer：30V/μs
  --- Gamma Buffer：2V/μs
• Thermal Shutdown Protection
• Short-Circuit Current Limit Protection
• Continuous Output Drive current：
  --- Vcom Buffer：±100mA(Max)
  --- Gamma Buffer：±30mA(Max)
• Ultra-small Package TQFP-48L(Exposed Pad)

APPLICATIONS

• TFT-LCD Reference Driver

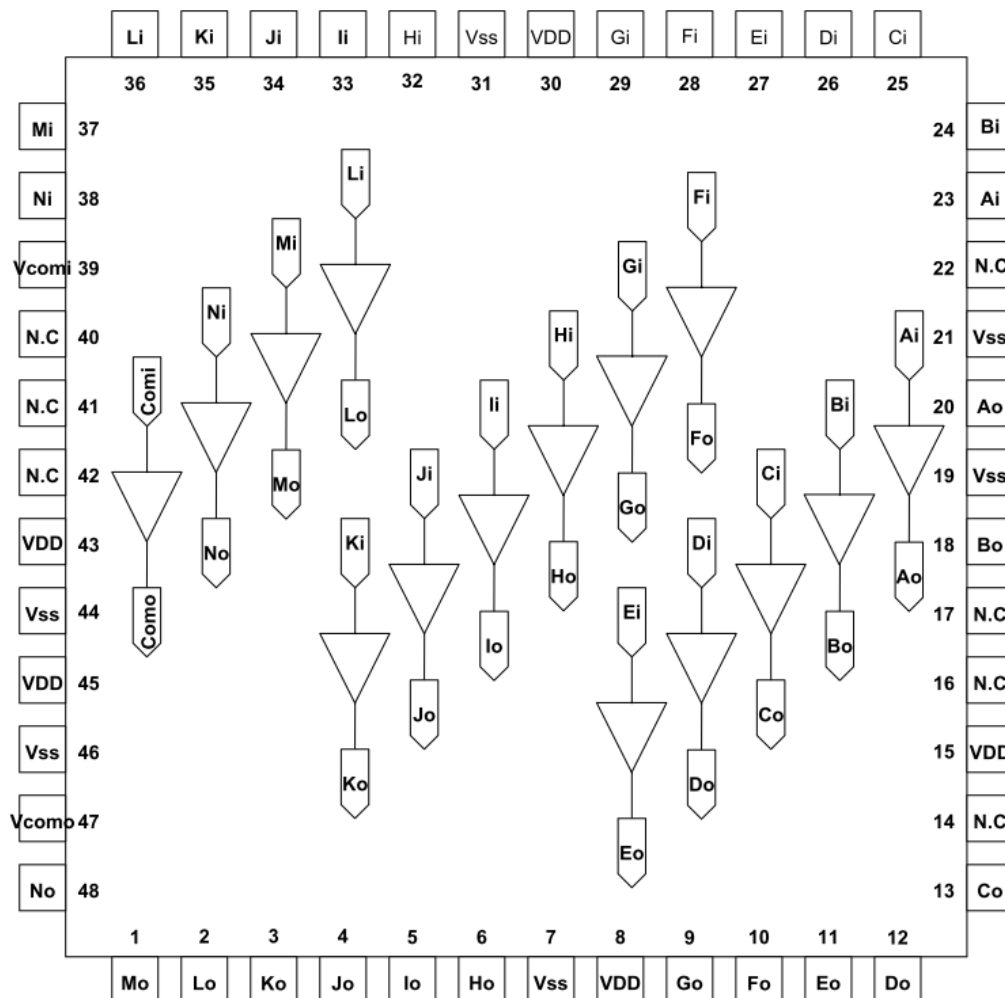## PIN ASSIGNMENT

GENERAL DESCRIPTION

The EC5575A is a 14+1 channel voltage buffers that buffers reference voltage for gamma correction in a thin film transistor liquid crystal display (TFT LCD). This device incorporating a Vcom amplifier circuit, four rail to rail buffer amplifier circuits (the highest two stage and lowest two stage) and 10 buffer amplifiers circuits.

The EC5575A is available in a space saving 48-pin TQFP package, and the operating temperature is from –20°C to +85°C.

A, B, M, N: Rail to Rail OPAMPs

Ordering Information

EC5575AN XX - X

— T : Tray

— GH : TQFP-48L(Exposed Pad)
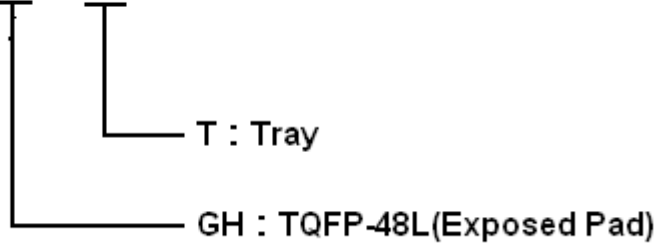
Part No.	Top Mark	Package	Description
EC5575ANGHT	AS15-HF YYWWT LLLLLLLL	TQFP-48L (Exposed Pad)	YYWW is date code, LLLLLLL is lot no. T：Tracking Code

ABSOLUTE MAXIMUM RATINGS (T$_A$ = 25 °C)

Values beyond absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional device operation is not implied. Exposure to AMR conditions for extended periods may affect device reliability.

Supply Voltage between V$_{S+}$ and V$_{S-}$	+18V	Storage Temperature	-65°C to +150°C
Input Voltage (For rail-to-rail)	V$_{S-}-0.5$V, V$_{S+}+0.5$V	Operating Temperature	-40°C to +85°C
Maximum Continuous Output Current (A ~ N Buffers)	30mA	Lead Temperature	260°C
Maximum Continuous Output Current(Com Buffer)	100mA	ESD Voltage	2kV
Maximum Die Temperature	+150°C		

Important Note:

All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T$_J$ = T$_C$ = T$_A$

ELECTRICAL CHARACTERISTICS

V$_{S+}$= +5V, V$_{S-}$ = -5V, R$_L$ = 10kΩ and C$_L$ = 10pF , T$_A$ = 25°C unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Units
Input Characteristics						
V$_{OS}$	Input Offset Voltage	V$_{CM}$= 0V		2	12	mV
TCV$_{OS}$	Average Offset Voltage Drift [1]			5		µV/°C
I$_B$	Input Bias Current	V$_{CM}$= 0V		2	50	nA
R$_{IN}$	Input Impedance			1		GΩ
C$_{IN}$	Input Capacitance			1.35		pF
Output Characteristics						
V$_{OL}$	Output Swing Low	I$_L$= -5mA (A, B, M, N, Com Buffers)		-4.92	-4.85	V
V$_{OH}$	Output Swing High	I$_L$= 5mA (A, B, M, N, Com Buffers)	4.85	4.92		V
V$_{OL}$	Output Swing Low	I$_L$= -5mA (C ~ L Buffers)	-3.5			V
V$_{OH}$	Output Swing High	I$_L$= 5mA (C ~ L Buffers)	3.5			V
I$_{SC(A~N)}$	Short Circuit Current	(A ~ N Buffers)		±120		mA
I$_{OUT(A~N)}$	Output Current	(A ~ N Buffers)		±30		mA
I$_{SC(Com)}$	Short Circuit Current	(Com Buffer)		±300		mA
I$_{OUT(Com)}$	Output Current	(Com Buffer)		±100		mA
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	V$_S$ is moved from ±3.25V to ±7.75V	60	80		dB
I$_{S(A~R)}$	Supply Current (Per Amplifier)	No Load (A ~ N Buffers)		500	750	µA
I$_{S(Com)}$	Supply Current	(Com Buffer)		3		mA
Dynamic Performance						
SR$_{A~R}$	Slew Rate [2]	-4.0V≦V$_{OUT}$≦4.0V, 20% to 80%		2		V/µs
SR$_{Com}$	Slew Rate [2]	-4.0V≦V$_{OUT}$≦4.0V, 20% to 80%		30		V/µs
t$_S$	Settling to +0.1% (AV = +1)	(AV = +1), V$_O$=2V Step		5		µs
BW$_{A~R}$	-3dB Bandwidth	RL = 10KΩ, CL = 10PF		2		MHz
BW$_{Com}$	-3dB Bandwidth	RL = 10KΩ, CL = 10PF		30		MHz
PM	Phase Margin	RL = 10KΩ, CL = 10PF		60		Degrees
CS	Channel Separation	f = 1 MHz		75		dB
Temperature Performance						
Temp	Thermal Shutdown			150		℃

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges

APPLICATIONS INFORMATION

Product Description
The EC5575A rail-to-rail 14+1 channel voltage buffers are built on an advanced high voltage CMOS process. It's beyond rails input capability and full swing of output range made itself an ideal amplifier for use in a wide range of general-purpose applications. The features of high slew rate (Vcom: 30V/μs, Gammas: 2V/μs), fast settling time, high unity-gain bandwidth (Vcom: 30MHz, Gammas: 2MHz) as well as high output driving capability have proven the EC5575A a good voltage reference buffer in TFT-LCD for grayscale reference applications. High phase margin and extremely low power consumption (Vcom: 3mA, Gammas: 500μA) make the EC5575A ideal for connected in voltage follower mode for low power high drive applications.

Supply Voltage, Input Range and Output Swing
The EC5575A can be operated with a single nominal wide supply voltage ranging from 6V to 18V with stable performance over operating temperatures of -20 °C to +85 °C. With 500mV greater than rail-to-rail input common mode voltage range and 75dB of Common Mode Rejection Ratio, the EC5575A allows a wide range sensing among many applications without having any concerns over exceeding the range and no compromise in accuracy. The output swings of the EC5575A typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. The output voltage swing can be even closer to the supply rails by merely decreasing the load current. Figure 1 shows the input and output waveforms for the device in the unity-gain configuration. The amplifier is operated under 10V supply with a 10K Ω and 10pF load connected to GND. The input is a 10Vp-p sinusoid. An approximately 9.985 Vp-p of output voltage swing can be easily achieved.
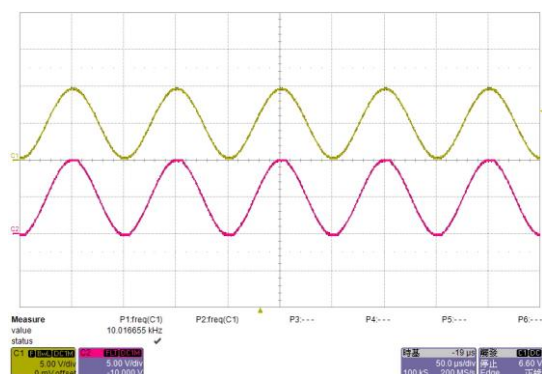

Figure 1. Operation with Rail-to-Rail Input and Output

Output Short Circuit Current Limit
An output short circuit current (Vcom: ±300mA, Gammas: ±120mA) will be limited by the EC5575A if the output is directly shorted to the positive or the negative supply. For an indefinitely output short circuit, the power dissipation could easily increase such that the device may be damaged. The internal metal interconnections are well designed to prevent the output continuous current from exceeding ±30mA for gammas and ±100mA for Vcom such that the maximum reliability can be well maintained.

Output Phase Reversal
The EC5575A is designed to prevent its output from being phase reversal as long as the input voltage is limited from $V_{S-} - 0.5V$ to $V_{S+} + 0.5V$. Figure 2 shows a photo of the device output with its input voltage driven beyond the supply rails. Although the phase of the device's output will not be reversed, the input's over-voltage should be avoided. An improper input voltage exceeds supply range by more than 0.6V may result in an over stress damage.
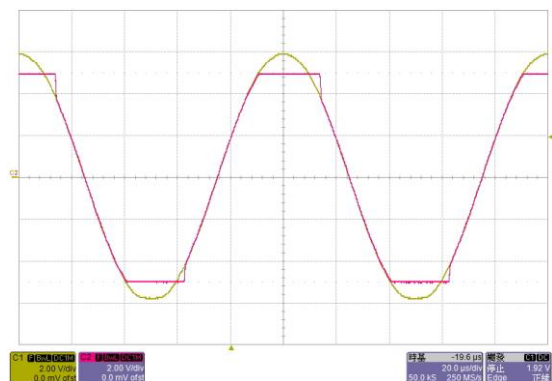

Figure 2. Operation with Beyond-the Rails Input

Power Dissipation
The EC5575A is designed for maximum output current capability. Even though momentary output shorted to ground causes little damage to the device.

For the high drive amplifier EC5575A, it is possible to exceed the 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area. The maximum power dissipation allowed in a package is determined according to:

$$P_{Dmax} = \frac{T_{Jmax} - T_{Amax}}{\Theta_{JA}}$$

Where:
T_{Jmax} = Maximum Junction Temperature
T_{Amax} = Maximum Ambient Temperature
Θ_{JA} = Thermal Resistance of the Package
P_{Dmax} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:
$$P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_{S+} - V_O) * I_L]$$
When sourcing, and
$$P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_O - V_{S-}) * I_L]$$
When sinking.

Where:
i = 1 to 15

V_S = Total Supply Voltage
I_{Smax} = Maximum Supply Current Per Amplifier
V_O = Maximum Output Voltage of the Application

I_L = Load current
R_L = Load Resistance = $(V_{S+} - V_O)/I_L = (V_O - V_{S-})/I_L$

A calculation for R_L to prevent device from overheat can be easily solved by setting the two P_{Dmax} equations equal to each other.
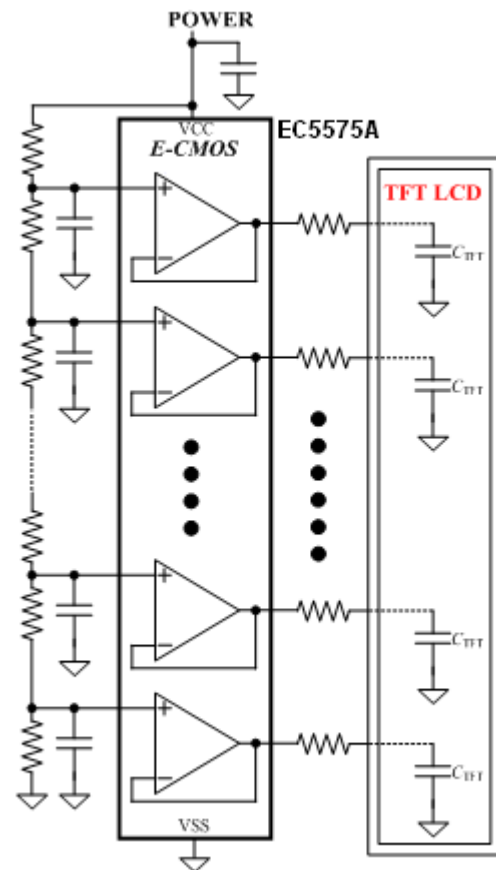
Driving Capacitive Loads
The EC5575A is designed to drive a wide range of capacitive loads. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features make the EC5575A ideally for applications such as TFT LCD panel grayscale reference voltage buffers, ADC input amplifiers, etc.
As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. Depending on the application, it must be necessary to reduce peaking and to improve device stability. To improve device stability, a small value of series resistor (usually between 5Ω and 50Ω) must be placed in series with the output. The advantage is that it improves the settling and overshooting performance with very large capacitive loads. Figure 3 shows the typical application configuration.

Figure 3. Typical Application Configuration.

Power Supply Bypassing and Printed Circuit Board Layout
With high phase margin, the EC5575A performs stable gain at high frequency. Like any high-frequency device, good layout of the printed circuit board usually comes with optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{S-} pin is connected to ground, a 0.1 µF ceramic capacitor should be placed from V_{S+} pin to V_{S-} pin as a bypassing capacitor. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

OUTLINE DIMENSIONS (Dimensions shown in millimeters)

TQFP-48(Exposed pad)

THERMALLY ENHANCED VARIATIONS ONLY
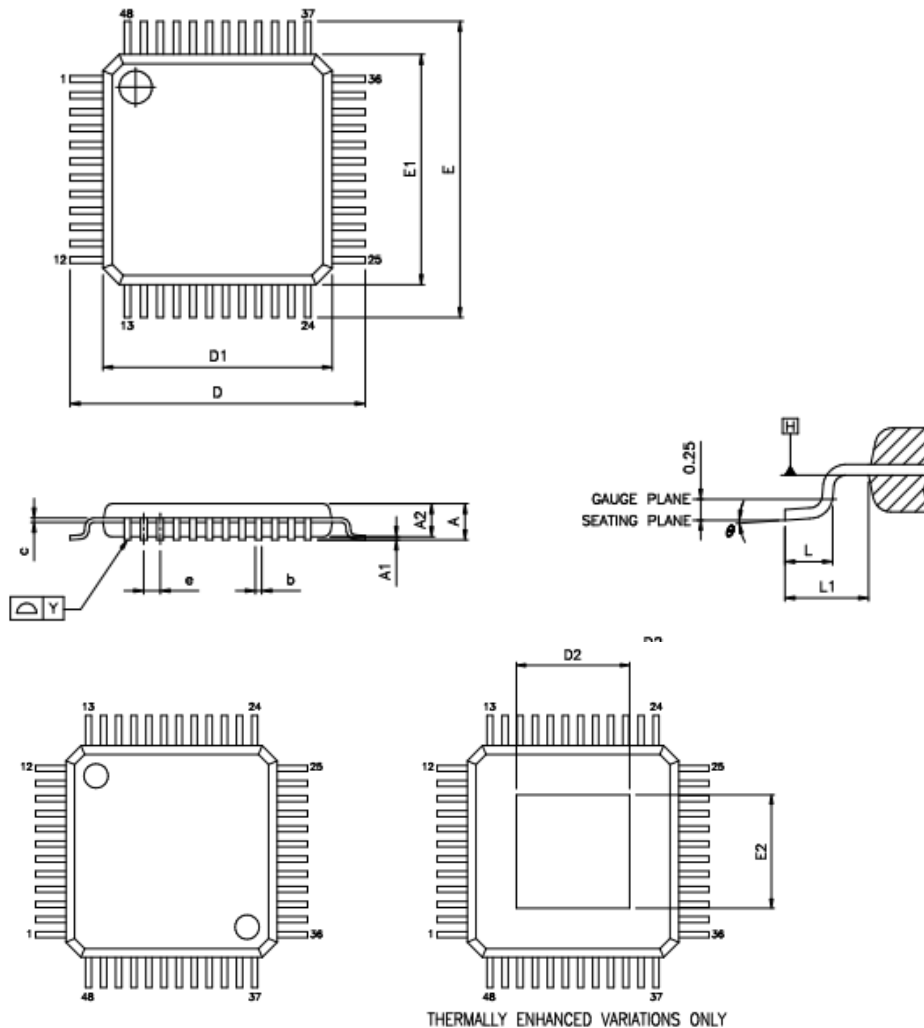
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	——	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
Y	0.08		

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
	4.00	4.20	4.00	4.20

NOTES:
1. JEDEC OUTLINE :
   MS−026 ABC
   MS−026 ABC−HD(THERMALLY ENHANCED VARIATIONS ONLY)
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H] .
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

E-CMOS Corp. (www.ecmos.com.tw)   3K29N-Rev. F001

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