WINSTAR Display

OLED SPECIFICATION

Model No:

WEO012864BLPP3N00000

OLED Specification

Contents

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WINSTAR

WINSTAR Display

華凌光電股份有限公司

Technology - Innovation - Value

Eco Friendly - Revolution

WIN YOUR LIFE, STAR YOUR EYES

SPECIFICATION Ver:0

CUSTOMER :

MODULE NO. : WEO012864BLPP3N00000

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION: DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2012/09/17		First issue

1. Module Classification Information

W E O 012864 B L P P 3 N 00000

1 2 3 4 5 6 7 8 ⑨ ⑩ □□ □

1	Brand：WINSTAR DISPLAY CORPORATION		
2	E：OLED		
3	Display Type：H→Character Type, G→Graphic Type, O→COG Type		
4	Number of dots： 128*64 Dots		
5	Serials code		
6	Emitting Color	A：Amber	R：RED
		B：Blue	C：Full color
		G：Green	W：White
		Y：Yellow Green	L：Yellow
7	Polarizer	P：With Polarizer; N: Without Polarizer	
8	Display Mode	P：Passive Matrix ; A: Active Matrix	
9	Driver Voltage	3: 3.0 V; 5: 5.0V	
10	Touch Panel	N：Without touch panel; T: With touch panel	
11	Products type	0：Standard type 1. Sunlight Readable type 2. Transparent OLED (TOLED) 3. Flexible OLED 4. OLED for Lighting	
12	Product grades	product grades: 0：Standard(A-level) 2：B-level 3：C-level 4：high class(AA-level) 5：Customer offerings	
13	Serial No.	Application serial number(00~ZZ)	

2. General Description

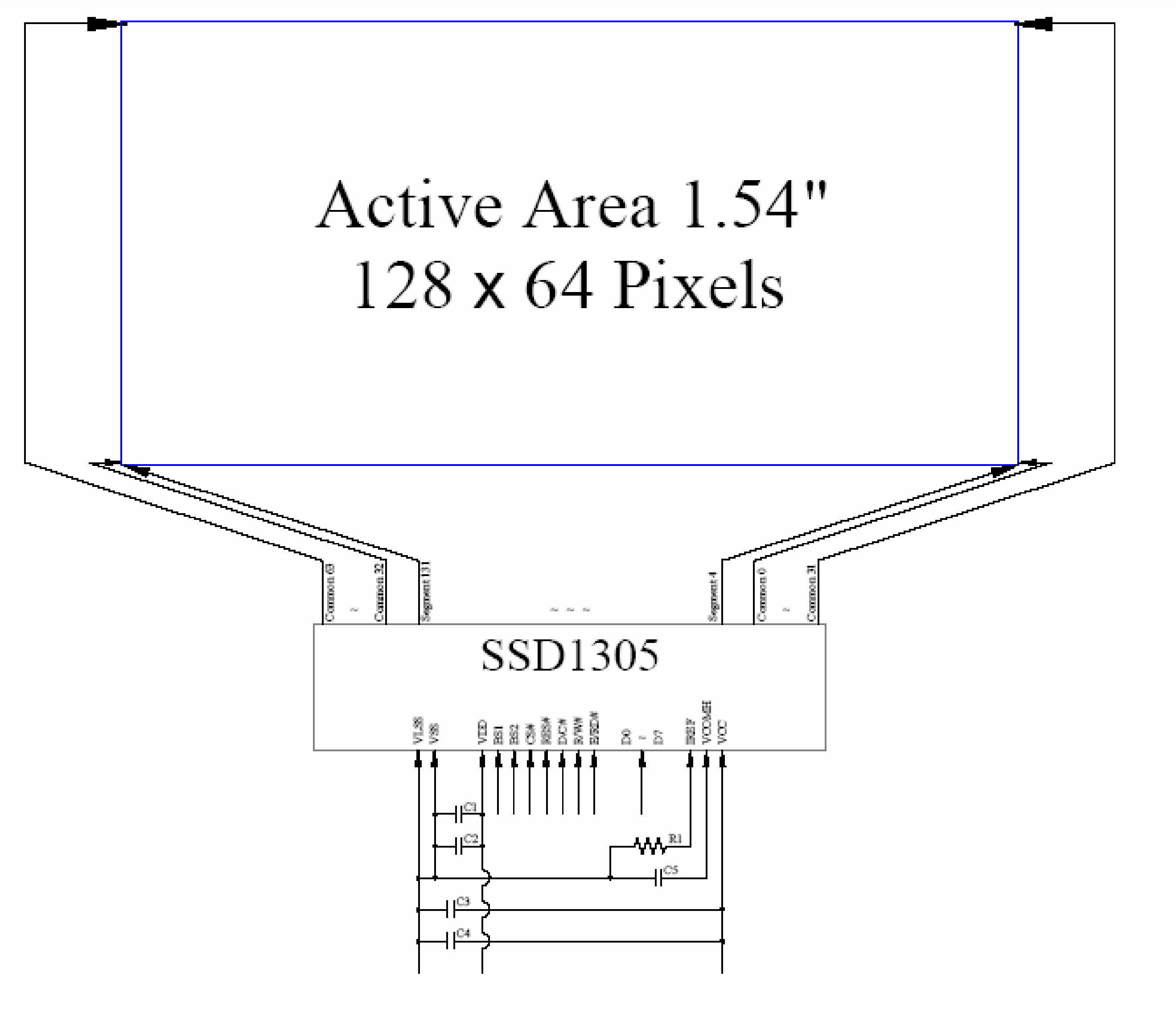
Item	Dimension	Unit
Number of Characters	128 x 64 Dots	—
Module dimension	45.24 × 29.14 × 2.05 (mm)	mm
Active Area	35.056 × 17.52 (mm)	mm
Pixel Pitch	0.274 × 0.274 (mm)	mm
Pixel Size	0.258 × 0.258 (mm)	mm
Display Mode	Passive Matrix	
Display Color	Yellow	
Drive Duty	1/64 Duty	

3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	4	V	1,2
Supply Voltage for Display	VCC	0	15	V	1,2
Operating Temperature	TOP	-40	80	℃	—
Storage Temperature	TSTG	-40	80	℃	—

Note 1: All the above voltages are on the basis of “VSS = 0V”.
Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.“Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

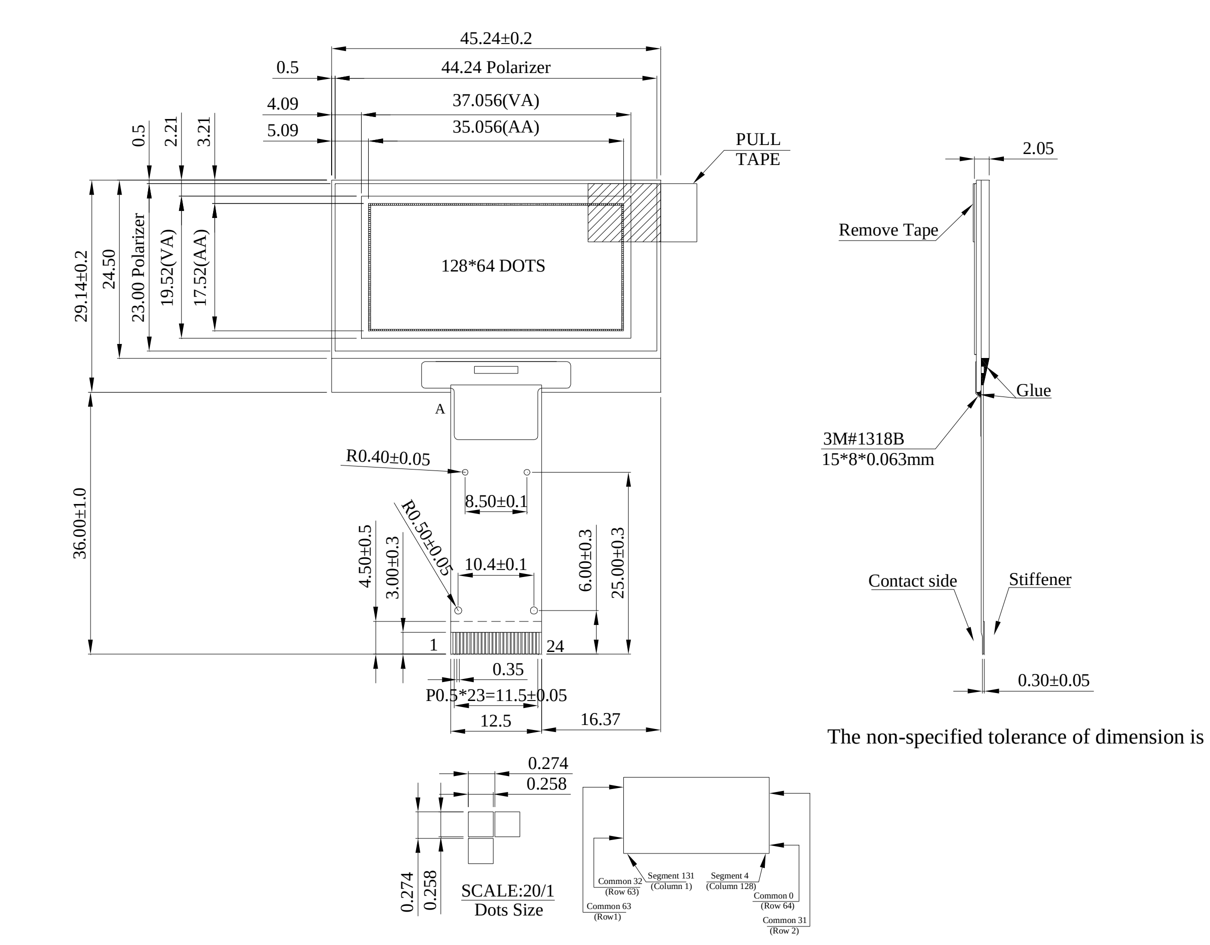
4. Block Diagram



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7
C1, C3: 0.1μF
C2: 4.7μF
C4: 10μF
C5: 4.7μF / 25V Tantalum Capacitor

R1: 910kΩ, R1 = (Voltage at IREF - VSS) / IREF

5. Contour Drawing



PIN NO.	SYMBOL
1	NC(GND)
2	VLSS
3	VSS
4	NC
5	VDD
6	BS1
7	BS2
8	CS#
9	RES#
10	D/C#
11	R/W#
12	E/RD#
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	IREF
22	VCOMH
23	VCC
24	GND

The non-specified tolerance of dimension is ±0.2mm.

6. Interface Pin Function

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>NC(GND)</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</td></tr>
<tr><td>2</td><td>VLSS</td><td>Ground of Analog Circuit
This is an analog ground pin. It should be connected to VSS externally.</td></tr>
<tr><td>3</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>NC</td><td>Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>5</td><td>VDD</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>6</td><td>BS1</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table><tr><th></th><th>68XX-parallel</th><th>80XX-parallel</th><th>Serial</th><th>I2C</th></tr><tr><td>BS1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>BS2</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table></td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>8</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low</td></tr>
<tr><td>9</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>10</td><td>D/C#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>11</td><td>R/W#</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.</td></tr>
</table>

12	E/RD#	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
13~20	D0~D7	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
21	IREF	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10μA.
22	VCOMH	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
23	VCC	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. It must be supplied externally.
24	GND	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

7. Optics & Electrical Characteristics

7.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	100	-	-	cd/m^2
C.I.E. (Yellow)	(x) (y)	Without Polarizer	0.43 0.46	0.47 0.50	0.51 0.54	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.5V.
Software configuration follows Section 4.4 Initialization.

7.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		2.4	2.8	3.5	V
Supply Voltage for Display	V_{CC}	Note 3	14.5	15.0	15.5	V
High Level Input	V_{IH}	I_{OUT}= 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT}= 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT}= 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT}= 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}	Note 4 Note 5	--	180 180	300 300	μA μA
Operating Current for V_{CC}	I_{CC}	Note 4 Note 5	--	60 72	100 120	mA mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	5	μA

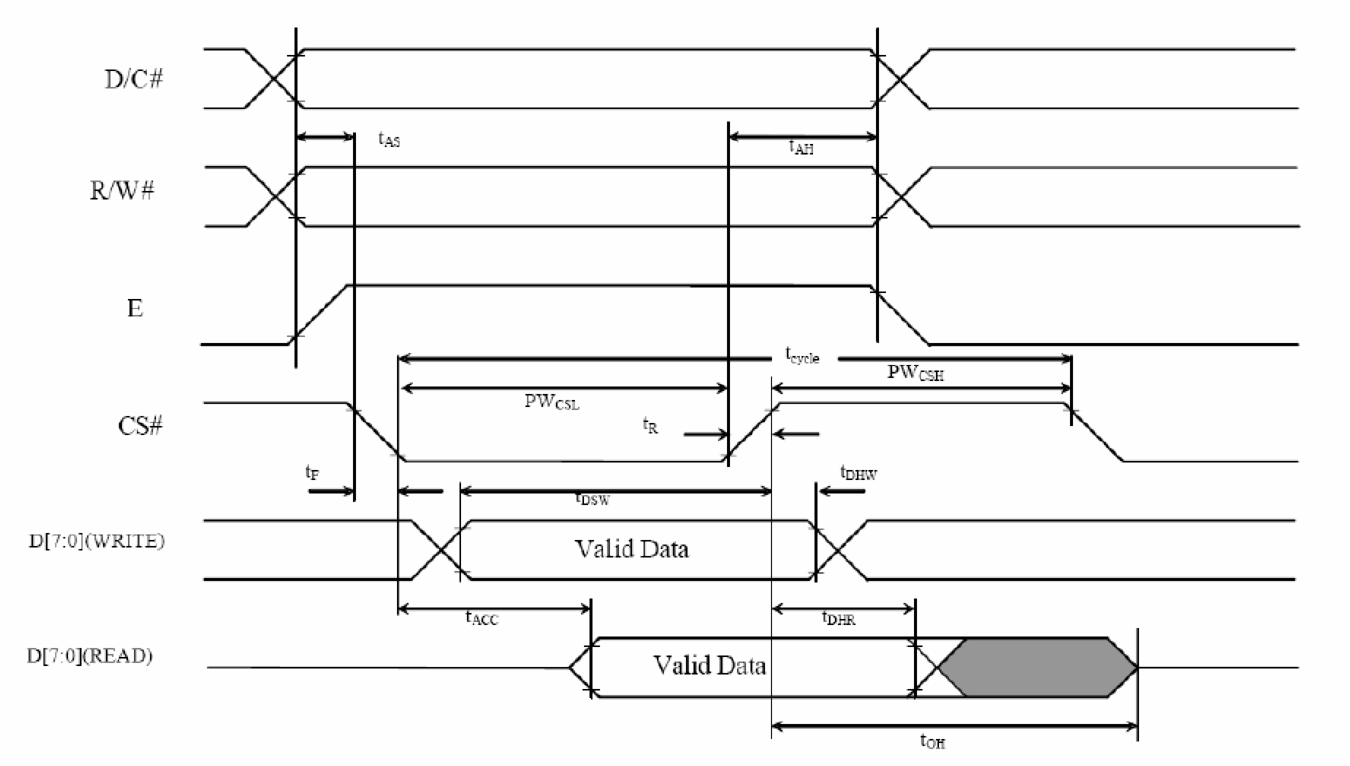
Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{DD} = 2.8V, V_{CC} = 12.5V, 50% Display Area Turn on.
Note 5: V_{DD} = 2.8V, V_{CC} = 12.5V, 100% Display Area Turn on.
* Software configuration follows Section 4.4 Initialization.

7.3 AC Characteristics

7.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	System Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

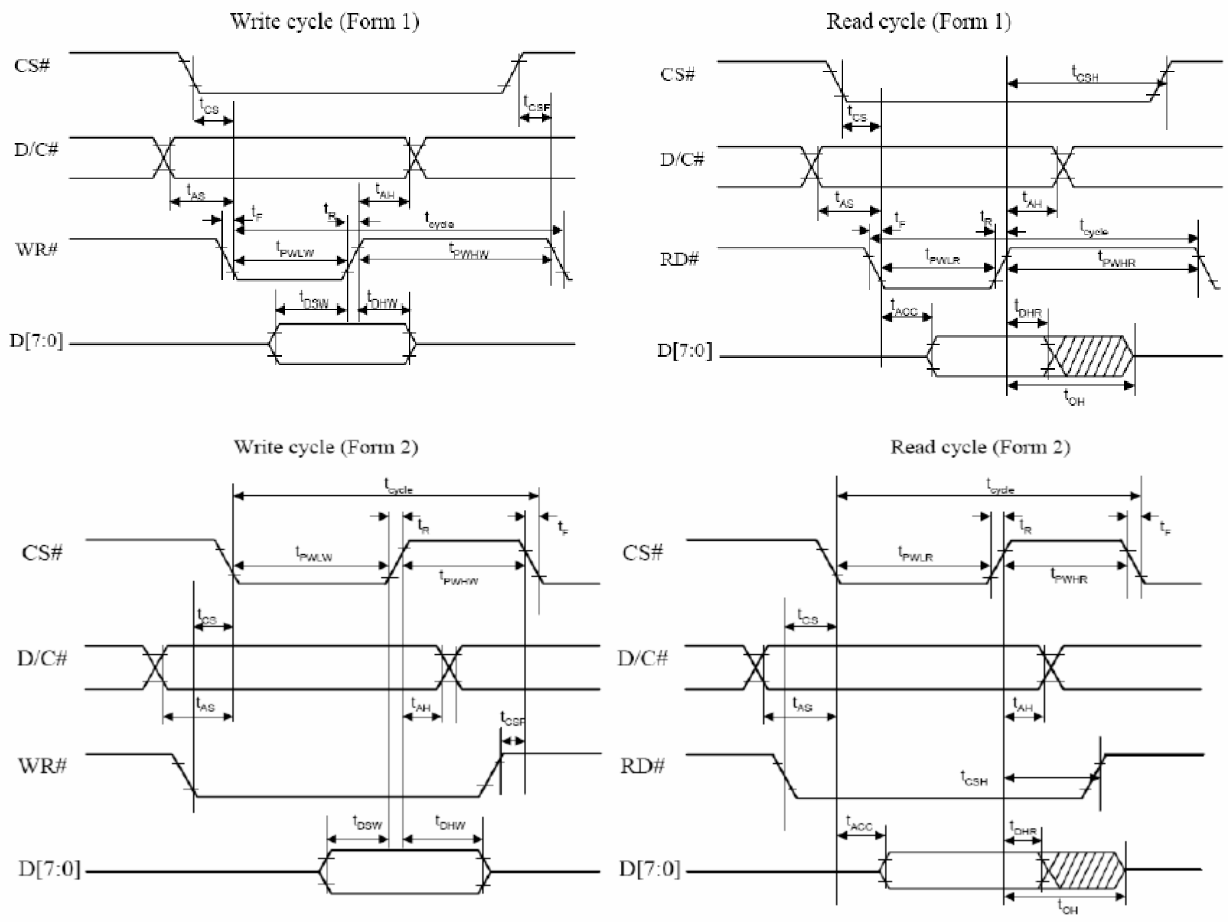
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)



7.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

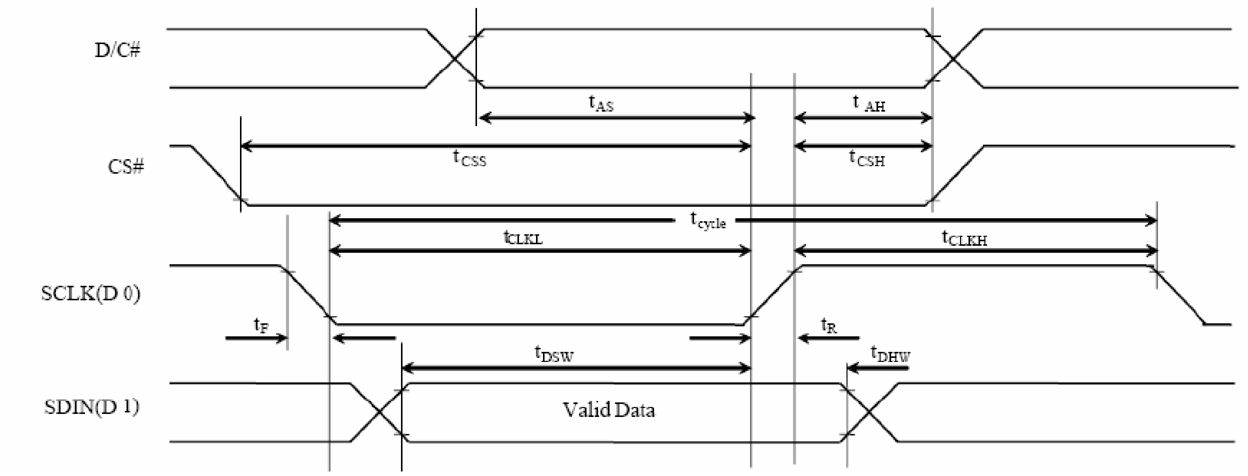
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)

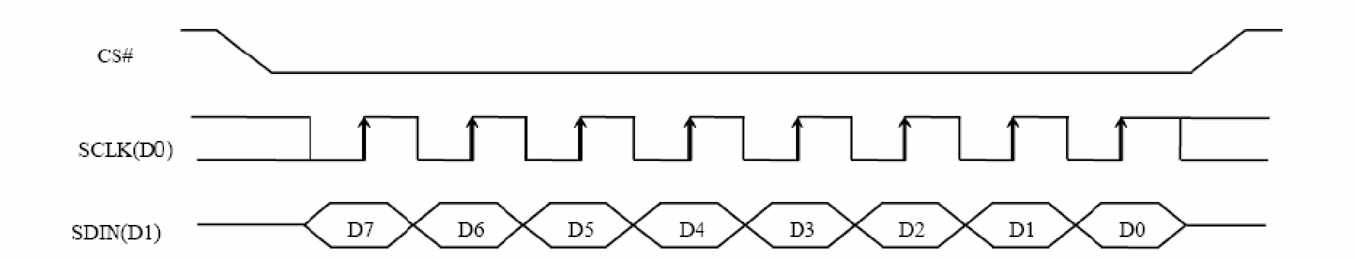


7.3.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	50	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Serial Clock Low Time	100	-	ns
t_{CLKH}	Serial Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)

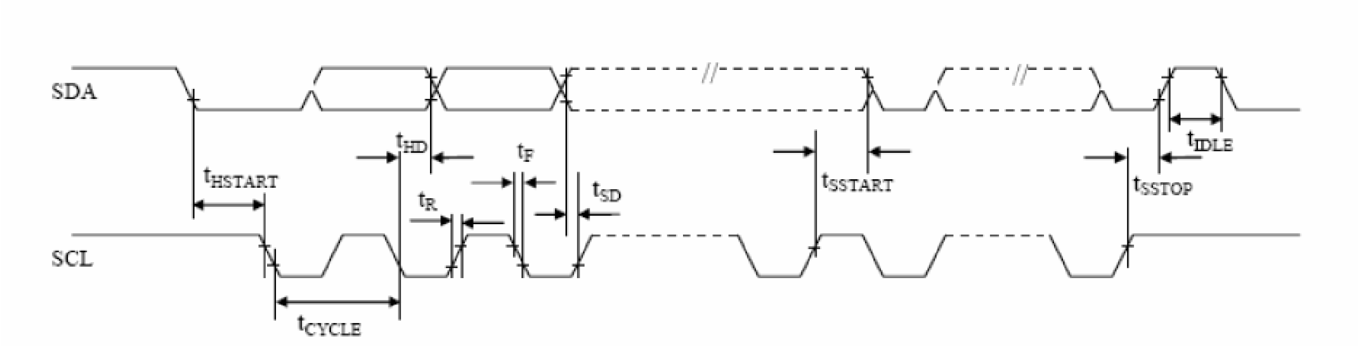




7.3.4 I2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for “SDA_{OUT}” Pin) Data Hold Time (for “SDA_{IN}” Pin)	0 300	-	ns
t_{SD}	Data Setup Time	100	-	ns
	Start Condition Setup Time			
t_{SSTART}	(Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25℃)



8. Reliability

8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	80℃, 240 hrs	The operational functions work.
Low Temperature Operation	-40℃, 240 hrs	
High Temperature Storage	80℃, 240 hrs	
Low Temperature Storage	-40℃, 240 hrs	
HighTemperature/Humidity Storage	60℃, 90% RH, 240 hrs	
Thermal Shock	-40℃ ⇔80℃, 24 cycles 1 hr dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

8.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

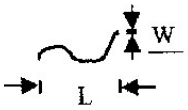
Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	10,000	-	hr	100 cd/m$_2$,50%Checkerboard	6
	40,000	-	hr	100 cd/m$_2$, 50% Checkerboard	

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

8.3 Failure Check Standard

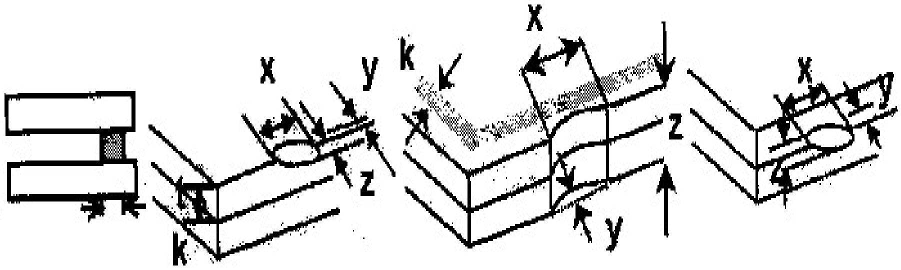
After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5℃; 55±15% RH.

9. Inspection specification

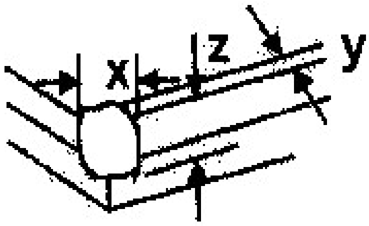
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 OLED viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on OLED (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">OLED black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)


<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size Φ</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

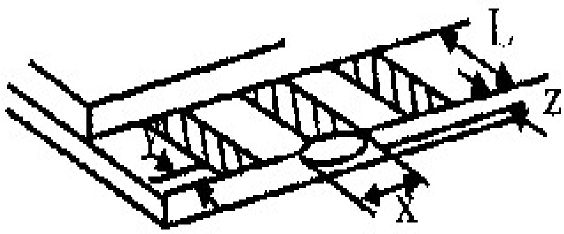
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 OLED black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: OLED side length
L: Electrode pad length:

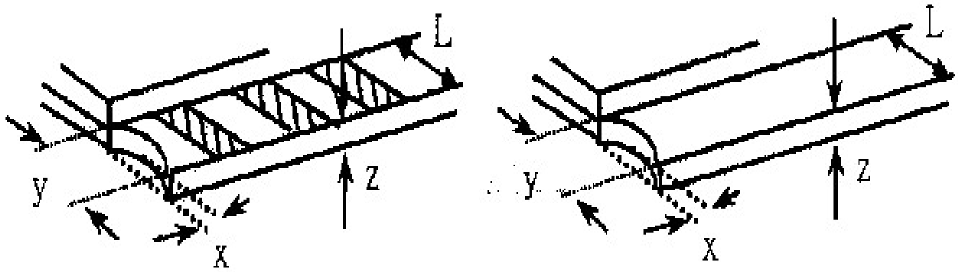
6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:


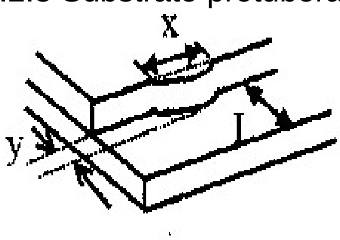
<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is total length of each chip.

6.1.2 Corner crack:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is the total length of each chip.</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: OLED side length
L: Electrode pad length
6.2 Protrusion over terminal :
6.2.1 Chip on electrode pad :


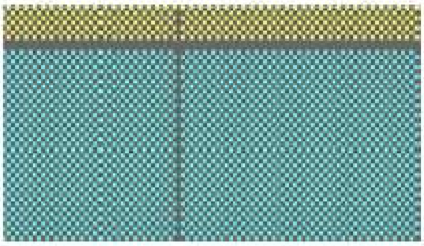
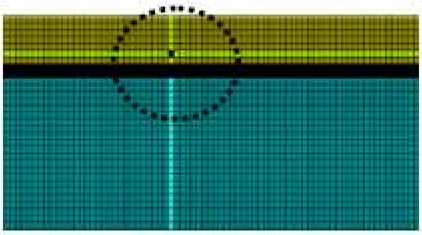
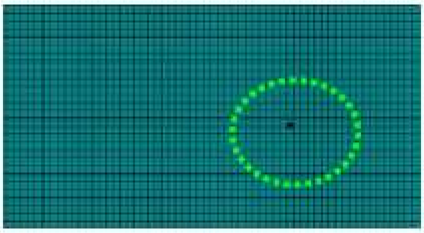
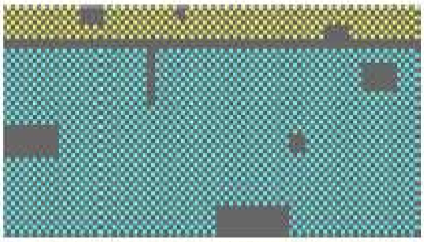
<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.
6.2.3 Substrate protuberance and internal crack.


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
07	Cracked glass	The OLED with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using OLED spot, lines and contamination standards. 8.3 Backlight doesn’t light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major