ATA45 Series FLASH CARDS 8MB to 512MB

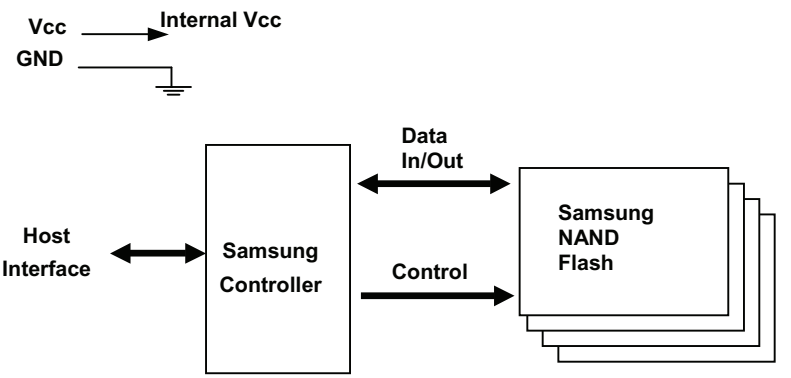
PRODUCT DESCRIPTION

ATA45 series Flash ATA cards are built with NAND flash memory components operating as solid-state disk. They comply with the PC card ATA standard and are suitable for use as a data storage memory medium for PCs or other electronic equipment. The read/write unit is 1 sector (512 bytes) sequential access.

FEATURES

- PC Card-ATA/True IDE/ I/O Card mode compatible host interface
  - 68 pin connector and type II stainless steel housing
  - Automatic sensing of PC Card ATA and IDE mode
  - Included 256-byte CIS ROM
  - Support the five PC Card ATA addressing modes
  - Host Interface bus width: 8/16-bit Access
  - Flash Interface bus width: 8-bit Access
  - Support 3 power save mode: standby / idle / active
  - Auto power down function
  - 2-bit ECC function
- Operating Voltage: 3.3 V and 5.0 V
- ISA standard and Read/Write unit is 512 bytes (sector) sequential access
- High performance:
  - Host data transfer rate 20.0 MB/sec
  - Flash data transfer rate 10.0 MB/sec
- Maximum card density is 512 MB
- 3 variations of mode access
  - Memory card mode
  - I/O card mode
  - True-IDE mode
- Internal self-diagnostic program operates at V_{CC} power on
- High data reliability
  - Endurance: 100,000 Program / Erase cycles
  - High reliability based on internal ECC (Error Correcting Code) function 2-bit ECC
  - Data reliability is 1 error in 10^{14} bits read.
- Power Consumption
  - Active mode 30 mA (typ.), 40 mA (max.)
  - Idle mode 10 mA
  - Stop mode 400 µA

CARD BLOCK DIAGRAM



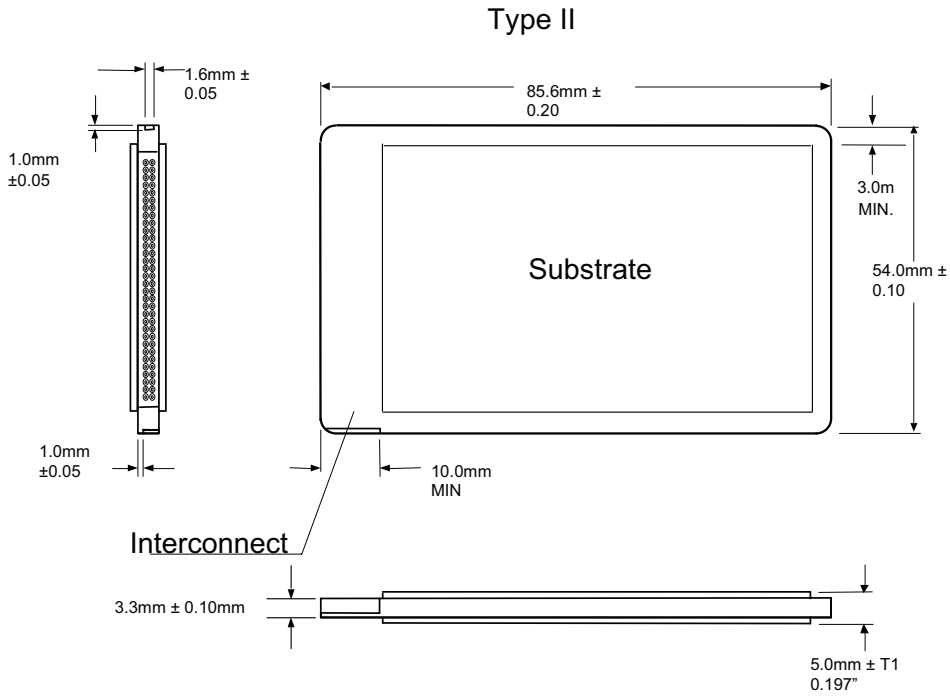
CARD CAPACITIES (CF TYPE I BLANK HOUSING)

Capacity	Part Number	Sectors/Card	Cylinder	Sector/Track	Heads
8 MB	WED7P008ATA4504C25	15,616	122	32	4
16 MB	WED7P016ATA4504C25	31,488	246	32	4
32 MB	WED7P032ATA4504C25	62,976	492	32	4
48 MB	WED7P048ATA4504C25	94,464	738	32	4
64 MB	WED7P064ATA4504C25	125,952	246	32	16
96 MB	WED7P096ATA4504C25	188,928	369	32	16
128 MB	WED7P128ATA4504C25	251,904	492	32	16
256 MB	WED7P256ATA4504C25	503,808	984	32	16
512 MB	WED7P512ATA4504C25	1,029,168	1,021	63	16

PHYSICAL SPECIFICATION

The ATA45 series physical specification complies with PCMCIA standard card format.

CARD SIZE AND OUTLINE



INTERFACE SPECIFICATION

SIGNAL PIN ASSIGNMENTS

Pin NO.	Memory Card Mode Signal name	I/O	I/O Card Mode Signal name	I/O	True IDE Mode Signal name	I/O
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	$\overline{CE1}$	I	$\overline{CE1}$	I	$\overline{CE1}$	I
8	A10	I	A10	I	A10	I
9	$\overline{OE}$	I	$\overline{OE}$	I	$\overline{ATASEL}$	I
10	—	—	—	—	—	—
11	A9	I	A9	I	A9	I
12	A8	I	A8	I	A8	I
13	—	—	—	—	—	—
14	—	—	—	—	—	—
15	$\overline{WE}$	I	$\overline{WE}$	I	$\overline{WE}$	I
16	RDY/$\overline{BSY}$	O	$\overline{IREQ}$	O	INTRQ	O
17	VCC	—	VCC	—	VCC	—
18	—	—	—	—	—	—
19	—	—	—	—	—	—
20	—	—	—	—	—	—
21	—	—	—	—	—	—
22	A7	I	A7	I	A7	I
23	A6	I	A6	I	A6	I
24	A5	I	A5	I	A5	I
25	A4	I	A4	I	A4	I
26	A3	I	A3	I	A3	I
27	A2	I	A2	I	A2	I
28	A1	I	A1	I	A1	I
29	A0	I	A0	I	A0	I
30	D0	I/O	D0	I/O	D0	I/O
31	D1	I/O	D1	I/O	D1	I/O
32	D2	I/O	D2	I/O	D2	I/O
33	WP	O	$\overline{IOIS16}$	O	$\overline{IOIS16}$	O
34	GND	—	GND	—	GND	—
35	GND	—	GND	—	GND	—
36	$\overline{CD1}$	O	$\overline{CD1}$	O	$\overline{CD1}$	O
37	D11	I/O	D11	I/O	D11	I/O
38	D12	I/O	D12	I/O	D12	I/O
39	D13	I/O	D13	I/O	D13	I/O
40	D14	I/O	D14	I/O	D14	I/O
41	D15	I/O	D15	I/O	D15	I/O
42	$\overline{CE2}$	I	$\overline{CE2}$	I	$\overline{CE2}$	I
43	$\overline{VS1}$	O	$\overline{VS1}$	O	$\overline{VS1}$	O
44	$\overline{IORD}$	I	$\overline{IORD}$	I	$\overline{IORD}$	I
45	$\overline{IOWR}$	I	$\overline{IOWR}$	I	$\overline{IOWR}$	I
46	—	—	—	—	—	—
47	—	—	—	—	—	—
48	—	—	—	—	—	—
49	—	—	—	—	—	—
50	—	—	—	—	—	—

SIGNAL PIN ASSIGNMENTS CONT.

Pin NO.	Memory Card Mode Signal name	I/O	I/O Card Mode Signal name	I/O	True IDE Mode Signal name	I/O
51	VCC	—	VCC	—	VCC	—
52	—	—	—	—	—	—
53	—	—	—	—	—	—
54	—	—	—	—	—	—
55	—	—	—	—	—	—
56	$\overline{\text{CSEL}}$	I	$\overline{\text{CSEL}}$	I	$\overline{\text{CSEL}}$	I
57	$\overline{\text{VS2}}$	O	$\overline{\text{VS2}}$	O	$\overline{\text{VS2}}$	O
58	RESET	I	RESET	I	RESET	I
59	$\overline{\text{WAIT}}$	O	$\overline{\text{WAIT}}$	O	IORDY	O
60	$\overline{\text{INPACK}}$	O	$\overline{\text{INPACK}}$	O	$\overline{\text{INPACK}}$	O
61	$\overline{\text{REG}}$	I	$\overline{\text{REG}}$	I	$\overline{\text{REG}}$	I
62	BVD2	I/O	$\overline{\text{SPKR}}$	I/O	$\overline{\text{DASP}}$	I/O
63	BVD1	I/O	$\overline{\text{STSCHG}}$	I/O	$\overline{\text{PDIAG}}$	I/O
64	D8	I/O	D8	I/O	D8	I/O
65	D9	I/O	D9	I/O	D9	I/O
66	D10	I/O	D10	I/O	D10	I/O
67	$\overline{\text{CD2}}$	O	$\overline{\text{CD2}}$	O	$\overline{\text{CD2}}$	O
68	GND	—	GND	—	GND	—

INTERFACE SIGNALS DESCRIPTION

Symbol	Type	Name and Function
A_0 - A_{10}	INPUT	**ADDRESS BUS:** These address lines along with the $\overline{REG}$ signal are used to select the following: The I/O port address registers within the PC Storage Card, the memory mapped port address registers within the PC Storage Card, a byte in the Card's information structure and its configuration control and status registers. This signal is the same as the PC Card Memory Mode signal in PC Card I/O mode. In True IDE Mode only A [2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
D_0 - D_{15}	INPUT/ OUTPUT	**DATA BUS:** These signal lines carry the Data, Commands and Status information between the host and the controller. D_0 is the LSB of the even byte of the word. D_8 is the LSB of the odd byte of the word. This signal is the same as the PC Card memory mode signal in PC Card I/O mode. In True IDE mode, all Task File operations occur in byte mode on the low order bus D_0-D_7 while all data transfers are 16 bit using D_0–D_{15}.
$\overline{CE_1}$, $\overline{CE_2}$	INPUT	**CARD ENABLE:** $\overline{CE_1}$ and $\overline{CE_2}$ are card select signals, active low. These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. $\overline{CE_2}$ always accesses the odd byte of the word. $\overline{CE_1}$ accesses the even byte or the Odd byte of the word depending on A_0 and $\overline{CE_2}$. A multiplexing scheme based on A_0, $\overline{CE_1}$, $\overline{CE_2}$ allows 8 bit hosts to access all data on D_0-D_7. This signal is the same as the PC card memory mode signal in PC Card I/O mode. In the True IDE mode, CE_1 is the chip select for the task file registers while CE_2 is used to select the Alternate Status Register and the Device Control Register.
$\overline{OE}$, $\overline{ASTEL}$	INPUT	**OUTPUT ENABLE, ATA SELECT:** $\overline{OE}$ is used for the control of data read in Attribute area or Common memory area. To enable True IDE Mode this input should be grounded by the host (in power up).
$\overline{WE}$	INPUT	**WRITE ENABLE:** $\overline{WE}$ is used for the control of data write in Attribute memory area or Common memory area. This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O mode, this signal is used for writing the configuration registers. In True IDE mode, this input signal is not used and should be connected to VCC by the host.
$\overline{IORD}$	INPUT	**I/O READ:** $\overline{IORD}$ is used for control of read data in the Task File area. This card does not respond to $\overline{IORD}$ until I/O card interface setting up.
$\overline{IOWR}$	INPUT	**I/O WRITE:** $\overline{IOWR}$ is used for control of data write in the Task File area. This card does not respond to $\overline{IOWR}$ until I/O card interface setting up. This signal is not used in memory mode. The I/O write strobe pulse is used to clock I/O data on the card data bus into the PC Card controller registers when the PC Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). In True IDE mode, this signal has the same function as in PC Card I/O Mode.
RDY/$\overline{BSY}$, $\overline{IREQ}$, INTRQ	OUTPUT	**READY/BUSY INTERRUPT REQUEST:** In memory mode, this signal is set high when the PC Card is ready to accept a new data transfer operation and held low when the card is busy. The host memory card socket must provide a pull-up resistor. At power up and at reset, the RDY/$\overline{BSY}$ signal is held low (busy) until the PC Card has completed its power up or reset function. No access of any type should be made to the PC Card during this time. The RDY/$\overline{BSY}$ signal is held high (disabled from being busy) whenever the following condition is true: The PC Card has been powered up with RESET continuously disconnected or asserted. I/O operation - After the PC Card has been configured for I/O operation, this signal is used as Interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE mode, this signal is the active high Interrupt request to the host.
$\overline{CD_1}$, $\overline{CD_2}$	OUTPUT	**CARD DETECTION:** $\overline{CD_1}$ and $\overline{CD_2}$ are the card detection signals. $\overline{CD_1}$ and $\overline{CD_2}$ are connected to ground in this card, so the host can detect if the card is inserted or not.
WP, $\overline{IOIS16}$	OUTPUT	**WRITE PROTECT, 16 BIT I/O PORT:** In memory card mode, WP is held low because this card does not have a write protect switch. In the I/O card mode, $\overline{IOIS16}$ is asserted when Task File registers are accessed in 16-bit mode. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.
$\overline{REG}$	INPUT	**ATTRIBUTE MEMORY AREA SELECTION:** $\overline{REG}$ should be high level during common memory area accessing, and low level during Attribute area accessing. The attribute memory area is located only in an even address, so D_0 to D_7 are valid and D_8 to D_{15} are invalid in the word access mode. Odd addresses are invalid in the byte access mode. The signal must also be active (low) during I/O cycles when the I/O address is on the Bus. In True IDE Mode this input signal is not used and should be connected to VCC.
BVD2, $\overline{SPKR}$, $\overline{DASP}$	INPUT/ OUTPUT	**BATTERY VOLTAGE DETECTION, DIGITAL AUDIO OUTPUT, DISK ACTIVE/SLAVE PRESENT:** In memory card mode, BVD2 outputs the battery voltage status in the card. This card has no battery, so this output is high level constantly. In the I/O card mode, $\overline{SPKR}$ is held High because this card does not have digital audio output. In True IDE Mode $\overline{DASP}$ is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
$\overline{RESET}$, $\overline{RESET}$	INPUT	**RESET:** By assertion of the $\overline{RESET}$ signal, all registers of this card are cleared and the RDY/$\overline{BSY}$ signal turns to high level. In True IDE Mode $\overline{RESET}$ is the active low hardware reset from the host.

INTERFACE SIGNALS DESCRIPTION CONT.

Symbol	Type	Name and Function
$\overline{\text{WAIT}}$, IORDY	OUTPUT	**WAIT:** This signal outputs low level for the purpose of delaying memory access cycle or I/O access cycle. In True IDE Mode this output signal may be used as IORDY. As for this controller, this output is high impedance state constantly.
$\overline{\text{INPACK}}$	OUTPUT	**INPUT ACKNOWLEDGE:** This signal is not used in the memory card mode. The Input acknowledge signal is asserted by the PC Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the PC Card and the CPU. In True IDE mode, this output signal is not used and should be connected to Vcc at the host.
BVD1, $\overline{\text{STSCHG}}$, PDIAG	INPUT/ OUTPUT	**BATTERY VOLTAGE DETECTION, STATUS CHANGE, PASS DIAGNOSTIC:** In the memory card mode, BVD1 outputs the battery voltage status in the card. This card has no battery, so this output is high level constantly. In the I/O card mode, $\overline{\text{STSCHG}}$ is used for changing the status of the Configuration status register in the Attribute area, while the card is set I/O card interface. In True IDE Mode, $\overline{\text{PDIAG}}$ is the Pass Diagnostic signal in the Master/Slave handshake protocol.
$\overline{\text{VS}}_1$, $\overline{\text{VS}}_2$	OUTPUT	**Vcc VOLTAGE SENSE:** These signals are intended to notify the socket of the PC Card's CIS Vcc requirement. $\overline{\text{VS}}_1$ is held low and $\overline{\text{VS}}_2$ is not connected in this card.
$\overline{\text{CSEL}}$	INPUT	**CARD SELECT:** This signal is not used in the memory card mode and I/O card mode. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

PCMCIA-ATA REGISTER MAPPING ADDRESS.

PCMCIA-ATA I/O MAPPING ADDRESS

REG	Primary I/O A[10:0]	Secondary I/O A[10:0]	Independent I/O A[3:0]	IORD = L	IOWR = L
L	1F0H	170H	0H	Read Even Data	Write Even Data
L	1F1H	171H	1H	Error Register	Feature Register
L	1F2H	172H	2H	Sector Count	Sector Count
L	1F3H	173H	3H	Sector Number	Sector Number
L	1F4H	174H	4H	Cylinder Low	Cylinder Low
L	1F5H	175H	5H	Cylinder High	Cylinder High
L	1F6H	176H	6H	Drive/Head	Drive/Head
L	1F7H	177H	7H	Status Register	Command
L	—	—	8H	Duplicate Read Even Data	Duplicate Write Even Data
L	—	—	9H	Duplicate Read Odd Data	Duplicate Write Odd Data
L	—	—	0DH	Duplicate Error	Duplicate Feature
L	3F6H	376H	0EH	Alternate Status	Device Control
L	3F7H	377H	0FH	Drive Address	Reserved

PCMCIA-ATA MEMORY MAPPING ADDRESS

REG	A10	A[9:4]	A[3]	A[2]	A[1]	A[0]	IORD = L	IOWR = L
H	L	X	L	L	L	L	Read Data	Write Data
H	L	X	L	L	L	H	Error Register	Feature
H	L	X	L	L	H	L	Sector Count	Sector Count
H	L	X	L	L	H	H	Sector Number	Sector Number
H	L	X	L	H	L	L	Cylinder Low	Cylinder Low
H	L	X	L	H	L	H	Cylinder High	Cylinder High
H	L	X	L	H	H	L	Drive/Head	Drive/Head
H	L	X	L	H	H	H	Status Register	Command
H	L	X	H	L	L	L	Duplicate Read Even Data	Duplicate Write Even Data
H	L	X	H	L	L	H	Duplicate Read Odd Data	Duplicate Write Odd Data
H	L	X	H	H	L	H	Duplicate Error	Duplicate Feature
H	L	X	H	H	H	L	Alternate Status	Device Control
H	L	X	H	H	H	H	Drive Address	Reserved
H	H	X	X	X	X	L	Read Even Data	Write Even Data
H	H	X	X	X	X	H	Read Odd Data	Write Odd Data

THE ATA REGISTERS AND PCMCIA REGISTERS

STATUS REGISTER

DIRECTION - This register is read-only by the host.

ACCESS RESTRICTION - The contents of this register, except for BSY, will be ignored when BSY is set to one. BSY is valid at all time. The contents of the register and all other Command Block registers are not valid while a device is in the Sleep mode.

FUNCTIONAL DESCRIPTION - This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

BIT 0 ERR (Error) indicates that an error occurred during execution of the previous command. The Error register has additional information regarding the cause of the error when this bit is asserted.

BIT 1 IDX (Index) is vendor specific.

BIT 2 CORR (Corrected Data) is used to indicate a correctable data error. The definition of what constitutes a correctable error is vendor specific.

BIT 3 DRQ (Data Request) indicates that the device is ready to transfer a word or byte between the host and the device.

BIT 4 DSC (Device Seek Complete) indicates that the device heads are settled over a track.

BIT 5 DF (Device Fault) indicates a device fault error has been detected. The internal status or internal conditions that causes this error to be indicated is vendor specific.

BIT 6 DRDY (Device Ready) is set to indicate that the device is capable of accepting all command codes. This bit will be cleared at power on.

BIT 7 BSY (Busy) is set whenever the device has control of the command block registers. When the BSY bit is equal to one, the commands written to this register will be ignored by the device.

COMMAND REGISTER

DIRECTION - This register is write-only by host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero. The contents of this register and all other Command Block registers are not valid while a device is in the Sleep mode.

FUNCTIONAL DESCRIPTION - This register contains the command code being sent to the device. Command execution begins immediately after this register is written.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
Command Code							

ERROR REGISTER

DIRECTION - This register is read-only by host.

ACCESS RESTRICTION - The contents of this register shall be valid when BSY and DRQ are equal to zero and ERR is asserted.

FUNCTIONAL DESCRIPTION - This register contains the operation status for the current command.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
R	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF

BIT 0 AMNF (Address Mark Not Found) indicates the data address mark has not been found after finding the correct ID field.
BIT 1 TKONF (Track 0 Not Found) indicates the track 0 has not been found during a RECALIBRATE command.
BIT 2 ABRT (Aborted Command) indicates the requested command has been aborted because the command code or a command parameter is invalid or some other error has occurred.
BIT 3 MCR (Media Change Requested) is used by removable media devices.
BIT 4 IDNF (ID Not Found) indicates the requested sector's ID field could not be found.
BIT 5 MC (Media Change) is used by removable media devices.
BIT 6 UNC (Uncorrectable Data Error) indicate an uncorrectable data error has been encountered.
BIT 7 Reserved

FEATURE REGISTER

DIRECTION - This register is write-only by host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - This register is command specific.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
Command Specific							

SECTOR NUMBER REGISTER

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the starting sector number for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 7-0 of the LBA for any media access.

BIT DESCRIPTION

CHS

7	6	5	4	3	2	1	0
Sector (7:0)							

LBA

7	6	5	4	3	2	1	0
LBA (7:0)							

SECTOR COUNT REGISTER

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - This register contains the number of sector of data requested to be transferred on a read or write operation between the host and the device. If the value in this register is zero, a count of 256 sectors is specified.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
Sector Count							

CYLINDER LOW REGISTER

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the low order bits of the starting cylinder address for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 15-8 of the LBA for any media access.

BIT DESCRIPTION

CHS

7	6	5	4	3	2	1	0
Cylinder (7:0)							

LBA

7	6	5	4	3	2	1	0
LBA (15:8)							

CYLINDER HIGH REGISTER

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - If the LBA bit is cleared to zero in the Device/Head register, this register contains the low order bits of the starting cylinder address for any media access. If the LBA bit is set to one in the Device/Head register, this register contains Bits 23-16 of the LBA for any media access.

BIT DESCRIPTION

CHS

7	6	5	4	3	2	1	0
Cylinder (7:0)							

LBA

7	6	5	4	3	2	1	0
LBA (15:8)							

DEVICE/HEAD REGISTER

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRICTION - This register is write-only when BSY and DRQ are both equal to zero.

FUNCTIONAL DESCRIPTION - This register selects the device, defines address translation as CHS or LBA, and provides the head address if CHS mode or LBA (27:24) if LBA mode.

BIT DESCRIPTION

CHS (CYLINDER-HEAD-SECTOR)

7	6	5	4	3	2	1	0
1	LBA	1	DEV	HS3	HS2	HS1	HS0

LBA (LOGIC BLOCK ADDRESS)

7	6	5	4	3	2	1	0
1	LBA	1	DEV	LBA	(27:24)		

BIT 0~3 If LBA is equal to zero (CHS), these contain the head address of the starting CHS address. The HS3 bit is the most significant bit. If LBA is equal to one (LBA), these bits represent bits 27 through 24 of the LBA.

BIT 4 DEV is the device address. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected.

BIT 5 Bit 5 is set to one for backward compatibility.

BIT 6 LBA mode if this bit is set to one, otherwise, CHS mode.

BIT 7 Bit 7 is set to one for backward compatibility.

DATA REGISTER

DIRECTION - This register is bi-directional for the drive and host.

ACCESS RESTRUCTIONS - This register can be written or the content is valid on read when DRQ is set to one.

FUNCTIONAL DESCRIPTION - The data register is 16-bit wide.

BIT DESCRIPTION

15	14	13	12	11	10	9	8
Data (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Data (7:0)							

PCMICA CONFIGURATION OPTION REGISTER

DIRECTION - This register is read-only by host.

FUNCTION DESCRIPTION - Direct map to 0x200H in the Attribute Memory.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
SRESET	LevlReq	Configuration Index					

BIT 0~5 Configuration Index:
0 : common memory mode
1 : Independent IO mode
2 : Primary IO mode
3 : Secondary IO mode

BIT 6 LevlReq (level Mode IREQ#) : Level Mode Interrupts are selected when this bit is set to one, otherwise it is Pulse Mode Interrupts.

BIT 7 SRESET (Soft Reset): Setting this bit to one places the card in the reset state. This is equivalent to assertion of the RESET signal.

PCMICA CARD CONFIGURATION AND STATUS REGISTER

DIRECTION - This register is bi-directional for the drive and host.

FUNCTION DESCRIPTION - Direct map to 0x202H in the Attribute Memory.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
SCDect	SigChg	IOis8	ResrV	SPKR/DASP	PwrDn	Intr	ResrV

BIT 0 Reserved

BIT 1 Intr (Interrupt Request Pending) : The real time status of the host interrupt signal pin.

BIT 2 PwrDn (Power Down): This bit will enable the power down mode.

BIT 3 SPKR/DASP: Setting this bit to 1 will enable DASP- to the BVD2 pin of the PCMCIA connector, otherwise, the BVD2 will be held at high-impedance.

BIT 4 ResrV: Reserved bit must be 0.

BIT 5 IOis8 (I/O Cycles Occur Only as 8-bit Transfer): When the host can provide I/O cycle only using the D7:D0 data path, the PCMCIA software will set this bit to 1.

BIT 6 SigChg (Signal Change Enable/Disable): If this bit is set to one, the Signal Changed output is enabled.
BIT 7 SCDect (Status Change Detected): This bit indicates that at least one bit of the Pin replacement Register is set one.

PCMICA PIN REPLACEMENT REGISTER

DIRECTION - This register is read-only by host.

FUNCTION DESCRIPTION - Direct map to 0x204H in the Attribute Memory.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
ResrV	ResrV	CRdy	CWProt	ResrV	ResrV	CSRdy	CSWProt

BIT 0 CSWProt (Current State of Write Protect) : This bit represents the current the state of the Write Protect.
BIT 1 CSRdy (Current State of Ready) : This bit represents the internal state of the READY signal.
BIT 2~3 Reserved.
BIT 4 CWProt (Change Write Protect) : This bit is set to one when CSWProt changes state.
BIT 5 CRdy (Changed Ready) : This bit is set to one when CSRdy changes state.
BIT 6~7 ResrV : Reserved bit must be 0.

PCMICA SOCKET AND COPY REGISTER

DIRECTION - This register is bi-directional for the drive and host.

FUNCTION DESCRIPTION - Direct map to 0x206H in the Attribute Memory.

BIT DESCRIPTION

7	6	5	4	3	2	1	0
ResrV		Copy Number			Socket Number		

BIT 0~2 Socket Number : The first Socket is numbered 0.
BIT 3~5 Copy Number
BIT 6~7 ResrV : Reserved bit must be 0.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply voltage	– 0.3 to + 7.0	V
V_{IN}	Input voltage	– 0.3 to V DD + 0.3	V
I_{IN}	DC input current	– 10	mA
T_{STG}	Storage temperature	– 40 to + 80	°C

Recommended Operating Conditions

Symbol	Parameter		Ratings	Unit
V_{DD}	DC supply voltage	5V	4.5 to + 5.5	V
		3.3V	3.0 to 3.6	V
Ta	Storage temperature		0 to + 60	°C

D.C. Electrical Characteristics @ 3.3V
(T_A = 0 to +60°C, V_{CC} = 3.3V ± 5%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	CMOS		2.0			V
V_{IL}	Low level input voltage	CMOS				1.0	V
V_T	Switching threshold	CMOS			1.4		V
V_{T+}	Switching trigger, positive-going threshold	CMOS				2.0	V
V_{T-}	Switching trigger, negative-going threshold	CMOS		1.0			V
I_{IH}	High level input current	Input buffer	$V_{IN} = V_{DD}$	–10		10	uA
		Input buffer with pull-up		10	30	60	
I_{IL}	Low level input current	Input buffer	$V_{IN} = V_{SS}$	–10		10	uA
		Input buffer with pull-up		–160	–30	–10	
V_{OH}	High level output voltage		I_{OH} = –8 mA	2.4			V
V_{OL}	Low level output voltage		I_{OL} = 8 mA			0.4	V
I_{OZ}	Tri-state output leakage current		$V_{OUT} = V_{SS}$ or V_{DD}	–10		10	uA
I_{DD}	Maximum operating current		V_{DD} = 5.0V, f_{MCLK} = 20 MHz		30	40	mA
Iidle	Idle current					10	mA
Ids	Stop current					300	uA

ELECTRICAL CHARACTERISTICS @ 5V
(T_A = 0 TO 60°C, V_{CC} = 5V ± 10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	CMOS		3.5			V
		TTL		2.0			
V_{IL}	Low level input voltage	CMOS				1.5	V
		TTL				0.8	
V_T	Switching threshold	CMOS			2.5		V
		TTL			1.4		
V_{T+}	Switching trigger, positive-going threshold	CMOS				4.0	V
		TTL				2.0	
V_{T-}	Switching trigger, negative-going threshold	CMOS			1.0		V
		TTL			0.8		
I_{IH}	High level input current	Input buffer	$V_{IN} = V_{DD}$	–10		10	uA
		Input buffer with pull-up		10	50	100	
I_{IL}	Low level input current	Input buffer	$V_{IN} = V_{SS}$	–10		10	uA
		Input buffer with pull-up		–100	–50	–10	
V_{OH}	High level output voltage		I_{OH} = –8 mA	2.4			V
V_{OL}	Low level output voltage		I_{OL} = 8 mA			0.4	V
I_{OZ}	Tri-state output leakage current		$V_{OUT} = V_{SS}$ or V_{DD}	–10		10	uA
I_{DD}	Maximum operating current		V_{DD} = 5.0V, f_{MCLK} = 24 MHz		30	40	mA
Iidle	Idle current					10	mA
Ids	Stop current					400	uA

ENVIRONMENTAL AND RELIABILITY SPECIFICATIONS

ITEM	SPECIFICATION	
Vibration	Operating Non-Operating	15G peak to peak Max. 15G peak to peak Max.
Shock	Operating Non-Operating	2,000G Max. 2,000G Max.
Relative Humidity (non-condensing)	Operating Non-Operating	8% ~ 95% 8% ~ 95%
MTBF	Operating	> 1,000,000 hours
Endurance	Operating	≥ 100,000 erase program cycles
Data Reliability	Operating	< 1 non-recoverable error in 10^{14} bits read

INTERFACE SIGNAL TIMING

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, a direct mapped I/O transfer and a memory access. The two timing sequences are explained in detail in the PCMCIA PC Card Standard. The PC Card conforms to the timing in that reference document.

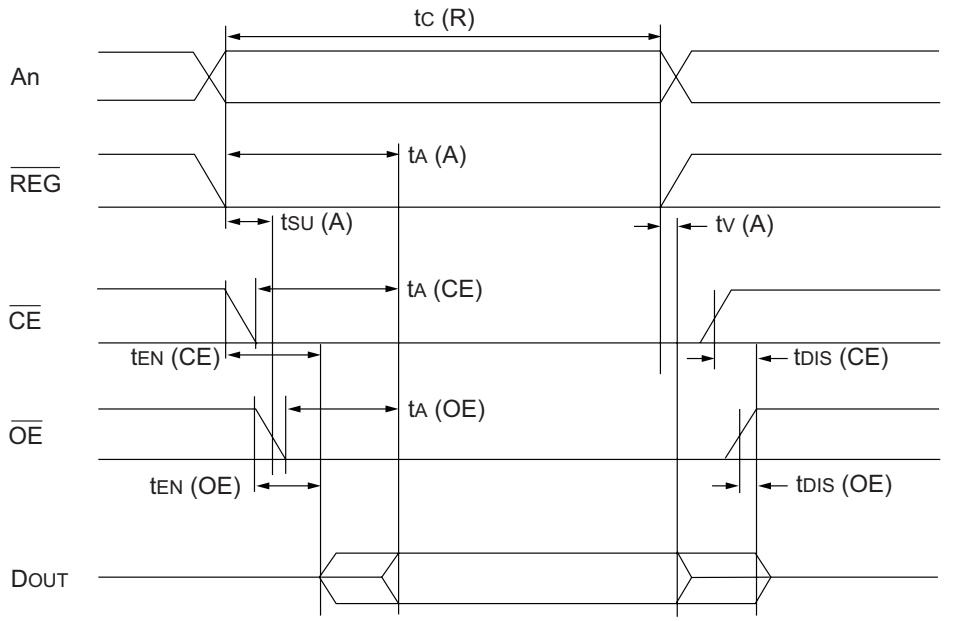
PC CARD INTERFACE

ATTRIBUTE MEMORY READ TIMING

Parameter	Symbol	IEEE Symbol	300ns	
			Min. ns	Max. ns
Read Cycle Time	$t_{C}(R)$	T_{AVAV}	300	
Address Access Time	$t_{A}(A)$	T_{AVQV}		300
Card Enable Access Time	$t_{A}(CE)$	T_{ELQV}		300
Output Enable Access Time	$t_{A}(OE)$	T_{GLQV}		150
Output Disable Time from CE	$t_{DIS}(CE)$	T_{EHQZ}		100
Output Disable Time from OE	$t_{DIS}(OE)$	T_{GHQZ}		100
Address Setup Time	$t_{SU}(A)$	t_{AVWL}	30	
Output Enable Time from CE	$t_{EN}(CE)$	t_{ELQNZ}	5	
Output Enable Time from OE	$t_{EN}(OE)$	t_{GLQNZ}	5	
Data Valid from Address Change	$t_{V}(A)$	t_{AXQX}	0	

NOTE: *All times are in nanosecond. Dout signifies data provided by the PC Card to the system. The $\overline{CE}$ signal or both the $\overline{OE}$ signal & the $\overline{WE}$ signal must be de-asserted between consecutive cycle operations.*

ATTRIBUTE MEMORY READ TIMING DIAGRAM



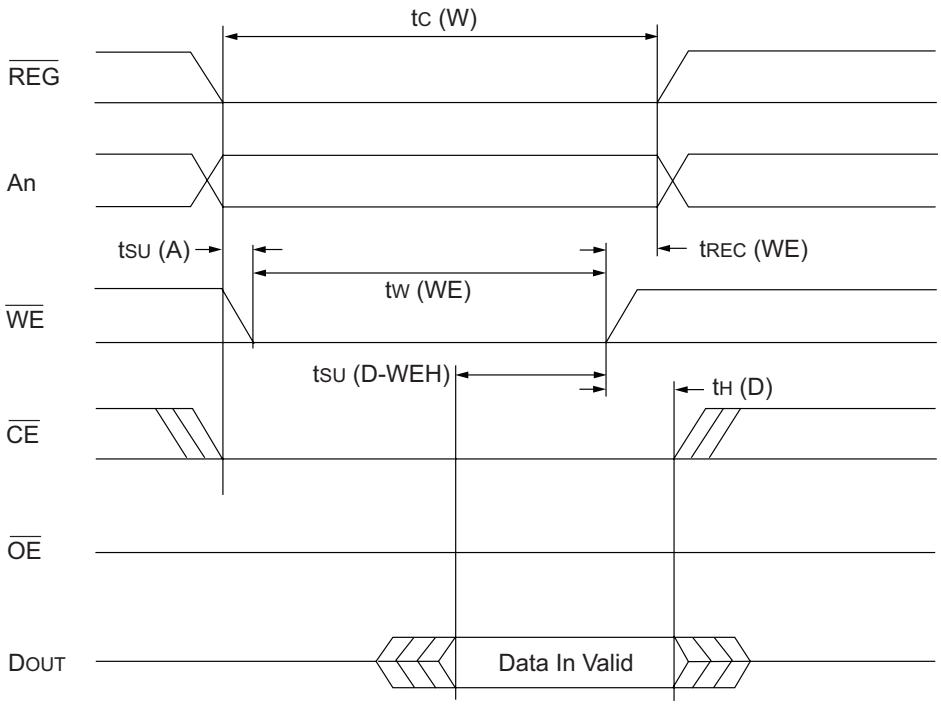
ATTRIBUTE MEMORY WRITE TIMING

Note: A host cannot write to CIS. This timing is specified only for the write to Configuration Register.

Parameter	Symbol	IEEE Symbol	250ns	
			Min. ns	Max. ns
Write Cycle Time	$t_{C}(W)$	t_{AVAV}	250	
Write Pulse Width	$t_{W}(WE)$	t_{WLWH}	150	
Address Setup Time	$t_{SU}(A)$	t_{AVWL}	30	
Write Recovery Time	$t_{REC}(WE)$	t_{WMAX}	30	
Data Setup Time for WE	t_{SU}(D-WEH)	t_{DVWH}	80	
Data Hold Time	$t_{H}(D)$	t_{WMDX}	30	

NOTE: All times are in nanosecond. Din signifies data provided by the system to the PC Card.

ATTRIBUTE MEMORY WRITE TIMING DIAGRAM

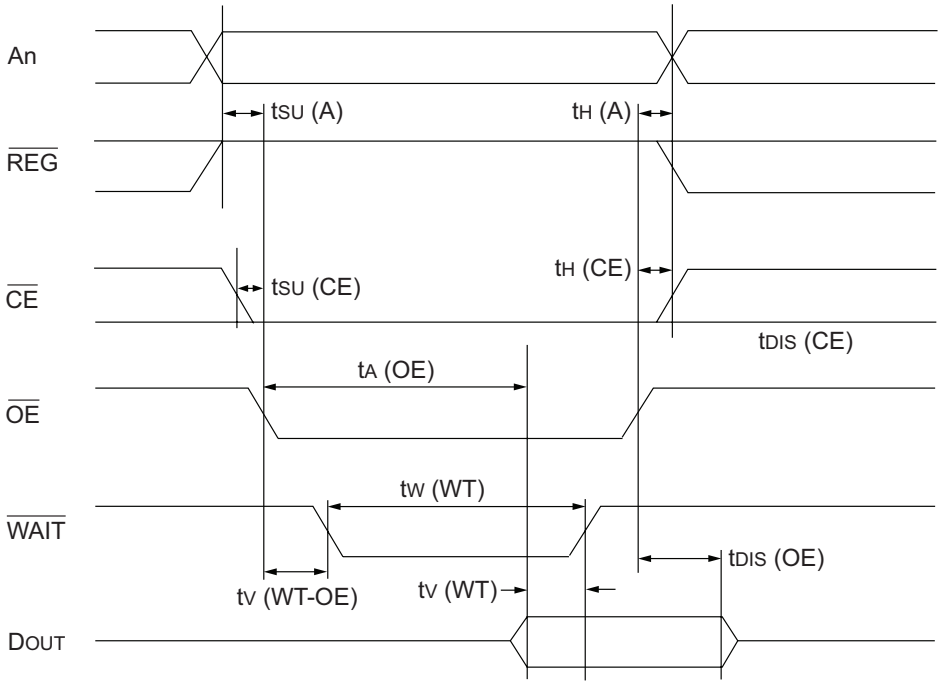


COMMON MEMORY READ TIMING

Parameter	Symbol	IEEE Symbol	Min. ns	Max. ns
Output Enable Access Time	ta (OE)	tGLQV		125
Output Disable Time from OE	tdis (OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Address Hold Time	th (A)	tGHAX	20	
CE Setup before OE	tsu (CE)	tELGL	0	
CE Hold following OE	th (CE)	tGHEH	20	
Wait Delay Falling from OE	tv (WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv (WT)	tQVWTH		0
Wait Width Time	tw (WT)	tWTLWTH		350

NOTE: *The maximum load on $\overline{WAIT}$ is 1 LSTTL with 50pF total load. All times are in nanoseconds. DOUT signifies data provided by the PC Card to the system. The $\overline{WAIT}$ signal may be ignored if the $\overline{OE}$ cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.*

COMMON MEMORY READ TIMING DIAGRAM

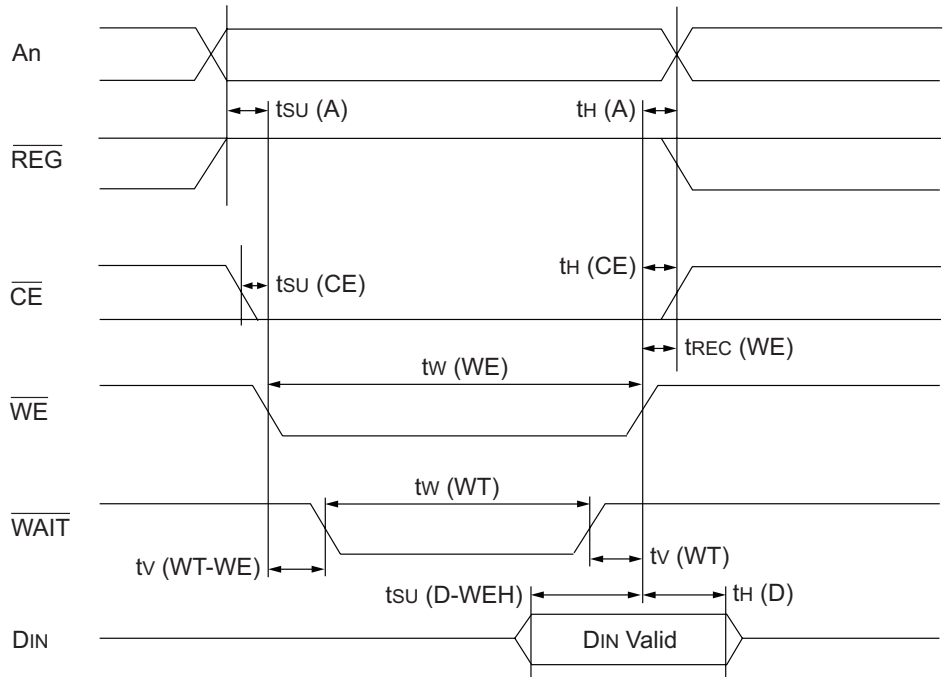


COMMON MEMORY WRITE TIMING

Parameter	Symbol	IEEE Symbol	Min. ns	Max. ns
Data Setup before WE	tsu (D-WEH)	tDVWH	80	
Data Hold following WE	th (D)	tIWMDX	30	
WE Pulse Width	tw (WE)	tWLWH	150	
Address Setup Time	tsu (A)	tAVWL	30	
CE Setup before WE	tsu (CE)	tELWL	0	
Write recovery Time	trec (WE)	tWMAX	30	
Address Hold Time	th (A)	tGHAX	20	
CE Hold following WE	th (CE)	tGHEH	20	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35
WE High from Wait Release	tv (WT)	tWTHWH	0	
Wait Width Time	tw (WT)	tWTLWTH		350

NOTE: *The maximum load on $\overline{WAIT}$ is 1 LSTTL with 50pF total load. All times are in nanoseconds. DIN signifies data provided by the system to the PC Card. The $\overline{WAIT}$ signal may be ignored if the $\overline{WE}$ cycle-to-cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.*

COMMON MEMORY WRITE TIMING DIAGRAM

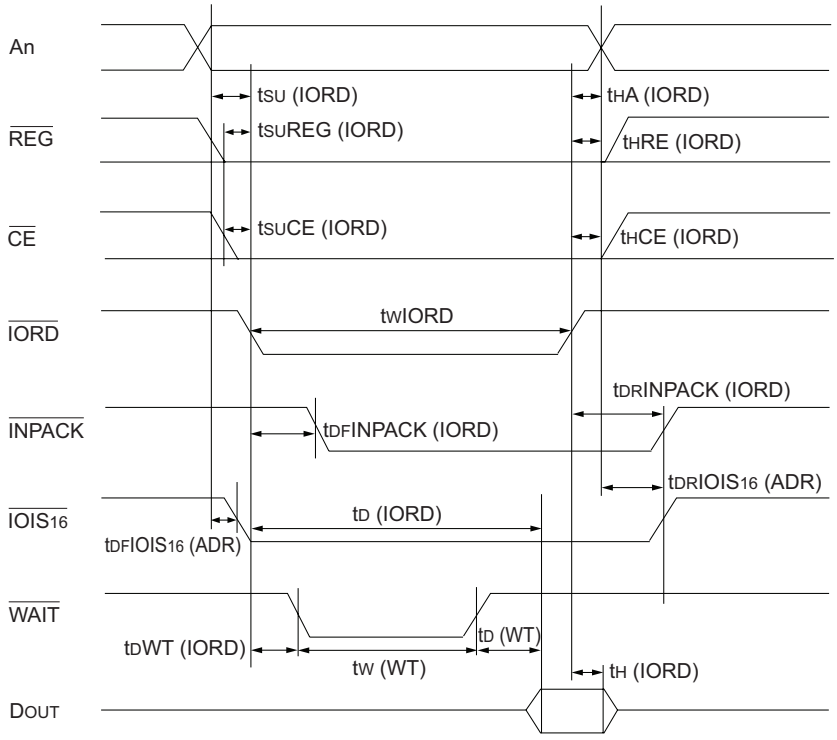


I/O INPUT (READ) TIMING

Parameter	Symbol	IEEE Symbol	Min. ns	Max. ns
Data Delay after IORD	td (IORD)	tIGLQV		100
Data Hold following IORD	th (IORD)	tIGHQX	0	
IORD Width Time	tw (IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA (IORD)	tAVIGL	70	
Address Hold following IORD	thA (IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE (IORD)	tELIGL	5	
CE Hold following IORD	thCE (IORD)	tIGHEH	20	
REG Setup before IORD (IORD)	tsuREG	tRGLIGL	5	
REG Hold following IORD	thREG (IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK (IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK (IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16 (ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16 (ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT (IORD)	tIGLWTL		35
Data Delay from Wait Rising	td (WT)	tWTHQV		0
Wait Width Time	tw (WT)	tWTLWTH		350

NOTE: *The maximum load on $\overline{WAIT}$, $\overline{INPACK}$ and $\overline{IOIS16}$ is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from $\overline{WAIT}$ high to $\overline{IORD}$ high is 0nsec, but minimum $\overline{IORD}$ width must still be met. DOUT signifies data provided by the PC Card to the system. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.*

I/O READ TIMING DIAGRAM

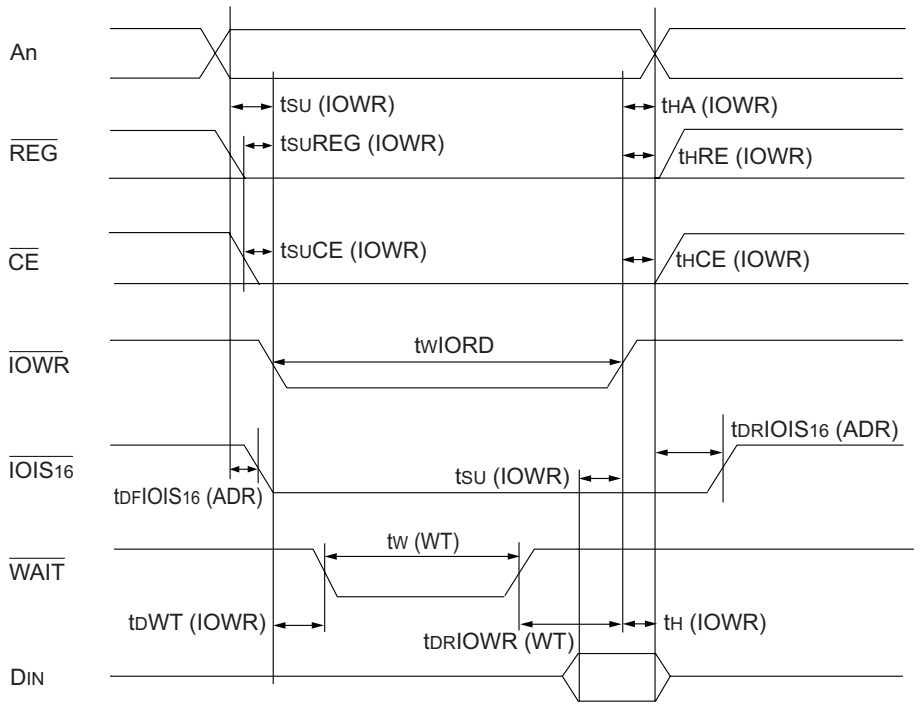


I/O INPUT (WRITE) TIMING

Parameter	Symbol	IEEE Symbol	Min. ns	Max. ns
Data Setup before IOWR	tsu (IOWR)	tDVIWH	60	
Data Hold following IOWR	th (IOWR)	tIWHDX	30	
IOWR Width Time	tw (IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA (IOWR)	tAVIWL	70	
Address Hold following IOWR	thA (IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE (IOWR)	tELIWL	5	
CE Hold following IOWR	thCE (IOWR)	tIWHEH	20	
REG Setup before IOWR	tsuREG (IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG (IOWR)	tIWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16 (ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16 (ADR)	tAVISH		35
Wait Delay Falling from IOWR	tdWT (IOWR)	tIWLWTL		35
IOWR high from Wait high	tdrIOWR (WT)	tWTJIWH	0	
Wait Width Time	tw (WT)	tWTLWTH		350

NOTE: *The maximum load on $\overline{WAIT}$, $\overline{INPACK}$, and $\overline{IOIS16}$ is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from $\overline{WAIT}$ high to $\overline{IOWR}$ high is 0nsec, but minimum $\overline{IOWR}$ width must still be met. DIN signifies data provided by the system to the PC Card. The Wait Width time meets the PCMCIA specification of 12s but is intentionally less in this specification.*

I/O WRITE TIMING DIAGRAM



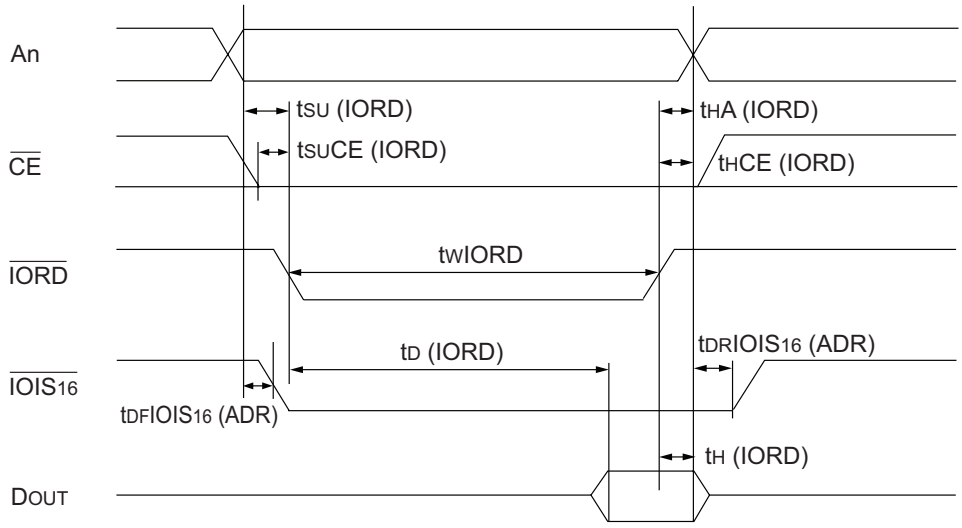
IDE MODE INTERFACE

IDE Mode Read Timing

Parameter	Symbol	IEEE Symbol	Min. ns	Max. ns
Data Delay after IORD	td (IORD)	tIGLQV		100
Data Hold following IORD	th (IORD)	tIGHQX	0	
IORD Width Time	tw (IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA (IORD)	tAVIGL	70	
Address Hold following IORD	thA (IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE (IORD)	tELIGL	5	
CE Hold following IORD	thCE (IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16 (ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16 (ADR)	tAVISH		35

NOTE: *The maximum load on $\overline{IOIS16}$ is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from WAIT high to $\overline{IORD}$ high is 0nsec, but minimum $\overline{IORD}$ width must still be met. DOUT signifies data provided by the PC Card to the system.*

IDE MODE READ TIMING DIAGRAM

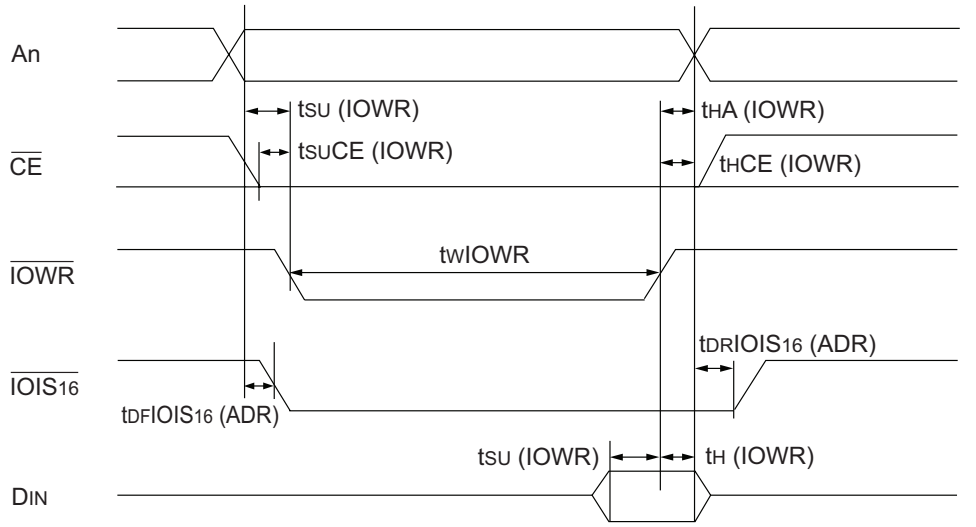


IDE Mode Write Timing

Parameter	Symbol	IEEE Symbol	Min. ns	Max. ns
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	twI(OWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

NOTE: *The maximum load on $\overline{IOIS16}$ is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from - WAIT high to $\overline{IOWR}$ high is 0nsec, but minimum $\overline{IOWR}$ width must still be met. DIN signifies data provided by the system to the PC Card.*

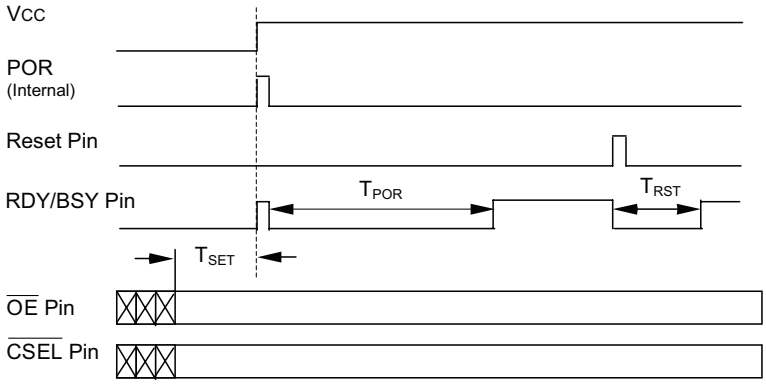
IDE MODE WRITE TIMING DIAGRAM



RESET TIMING

Parameter	Symbol	Min	Typ	Max	Unit
Level Set before Power On	tset	1			ms
Power on Reset	tpor			10	ms
Reset time	trst			10	ms

RESET TIMING DIAGRAM

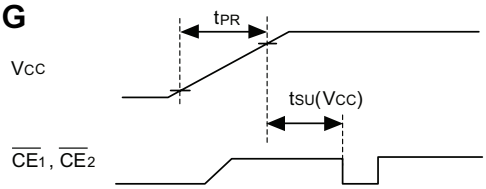


POWER ON RESET CHARACTERISTICS

All card status are reset automatically when Vcc voltage goes over about 2.3 V.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
$\overline{CE}$ setup time	tsu(Vcc)	100	—	—	ms	
Vcc rising up time	tpr	0.1	—	100	ms	

POWER ON RESET TIMING



Attention for Card Use

In the reset or power off, all register information is cleared.

All card status are cleared automatically when Vcc voltage turns below about 2.5V.

Notice that the card insertion/removal should not be executed during host is active, if the card is used in true IDE mode.

After the card hard reset, soft reset, or power on reset, the card cannot access during +READY pin is "low" level.

Please notice that the card insertion/removal should be executed after card internal operations are completed (status register bit 7 turns from "1" to "0").

Before the card insertion Vcc cannot be supplied to the card. After confirmation that $\overline{CD}_1$, $\overline{CD}_2$ pins are inserted, supply Vcc to the card.

$\overline{OE}$ must be kept at the Vcc level during power on reset in memory card mode and I/O card mode. $\overline{OE}$ must be kept constantly at the GND level in True IDE mode.

Unused pins of data bus (D_0 to D_{15}) signals should not be opened.

CARD INFORMATION STRUCTURE (CIS) & IDENTIFY DRIVE (ID) INFORMATION

IDENTIFY DRIVE INFORMATION

Word	8MB	16MB	32MB	48MB	64MB	96MB	128MB	256MB
0	848A	848A	848A	848A	848A	848A	848A	848A
1	007A	00F6	01EC	02E2	00F6	0171	01EC	03D8
2	0000	0000	0000	0000	0000	0000	0000	0000
3	0004	0004	0004	0004	0010	0010	0010	0010
4	0000	0000	0000	0000	0000	0000	0000	0000
5	0200	0200	0200	0200	0200	0200	0200	0200
6	0020	0020	0020	0020	0020	0020	0020	0020
7-8	0000	0000	0000	0001	0001	0002	0003	0007
	3D00	7B00	F600	7100	EC00	E200	D800	B000
9	0000	0000	0000	0000	0000	0000	0000	0000
10-19	All 2020	All 2020	All 2020	All 2020	All 2020	All 2020	All 2020	All 2020
20	0000	0000	0000	0000	0000	0000	0000	0000
21	0002	0002	0002	0002	0002	0002	0002	0002
22	0004	0004	0004	0004	0004	0004	0004	0004
23-26	*1	*1	*1	*1	*1	*1	1	*1
27-46	*2	*2	*2	2	*2	*2	*2	*2
47	0004	0004	0004	0004	0004	0004	0004	0004
48	0000	0000	0000	0000	0000	0000	0000	0000
49	0200	0200	0200	0200	0200	0200	0200	0200
50	0000	0000	0000	0000	0000	0000	0000	0000
51	0200	0200	0200	0200	0200	0200	0200	0200
52	0000	0000	0000	0000	0000	0000	0000	0000
53	0001	0001	0001	0001	0001	0001	0001	0001
54	007A	00F6	01EC	02E2	00F6	0171	01EC	03D8
55	0004	0004	0004	0004	0010	0010	0010	0010
56	0020	0020	0020	0020	0020	0020	0020	0020
57-58	3D00	7B00	F600	7100	EC00	E200	D800	B000
	0000	0000	0000	0001	0001	0002	0003	0007
59	0100	0100	0100	0100	0100	0100	0100	0100
60-61	3D00	7B00	F600	7100	EC00	E200	D800	B000
	0000	0000	0000	0001	0001	0002	0003	0007
62-127	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000
128	0000	0000	0000	0000	0000	0000	0000	0000
129-159	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000
160	0000	0000	0000	0000	0000	0000	0000	0000
161-255	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000	All 0000

Note 1. Firmware Version: Rev 1.15 (52 65 76 20 31 2E 31 35)

2. Model Number: SAMSUNG CF/ATA (53 41 4d 53 55 4e 47 20 43 46 2f 41 54 41 20 20 20 20 20 20)

CARD INFORMATION STRUCTURE

AttributeOffset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
000h	01	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	04									Link is 4bytes	Link to next tuple
004h	DF	Device Type Code Dh=I/O				W 1	Speed 7h			I/O device, No Write Protects, Device Speed = 400ns	Device ID WPS, Speed
006h	4A	X	9h				2h				
008h	01	Device Size								2Kbyte of address Space	Device Size
00Ah	FF	List End Marker								End of Devices	End Marker
00Ch	1 C	CISTPL_DEVICE_OC								Other Condition Device Info Tuple	Tuple Code
00Eh	04									Link is 4bytes	Link to next tuple
010h	02	0	Reserved, 0				VccU		M	3.3V Vcc Operation	OC Info
012h	D9	Device Type Code Dh=I/O				W 1	Speed 1h			I/O device, No Write Protects, Device Speed=250ns	Device ID WPS, Speed
014h	01	Device Size								2Kbyte of address Space	Device Size
016h	FF	List End Marker								End of Devices	End Marker
018h	18	CISTPL_JEDEC_C								JEDEC ID Common Mem	Tuple Code
01Ah	02									Link is 2bytes	Link to next tuple
01Ch	DF	PCMCIA Manufacture 's ID								First Byte of JEDEC ID	JEDEC ID of Device 1
01Eh	01	PCMCIA Code for PC Card-ATA No Vpp Required								Second Byte of JEDEC ID	JEDEC ID
020h	20	CISTPL_MANFID								Manufacture ID String	Tuple Code
022h	04									Link is 4bytes	Link to next tuple
024h	CE	PC Card Manufacture's ID Code									TPLMID_MANF
026h	00										TPLMID_MANF
028h	00	Manufacture Information									TPLMID_CARD
02Ah	00										TPLMID_CARD
02Ch	15	CISTPL_VERS_1								Level 1 Version/Product Infor mation	Tuple Code
02Eh	20									Link is 20bytes	Link to next tuple
030h	04	Major Version Number								PCMCIA 2.1	TPLLV1_MAJOR
032h	01	Minor Version Number								JEIDA 4.2	TPLLV1_MINOR
034h	53	Manufacture Information								S	String 1
036h	41									A	
038h	4D									M	
03Ah	53									S	
03Ch	55									U	
03Eh	4E									N	
040h	47									G Name of Manufacture	
042h	20										
044h	20										
046h	20										
048h	20										
04Ah	20										
04Ch	20										
04Eh	00	End of Manufacture Information								Null Terminator	End String 1
050h	52	Product Information								R	String 2
052h	65									e	
054h	76									v	
056h	20										
058h	31									1	
05Ah	2E									.	
05Ch	31									1 Firmware Revision	
05Eh	35									5	
060h	20										
062h	20										
064h	20										
066h	20										
068h	20										

CARD INFORMATION STRUCTURE CONT.

AttributeOffset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
06Ah	00	End of Product Information								Null Terminator	End String 2
06Ch	00	End of CIS Revision Number								Null Terminator	
06Eh	FF	List End Marker									End Marker
070h	21	CISTPL_FUNCID								Function ID Tuple	Tuple Code
072h	02									Link is 2bytes	Link to next tuple
074h	04	IC Card Function Code								Fixed Disk Function	TPLFID_FUNCTION
076h	01	RFU, 0						R	P	System Initialization Bit Mask, Power-On-Self Test	TPLFID_SYSINIT
078h	22	CISTPL_FUNCE								Function Extention Tuple	Tuple Code
07Ah	02									Link is 2bytes	Link to next tuple
07Ch	01	Disk Function Extension Tuple Type								Disk Device Interface	TPLFE_TYPE
07Eh	01	Interface Type Code								PCCard-ATA Interface	TPLFE_DATA
080h	22	CISTPL_FUNCE								Function Extention Tuple	Tuple Code
082h	03									Link is 3bytes	Link to next tuple
084h	02	Disk Function Extension Tuple Type								Disk Device Interface	TPLFE_TYPE
086h	0C	RFU				U	S		V	Silicon/Rotating, ID/SN is unique	TPLFE_DATA
088h	0F	R	I	E	N	P3	P2	P1	P0	Auto, Idle, Standby, Sleep Mode supported	TPLFE_DATA
08Ah	1A	CISTPL_CONFIG								Configuration Tuple	Tuple Code
08Ch	05									Link is 5bytes	Link to next tuple
08Eh	01	RFSZ			RMSZ				RASZ	Size of Fields Byte	TPCC_SZ
090h	03	TPCC_LAST								Entry Index 03h	Last entry of Configuration table
092h	00	TPCC_RADR								Configuration Registers are located at 200h	Location of Config Registers
094h	02	TPCC_RADR									
096h	0F	RFU				S	P	C	I	4 Configuration Registers are present	TPCC_RMSK
098h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
09Ah	08									Link is 8bytes	Link to next tuple
09Ch	C0	I	D	Configuration Entry Number						Memory Mapped I/O, D: Default Configuration, I: Interface Byte Follows	TPCE_INDX
09Eh	C0	MW	R	WP	BV	Interface Type				Memory Only Interface, Bvd & WP not used, RDY/BSY & Wait used for Memory Cycle	TPCE_IF
0A0h	A1	M	MS		IRQ	IO	T Power			Vcc power-description structure only, MS: Single 2-byte length specified M: Misc field structure is present	TPCE_FS
0A2h	01	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating Supply Voltage, No Extension	Power Parameters for Vcc
0A4h	55	X	Ah				5h			Vcc Nominal is 5V	Vcc Nominal Value
0A6h	08	Length in 256 bytes pages(LSB)								Length of Mem Space is 2KB	TPCE_MS Length LSB
0A8h	00	Length in 256 bytes pages(MSB)								Start at 0 on Card	TPCE_MS Length MSB
0AAh	20	X	R	P	R	A	Twin			Power Down	TPCE_MI
0ACh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
0AEh	06									Link is 6bytes	Link to next tuple
0B0h	00	I	D	Configuration Entry Number							TPCE_INDX
0B2h	01	M	MS		IRQ	IO	T	Power		Vcc power-description structure only	TPCE_FS
0B4h	21	R	DI	PI	AI	SI	HV	LV	NV	Maximum Current required averaged over 10ms, Nominal Operating Supply Voltage, With Extension	TPCE_PD
0B6h	B5	X	6h				5h			1V x3	Vcc Nominal Value
0B8h	1E	X	1Eh(30d)							Vcc Nominal is 3.3V	

CARD INFORMATION STRUCTURE CONT.

AttributeOffset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0BAh	4D	X	9h				5h			Peak I is 45mA	Peak I Value
0BCh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
0Beh	0A									Link is 10bytes	Link to next tuple
0C0h	C1	I	D Configuration Entry Number							I/O Mapped Contiguous 16 Registers Configuration, D: Default Configuration, I: Interface Byte Follows	TPCE_INDX
0C2h	41	W	R	P	B	Interface Type				I/O Interface, Bvd & WP not used, RDY/BSY active, Wait not used for memory access	TPCE_IF
0C4h	99	M	MS		IRQ	IO	T	Power		Misc & IRQ field are present, Vcc power-description structure only	TPCE_FS
0C6h	01	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage	TPCE_PD
0C8h	55	X	Ah				5h			Vcc Nominal is 5V	Vcc Nominal Value
0CAh	64	R	Bus 16/8		I/O AddrLines					Support 16/8 bit I/O access, I/O Address Lines are 16	TPCE_IO
0CCh	F0	S	P	L	M	V	B	I	N	IRQ Sharing S: Share Logic active P: Pulse IRQ supported L: Level IRQ supported M: Bit Mask of IRQ	TPCE_IR
0CEh	FF									IRQ Levels to be routed 0-7 recommended	TPCE_IR Mask Extension
0D0h	FF									IRQ Levels to be routed 8-15 recommended	TPCE_IR Mask Extension
0D2h	20	X	R	P	RO	A	T			Power Down supported	TPCE_MI
0D4h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
0D6h	06									Link is 6 bytes	Link to next tuple
0D8h	01	I	D Configuration Entry Number								TPCE_INDX
0DAh	01	M	MS		IRQ	IO	T	Power		Vcc power-description structure only	TPCE_FS
0DCh	21	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage, Maximum Current required averaged over 10ms	TPCE_PD
0DEh	B5	X	6h				5h			1Vx3	Vcc Nominal Value
0E0h	1E	X	1Eh(30d)							Vcc Nominal is 3.3V	
0E2h	4D	X	9h				5h			Peak I is 45mA	Peak I Value
0E4h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
0E6h	0F									Link is 15bytes	Link to next tuple
0E8h	C2	I	D	Configuration Entry Number							TPCE_INDX
0EAh	41	W	R	P	B	Interface Type				I/O Interface, Bvd & WP not used, RDY/BSY active, Wait not used for memory access	TPCE_IF
0ECh	99	M	MS		IRQ	IO	T	Power		Misc & IRQ field are present, Vcc power-description structure only	TPCE_FS
0EEh	01	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage	TPCE_PD
0F0h	55	X	Ah				5h			Vcc Nominal is 5V	Vcc Nominal Value

CARD INFORMATION STRUCTURE CONT.

AttributeOffset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0F2h	EA	R	Bus 16/8		I/O AddrLines					I/O range description, Support 16/8 bit I/O access, A 1 Kbyte I/O address space	TPCE_IO
0F4h	61	Size of length		Size of address		Number of I/O Address Ranges				Length is 1 byte long, Address is 2 byte long, 1 I/O Address Range Description field	I/O Range Description Byte
0F6h	F0	Start of I/O Address Block First(LSB)									
0F8h	01	Start of I/O Address Block First(MSB)									
0FAh	07	First I/O Range Length									
0FCh	F6	Start of I/O Address Block Second(LSB)									
0FEh	03	Start of I/O Address Block Second(MSB)									
100h	01	Second I/O Range Length									
102h	EE	S	P	L	M	V	B	I	N	IRQ Sharing S: Share Logic active, P: Pulse IRQ supported, L: Level IRQ supported, V: Vendor-Specific supported, B: Bus-Error supported, I: I/O-check supported	TPCE_IR
104h	20	X	R	P	RO	A	T			Power Down supported	TPCE_MI
106h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
108h	06									Link is 6bytes	Link to next tuple
10Ah	02	I	D	Configuration Entry Number							TPCE_INDX
10Ch	01	M	MS		IRQ	IO	T	Power		Vcc power-description structure	TPCE_FS only
10Eh	21	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage, Maximum Current required averaged over 10ms	TPCE_PD
110h	B5	X	6h				5h			1Vx3	Vcc Nominal Value
112h	1E	X	1Eh(30d)							Vcc Nominal is 3.3V	
114h	4D	X	9h				5h			Peak I is 45mA	Peak I Value
116h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
118h	0F									Link is 15bytes	Link to next tuple
11Ah	C3	I	D	Configuration Entry Number							TPCE_INDX
11Ch	41	W	R	P	B	Interface Type				I/O Interface, Bvd & WP not used, RDY/BSY active, Wait not used for memory access	TPCE_IF
11Eh	99	M	MS		IRQ	IO	T	Power		Misc & IRQ field are present, Vcc power-description structure only	TPCE_FS
120h	01	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage	TPCE_PD
122h	55	X	Ah				5h			Vcc Nominal is 5V	Vcc Nominal Value
124h	EA	R	Bus 16/8		I/O AddrLines					I/O range description, Support 16/8 bit I/O access, A 1 Kbyte I/O address space	TPCE_IO

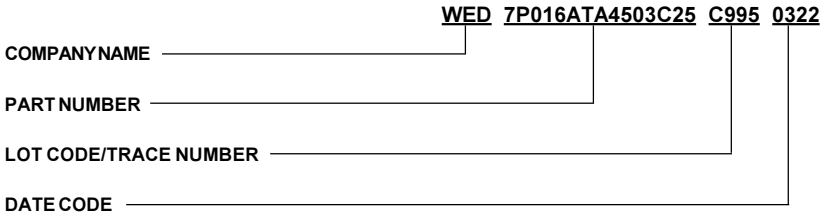
CARD INFORMATION STRUCTURE CONT.

AttributeOffset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
126h	61	Size of length		Size of address		Number of I/O Address Ranges				Length is 1 byte long, Address is 2 byte long, 1 I/O Address Range Description field	I/O Range Description Byte
128h	70	Start of I/O Address Block First (LSB)									
12Ah	01	Start of I/O Address Block First (MSB)									
12Ch	07	First I/O Range Length									
12Eh	76	Start of I/O Address Block Second(LSB)									
130h	03	Start of I/O Address Block Second(MSB)									
132h	01	Second I/O Range Length									
134h	EE	S	P	L	M	V	B	I	N	IRQ Sharing S: Share Logic active, P: Pulse IRQ supported, L: Level IRQ supported, V: Vendor-Specific supported, B: Bus-Error supported, I: I/O-check supported	TPCE_IR
136h	20	X	R	P	RO	A	T			Power Down supported	TPCE_MI
138h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
13Ah	06									Link is 6bytes	Link to next tuple
13Ch	03	I	D	Configuration Entry Number							TPCE_INDX
13Eh	01	M	MS		IRQ	IO	T	Power		Vcc power-description structure only	TPCE_FS
140h	21	R	DI	PI	AI	SI	HV	LV	NV	Nominal Operating supply Voltage, Maximum Current required averaged over 10ms	TPCE_PD
142h	B5	X	6h				5h			1Vx3	Vcc Nominal Value
144h	1E	X	1Eh(30d)							Vcc Nominal is 3.3V	
146h	4D	X	9h				5h			Peak I is 45mA	Peak I Value
148h	14	CISTPL_NO_LINK								No Link to Common Memory	Tuple Code
14Ah	00	No Bytes Following								Link Length is 0 byte	Link to next tuple
14Ch	FF	End of CIS Tuple Chain								End of CIS	Tuple Code

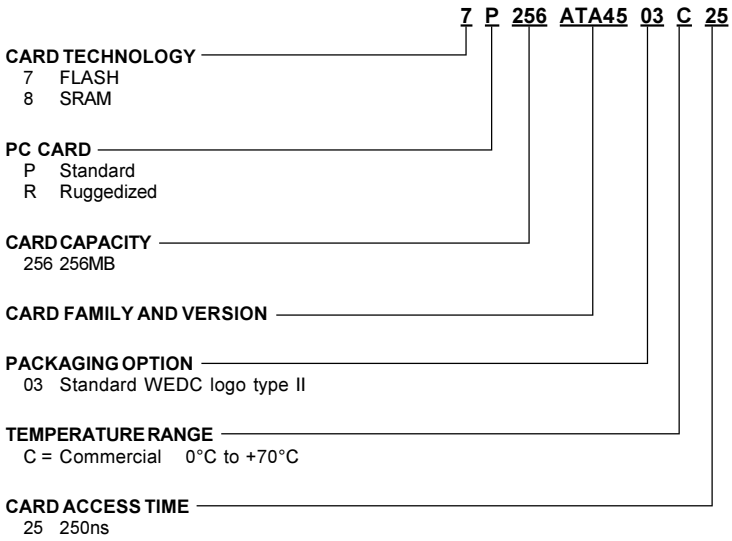
TRUE IDE TO PCMCIA INTERFACE

True IDE		PCMCIA ATA	
No(#)	**40pin**	**No(#)**	**68pin**
1	$\overline{\text{RESET}}$	58	RESET
2	GND	1,8,9,11,12,22,23,24,25,26,34,35,68, (56)	GND, A10-A3, $\overline{\text{OE}}$, $\overline{\text{CSEL}}$ (56)
3	D7	6	D7
4	D8	64	D8
5	D6	5	D6
6	D9	65	D9
7	D5	4	D5
8	D10	66	D10
9	D4	3	D4
10	D11	27	D11
11	D3	2	D3
12	D12	38	D12
13	D2	32	D2
14	D13	39	D13
15	D1	31	D1
16	D14	40	D14
17	D0	30	D0
18	D15	41	D15
19	GND	1,8,9,11,12,22,23,24,25,26,34,35,68, (56)	GND, A10-A3, $\overline{\text{OE}}$, $\overline{\text{CSEL}}$(56)
20	(keypin)		
21	$\overline{\text{DMACK}}$	60	$\overline{\text{INPACK}}$
22	GND	1,8,9,11,12,22,23,24,25,26,34,35,68, (56)	GND, A10-A3, $\overline{\text{OE}}$, $\overline{\text{CSEL}}$(56)
23	$\overline{\text{IOWR}}$	45	$\overline{\text{IOWR}}$
24	GND	1,8,9,11,12,22,23,24,25,26,34,35,68, (56)	GND, A10-A3, $\overline{\text{OE}}$, $\overline{\text{CSEL}}$(56)
25	$\overline{\text{IORD}}$	44	$\overline{\text{IORD}}$
26	GND	1,8,9,11,12,22,23,24,25,26,34,35,68, (56)	GND, A10-A3, $\overline{\text{OE}}$, $\overline{\text{CSEL}}$(56)
27	IORDY	59	$\overline{\text{WAIT}}$
28	CSEL	56	CSEL
29	$\overline{\text{DMACK}}$	61	$\overline{\text{REG}}$
30	GND	1,8,9,11,12,22,23,24,25,26,34,35,68, (56)	GND, A10-A3, $\overline{\text{OE}}$, $\overline{\text{CSEL}}$(56)
31	IREQ	16	RDY/$\overline{\text{BSY}}$
32	$\overline{\text{IOIS16}}$	33	WP
33	A1	28	A1
34	$\overline{\text{PDIAG}}$	63	BVD1
35	A0	29	A0
36	A2	27	A2
37	$\overline{\text{CS0}}$	7	$\overline{\text{CS0}}$
38	$\overline{\text{CS1}}$	42	$\overline{\text{CS1}}$
39	$\overline{\text{DASP}}$	62	BVD2
40	GND	1,8,9,11,12,22,23,24,25,26,34,35,68, (56)	GND, A10-A3, $\overline{\text{OE}}$, $\overline{\text{CSEL}}$(56)

PRODUCT MARKING



PART NUMBERING



ORDERING INFORMATION

7P XXX ATA45 SS T ZZ

XXX (unformatted capacity)

008	8MB
016	16MB
032	32MB
048	48MB
064	64MB
096	96MB
128	128MB
256	256MB
512	512MB

ATA45

Samsung based

SS

03	WEDC Flash ATA logo Type II
04	Blank Housing Type II
05	Blank Housing Type II Recessed

T

C	Commercial Temperature Range

ZZ

25	250ns

Document Title

Flash Cards ATA45 Series

Revision History

Rev level	Description	Date
Rev 0	Initial release	May 16, 2003