3.3V Slew Rate Limited, Half and Full Duplex

Preliminary Technical Data

ADM3483/ADM3485/ADM3488/ADM3490

FEATURES

- EIA RS-485/RS-422 Compliant
- Data Rate Options
  - ADM3483, ADM3488 – 250kbps
  - ADM3485, ADM3490 – 10Mbps
- Half and Full Duplex Options
- Reduced Slew Rates for Low EMI
- 2nA Supply Current in Shutdown Mode (ADM3483,ADM3485)
- Up to 32 Transceivers on a bus
- -7V to +12V Bus Common Mode Range
- Specified over –40°C to +85°C Temperature Range
- Available in 8-Lead SOIC
- ADM3483/85 available in an 8-Lead LFCSP Package

APPLICATIONS

- Low-Power RS-485 Applications
- EMI Sensitive Systems
- DTE-DCE Interfaces
- Industrial Control
- Packet Switching
- Local Area Networks
- Level Translators

GENERAL DESCRIPTION

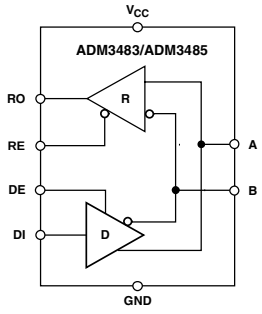
The ADM3483, ADM3485, ADM3488 and ADM3490 are 3.3V, low-power transceivers for RS-485 and RS-422 communication. Each part contains one driver and one receiver. The ADM3483 and ADM3488 feature slew-rate-limited drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The partially slew-rate-limited MAX3486 transmits up to 2.5Mbps. The ADM3485 and ADM3490 transmit at up to 10Mbps.

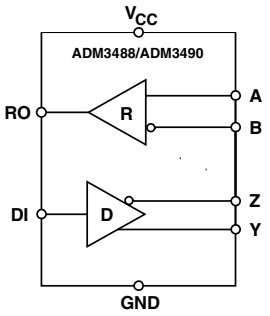
The drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if both inputs are open circuit. The ADM3488 and ADM3490 feature full duplex communication, while the ADM3483 and ADM3485 are designed for half-duplex communication.

The driver outputs are slew rate limited in order to reduce EMI and data errors caused by reflections from improperly terminated buses. Excessive power dissipation caused by bus contention or by output shorting is prevented with a thermal shutdown circuit.

The parts are fully specified over the commercial and industrial temperature ranges and all are available in 8-lead SOIC and the ADM3483 and the ADM3485 are also available in an 8-lead LFCSP packages.

FUNCTIONAL BLOCK DIAGRAMS





Part No.	Guaranteed Data Rate (Mpbs)	Supply Voltage (V)	Half/Full Duplex	Slew-Rate Limited	Driver/ Reciever Enable	Shutdown Current (nA)	Pin Count
ADM3483	0.25	3.0 to 3.6	Half	Yes	Yes	2	8
ADM3485	10		Half	No	Yes	2	8
ADM3488	0.25		Full	Yes	No	-	8
ADM3490	10		Full	No	No	-	8

Table 1. Selection Table

Rev. PrD

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ADM3483/ADM3485/ADM3488/ADM3490— SPECIFICATIONS

(V_{CC}=3.3V ±0.3%, T_A= T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}	2.0			V	R=100Ω (RS-422), Figure 3 Vcc = 3.3V ±5%
	1.5			V	R=54Ω (RS-485), Figure 3
	1.5			V	R=60Ω (RS-485), Vcc = 3.3V, Figure 4
Δ $\|V_{OD}\|$ for Complementary Output States			0.2	V	R=54Ω or 100Ω, Figure 3
Common Mode Output Voltage, V_{OC}			3	V	R=54Ω or 100Ω, Figure 3
Δ $\|V_{OC}\|$ for Complementary Output States			0.2	V	R=54Ω or 100Ω, Figure 3
DRIVER INPUT LOGIC					
CMOS Input Logic Threshold Low, V_{IH}	0.8			V	DE,DI,$\overline{RE}$
CMOS Input Logic Threshold High, V_{IL}			2.0	V	DE,DI,$\overline{RE}$
CMOS Logic Input Current, I_{N1}			±2	µA	DE,DI,$\overline{RE}$
Input Current (A,B), I_{N2}			1.0	mA	V_{IN} = 12V DE = 0V
			-0.8	mA	V_{IN} = -7V VCC = 0V or 3.6V
Output Leakage (Y,Z), I_O			20	µA	V_{IN} = 12V DE = 0V, $\overline{RE}$ = 0V
			-20	µA	V_{IN} = -7V VCC = 0V or 3.6V
Output Leakage (Y,Z) in Shudown Mode, I_O		1		µA	V_{IN} = 12V DE = 0V, $\overline{RE}$ = 0V
		-1		µA	V_{IN} = -7V VCC = 0V or 3.6V
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	-0.2		0.2	V	-7V<V_{CM}<+12V
Input Hysteresis, Δ V_{TH}		50		mV	V_{CM}=0V
CMOS Output Voltage High, V_{OH}	Vcc – 0.4			V	I_{OUT}= -1.5mA V_{ID} = 200mV, Figure 5
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT}= 2.5mA, V_{ID} = 200mV, Figure 5
Three-State Output Leakage Current, I_{OZR}			±1	µA	Vcc = 3.6V, 0V ≤ V_{OUT} ≤ Vcc
Input Resistance , R_{IN}	12			kΩ	-7V<V_{CM}<+12V
POWER SUPPLY CURRENT					
Supply Current		1.1	2.2	mA	DE = V_{CC} $\overline{RE}$ = 0V or V_{CC} No Load,
		0.95	1.9	mA	DE = V_{CC} DI = 0V or V_{CC} $\overline{RE}$ = 0V
Supply Current in Shutdown Mode, I_{SHDN}		0.002	1	µA	DE = 0V, $\overline{RE}$ = V_{CC}, DI = V_{CC} or 0V
Driver Short-Circuit Output Current, I_{OSD}			-250	mA	V_{OUT} = -7V
			250	mA	V_{OUT} = 12V
Receiver Short-Circuit Output Current, I_{OSR}	±8		±60	mA	0V < V_{RO} < V_{CC}

TIMING SPECIFICATIONS-ADM3485/ADM3490 (V_{CC}=3.3V, T_A= 25°)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Delay, t_{DD}	1	22	35	ns	R_L = 60Ω, Figure 6
Differential Output Transition Time, t_{TD}	3	8	25	ns	R_L = 60Ω, Figure 6
Propagation Delay, Low-to-High Level, t_{PLH}	7	22	35	ns	R_L = 27Ω, Figure 7
Propagation Delay, High-to-Low Level, t_{PHL}	7	22	35	ns	R_L = 27Ω, Figure 7
$\|t_{PLH} - t_{PHL}\|$ Propagation Delay Skew (Note 2), t_{PDS}			8	ns	R_L = 27Ω, Figure 7
DRIVER OUTPUT ENABLE/DISABLE TIMES (ADM3485 ONLY)					
Output Enable Time Low Level, t_{PZL}		45	90	ns	R_L = 110Ω, Figure 8
Output Enable Time High Level, t_{PZH}		45	90	ns	R_L = 110Ω, Figure 8
Output Enable Time from High Level, t_{PHZ}		40	80	ns	R_L = 110Ω, Figure 8
Output Enable Time from Low Level, t_{PLZ}		40	80	ns	R_L = 110Ω, Figure 9
Output Enable Time from Shutdown to Low Level, t_{PSL}		650	900	ns	R_L = 110Ω, Figure 9
Output Enable Time from Shutdown to High Level, t_{PSH}		650	900	ns	R_L = 110Ω, Figure 8

TIMING SPECIFICATIONS-ADM3483/ADM3488 (V_{CC}=3.3V, T_A= 25°)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Delay, t_{DD}	600	900	1400	ns	R_L = 60Ω, Figure 6
Differential Output Transition Time, t_{TD}	400	700	1200	ns	R_L = 60Ω, Figure 6
Propagation Delay, Low-to-High Level, t_{PLH}	700	1000	1500	ns	R_L = 27Ω, Figure 7
Propagation Delay, High-to-Low Level, t_{PHL}	700	1000	1500	ns	R_L = 27Ω, Figure 7
$\|t_{PLH} - t_{PHL}\|$ Propagation Delay Skew (Note 2), t_{PDS}		100		ns	R_L = 27Ω, Figure 7
DRIVER OUTPUT ENABLE/DISABLE TIMES (ADM3485 ONLY)					
Output Enable Time Low Level, t_{PZL}		900	1300	ns	R_L = 110Ω, Figure 9
Output Enable Time High Level, t_{PZH}		600	800	ns	R_L = 110Ω, Figure 8
Output Enable Time from High Level, t_{PHZ}		50	80	ns	R_L = 110Ω, Figure 8
Output Enable Time from Low Level, t_{PLZ}		50	80	ns	R_L = 110Ω, Figure 9
Output Enable Time from Shutdown to Low Level, t_{PSL}		1.9	2.7	ns	R_L = 110Ω, Figure 9
Output Enable Time from Shutdown to High Level, t_{PSH}		2.2	3.0	ns	R_L = 110Ω, Figure 8

TIMING SPECIFICATIONS (V_{CC}=3.3V, T_A= 25°)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RECEIVER					
Time to Shutdown, t_{SHDN}	80	190	300	ns	ADM3483/ADM3485 only, Note 3
Propagation Delay, Low-to-High Level, t_{RPLH}	25	65	90	ns	V_{ID} = 0V to 3.0V, C_L = 15pF, Figure 10
	25	75	120	ns	ADM3483/ADM3488 only.
Propagation Delay, High-to-Low Level, t_{RPHL}	25	65	90	ns	V_{ID} = 0V to 3.0V, C_L = 15pF, Figure 10
	25	75	120	ns	ADM3483/ADM3488 only.
$\lvert t_{PLH} - t_{PHL} \rvert$ Propagation Delay Skew, t_{RPDS}			10	ns	V_{ID} = 0V to 3.0V, C_L = 15pF, Figure 10
			20	ns	ADM3483/ADM3488 only.
Output Enable Time to Low Level, t_{PRZL}		25	50	ns	C_L = 15pF, Figure 11, ADM3483/ADM3485 only
Output Enable Time to High Level, t_{PRZH}		25	50	ns	C_L = 15pF, Figure 11, ADM3483/ADM3485 only
Ouput Disable Time from High Level, t_{PRHZ}		25	45	ns	C_L = 15pF, Figure 116, ADM3483/ADM3485 only
Ouput Disable Time from Low Level, t_{PRLZ}		25	45	ns	C_L = 15pF, Figure 11, ADM3483/ADM3485 only
Output Enable Time from Shutdown to Low Level, t_{PRSL}		720	1400	ns	C_L = 15pF, Figure 11, ADM3483/ADM3485 only
Output Enable Time from Shutdown to High Level, t_{PRSH}		720	1400	ns	C_L = 15pF, Figure 11, ADM3483/ADM3485 only

Note1: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when DI input changes state.
Note 2: Measured on $\lvert t_{PLH}$ (Y) - t_{PHL} (Y) $\rvert$ and $\lvert t_{PLH}$ (Z) - t_{PHL} (Z) $\rvert$.
Note 3: The transceivers are put into shutdown by bringing RE high and DE low. If the inputs are in this state for less than 80ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 300ns, the part are guaranteed to have entered shutdown.

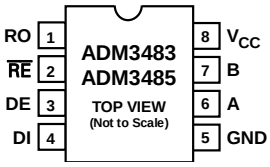
AB1SOLUTE MAXIMUM RATINGS

Table 2. (T_A = 25°C unless otherwise noted)

Parameter	Rating
V_{CC} to GND	TBD
Digital I/O Voltage (DE, $\overline{RE}$, DI, ROUT)	TBD
Driver Output/Receiver Input Voltage	TBD
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
θ_{JA} Thermal Impedance	
SOIC	110°C/W
LFCSP	62°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapour Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



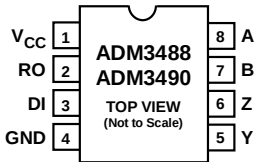


Table 3. ADM3483/ADM3485 Pin Descriptions

Pin No.	Mnemonic	Description
1	RO	Receiver Output. When enabled, if A > B by 200 mV, then RO = high. If A < B by 200 mV, then RO = low.
2	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential inputs A and B. A low level places it in a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high while a logic high on DI forces A high and B low.
5	GND	Ground.
6	A	Noninverting Receiver Input A/Driver Output A.
7	B	Inverting Receiver Input B/Driver Output B.
8	V_{CC}	5 V Power Supply.

Table 4. ADM34884/ADM3490 Pin Descriptions

Pin No.	Mnemonic	Description
1	V_{CC}	5 V Power Supply.
2	RO	Receiver Output. When enabled, if A > B by 200 mV, then RO = high. If A < B by 200 mV, then RO = low.
3	DI	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high while a logic high on DI forces A high and B low.
4	GND	Ground.
5	Y	Driver Noninverting Output.
6	Z	Driver Inverting Output.
7	B	Receiver Inverting Input.
8	A	Receiver Noninverting Input.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

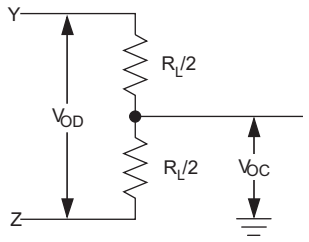


Figure 3. Driver V_{OD} and V_{OC}

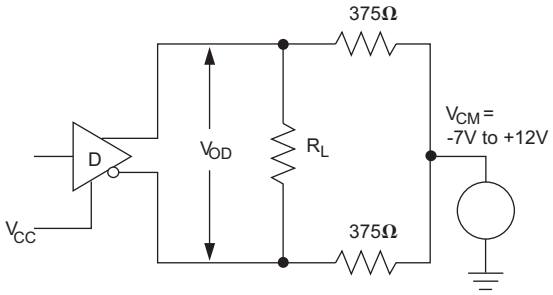


Figure 4. Driver V_{OD} with Varying Common-Mode Voltage

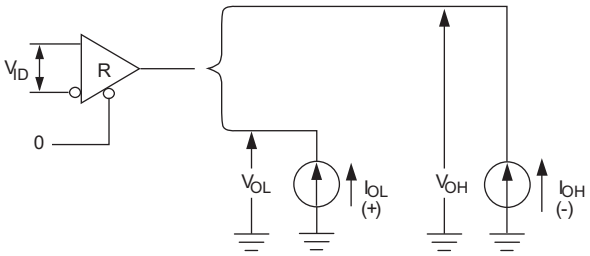
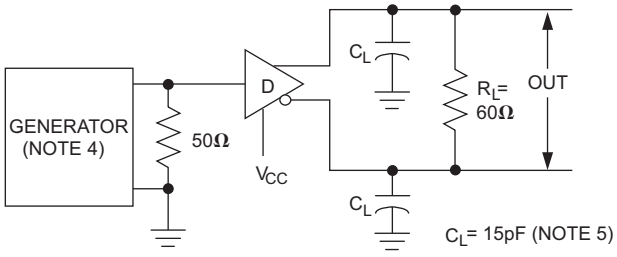


Figure 5. Receiver V_{OH} and V_{OL}



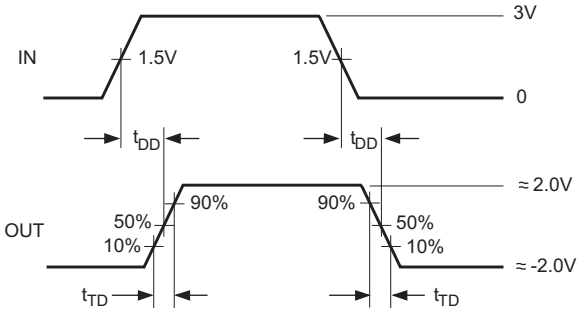
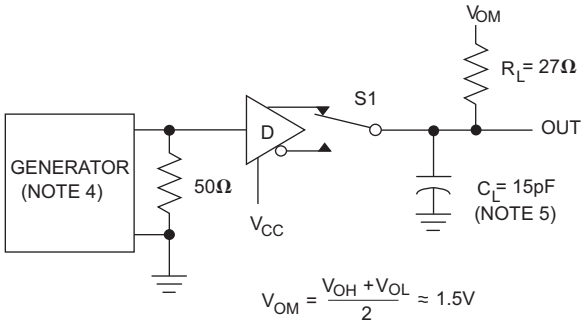


Figure 6. Driver Differential Output Delay and Transition Times



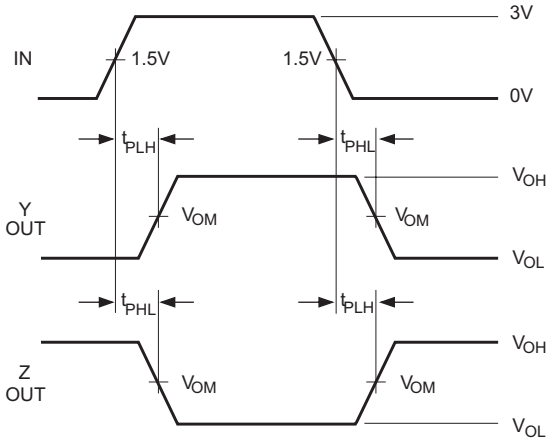


Figure 7. Driver Propagation Delays

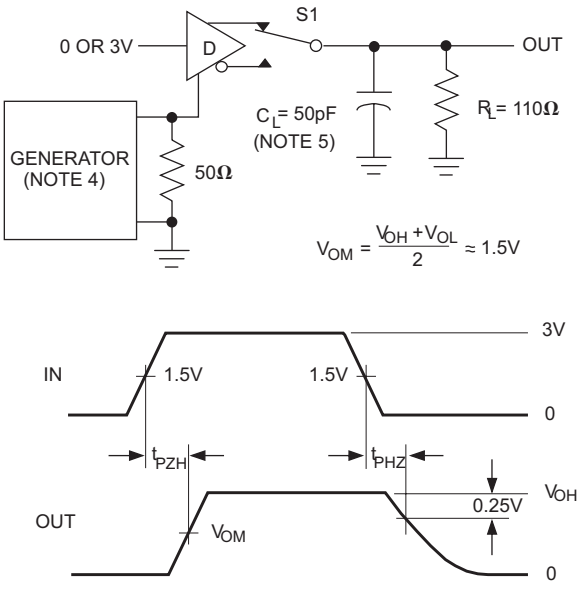


Figure 8. Driver Enable and Disable Times (t_{PZH}, t_{PSH}, t_{PHZ})

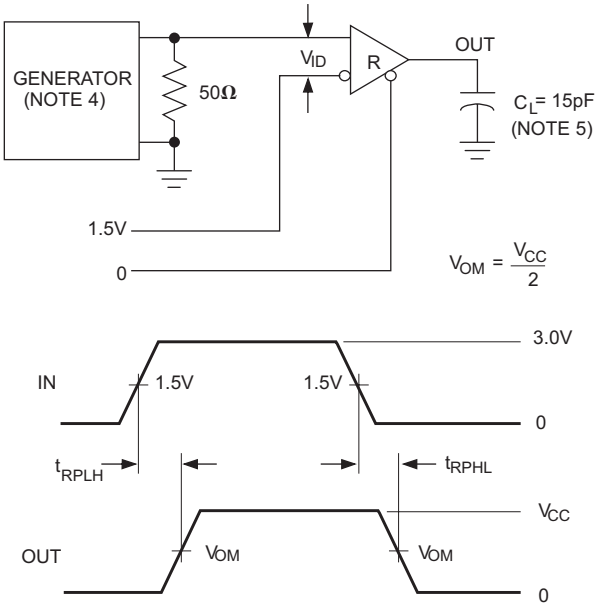


Figure 10. Receiver Propagation Delay

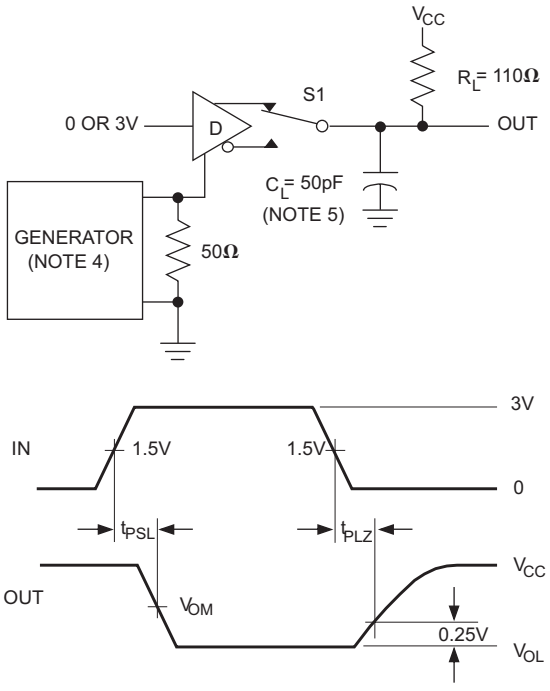


Figure 9. Driver Enable and Disable Times (t_{PZL}, t_{PSL}, t_{PLZ})

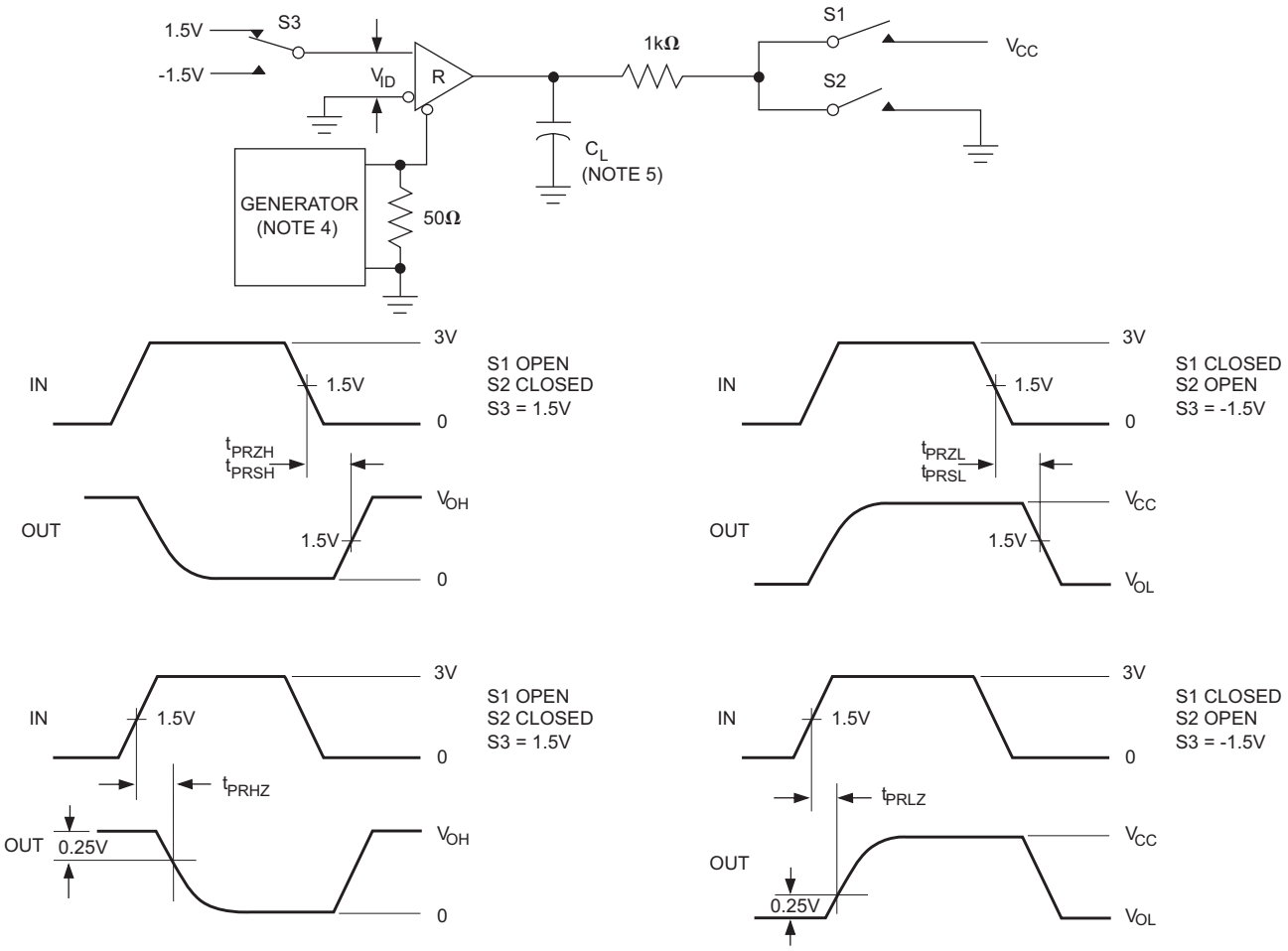


Figure 11. Receiver Enable and Disable Times

TYPICAL PERFORMANCE CHARACTERISTICS

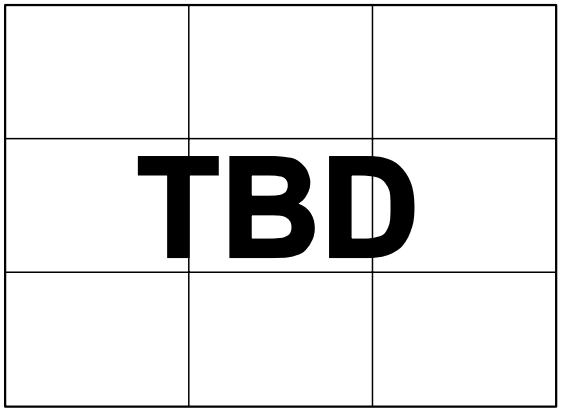


Figure 1. Output Current vs. Receiver Output Low Voltage

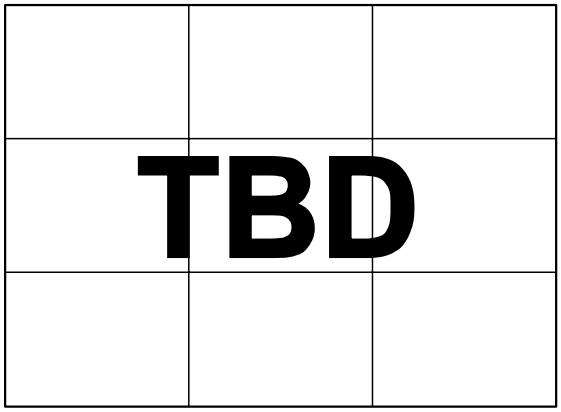


Figure 4. Receiver Output Low Voltage vs. Temperature

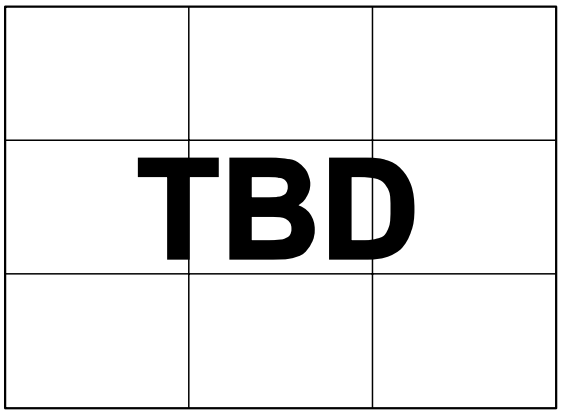


Figure 2. Output Current vs. Receiver Output High Voltage

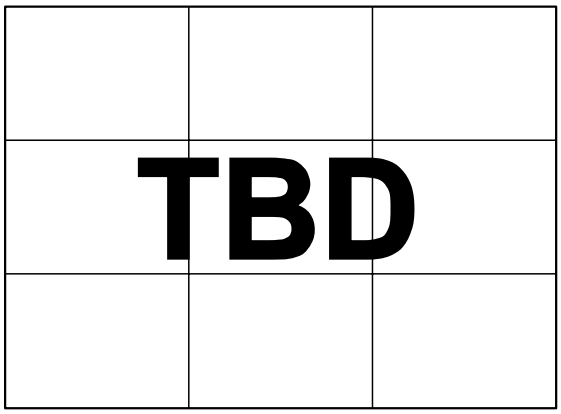


Figure 5. Driver Output Current vs. Differential Output Voltage

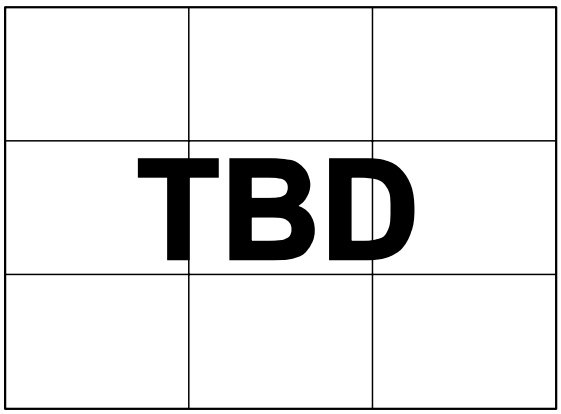


Figure 3. Receiver Output High Voltage vs. Temperature

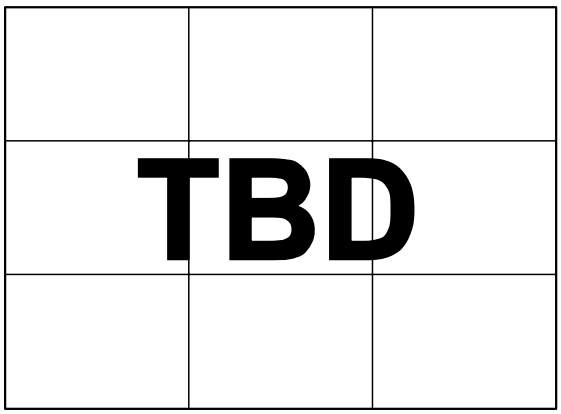


Figure 6. Driver Differential Output Voltage vs. Temperature

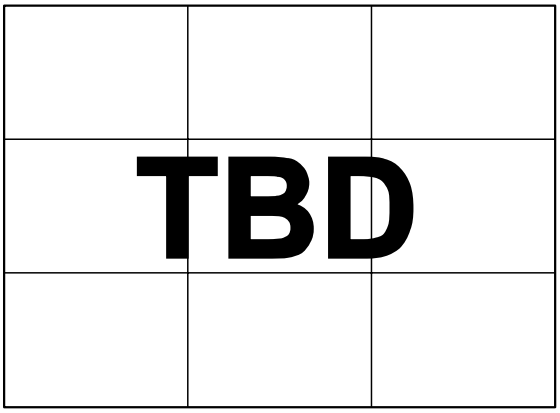


Figure 7. Output Current vs. Driver Output Low Voltage

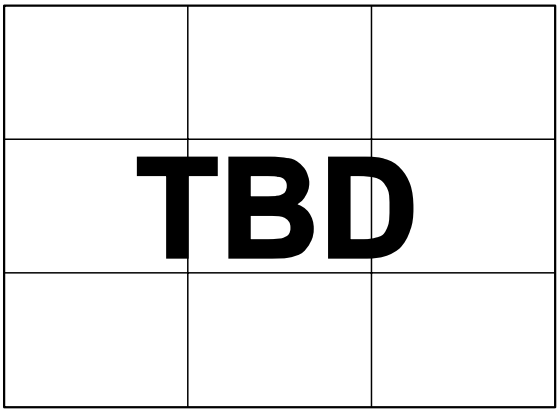


Figure 10. Shutdown Current vs. Temperature

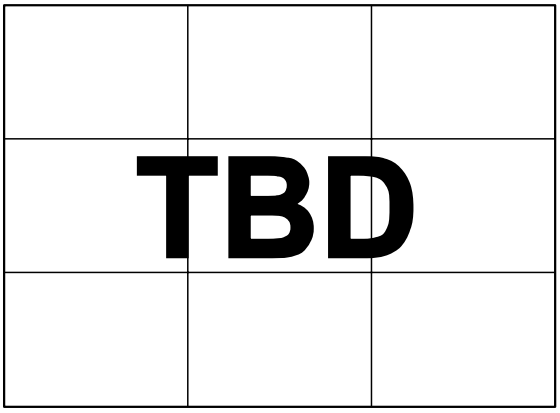


Figure 8. Output Current vs. Driver Output High Voltage

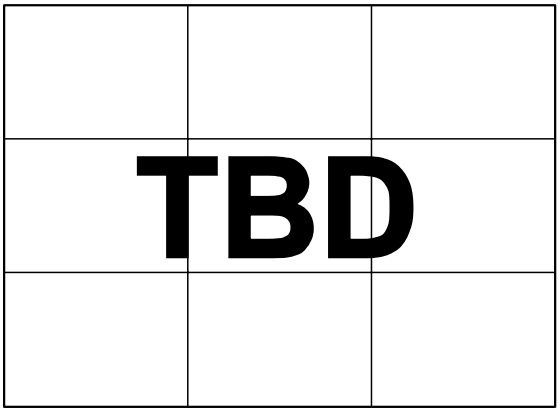


Figure 11. TBD

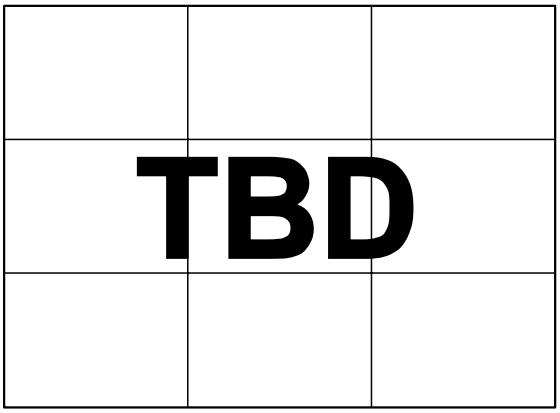


Figure 9.Supply Current vs. Temperature

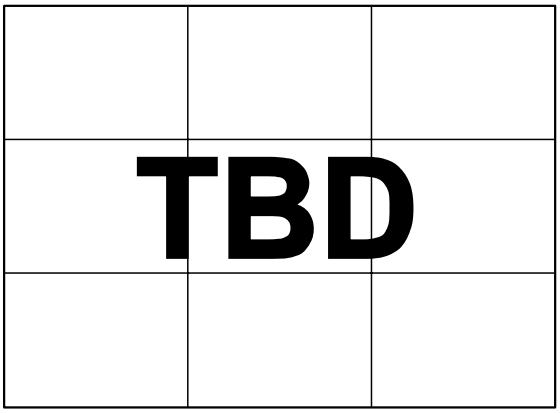


Figure 12. TBD

CIRCUIT DESCRIPTION

The ADM3483/ADM3485/ADM 3488/ADM3490 are low-power transceivers for RS-485 and RS-422 communications. The ADM3483 and ADM3488 can transmit and receive at data rates up to 250kbps, and the ADM3485/ ADM3490 at up to 10Mbps. The ADM3488/ ADM3490 are full-duplex transceivers, while the ADM3483/ADM3485 are half-duplex. Driver Enable (DE) and Receiver Enable (RE) pins are included on the ADM3483/ADM3485. When disabled, the driver and receiver outputs are high impedance.

DEVICES WITH RECEIVER/DRIVER ENABLES (ADM3483/ADM2485)

Inputs			Outputs		Mode
$\overline{RE}$	DE	DI	B*	A*	
X	1	1	0	1	Normal
X	1	0	1	0	Normal
0	0	X	High-Z	High-Z	Normal
1	0	X	High-Z	High-Z	Shutdown

Table x. Transmitting Truth Table

Inputs			Outputs	Mode
$\overline{RE}$	DE	A,B	RO	
0	0*	≥+0.2V	1	Normal
0	0*	≤-0.2V	0	Normal
0	0*	Inputs Open	1	Normal
1	0	x	High-Z	Shutdown

Table x. Receiving Truth Table

DEVICES WITHOUT RECEIVER/DRIVER ENABLES (ADM3488/ADM2490)

Input	Outputs	
DI	Z	Y
1	0	1
0	1	0

Table x. Transmitting Truth Table

Input	Outputs
A,B	RO
≥+0.2	0
≤ -0.2	1
Inputs Open	1

Table x. Receiving Truth Table

REDUCED EMI AND REFLECTIONS

(ADM3483/ ADM3488)

The ADM3483/ADM3488 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables.

LOW-POWER SHUTDOWN MODE

(ADM3483/ADM3485)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled (high impedance). In shutdown, the devices typically draw only 2nA of supply current. For these devices, the t_{PSH} and t_{PSL} enable times assume the part was in the low-power shutdown mode; the t_{PZH} and t_{PZL} enable times assume the receiver or driver was disabled, but the part was not shut down.

DRIVER OUTPUT PROTECTION

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two methods. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see Typical Performance Characteristics). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

PROPAGATION DELAY

Skew time is simply the difference between the low-to-high and high-to-low propagation delay. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle). The receiver skew time, |tPRLH - tPRHL|, is under 10ns (20ns for the ADM3483/ADM3488). The driver skew times are 8ns for the ADM485/ADM3490, and typically under 100ns for the ADM3483/ADM3488.

LINE LENGTH VS. DATA RATE

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 13.

TYPICAL APPLICATIONS

The ADM3483, ADM3485, ADM3488 and ADM3490 transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 11 and 12 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 13. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited ADM3483/ADM3488 are more tolerant of imperfect termination.

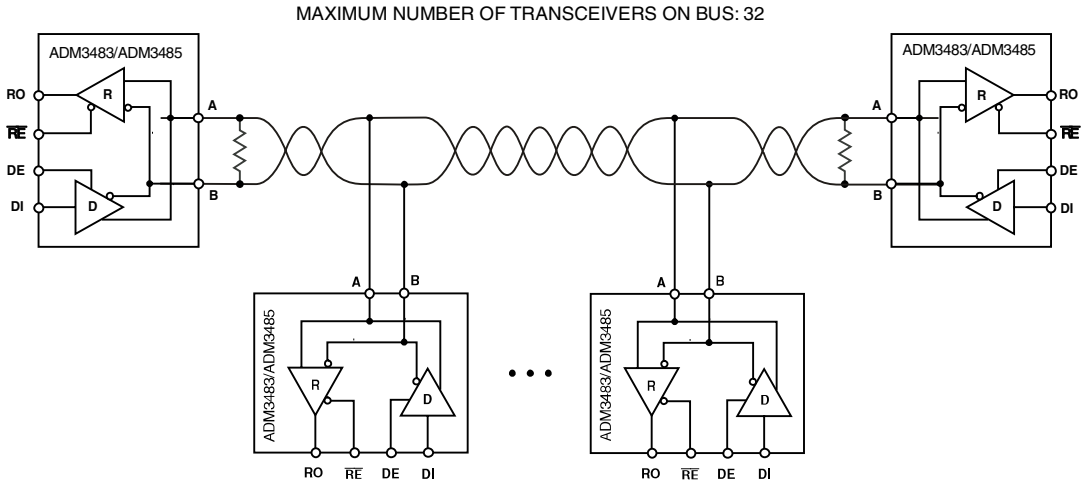


Figure 11. ADM3483/ADM3485 Typical RS-485 Network

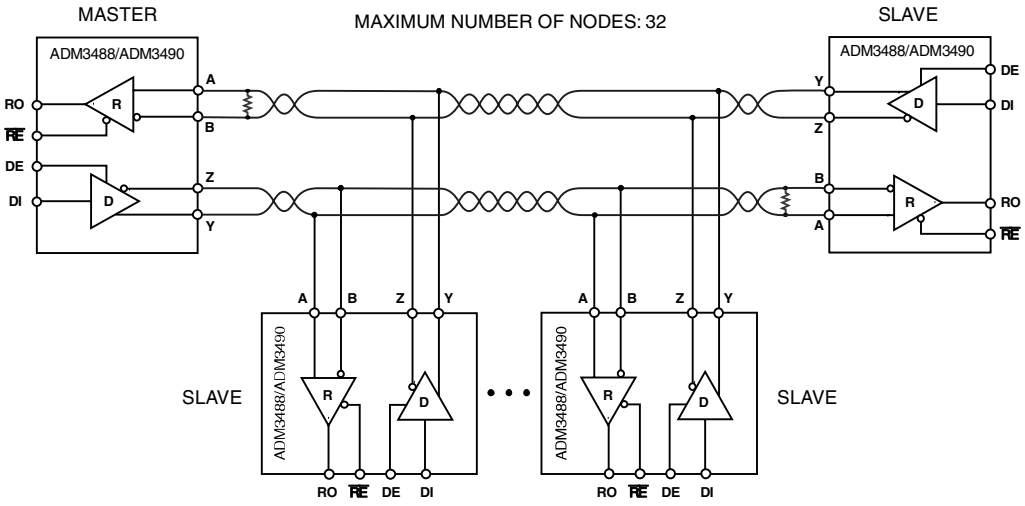


Figure 12. ADM3488/ADM3490 Full Duplex RS-485 Network

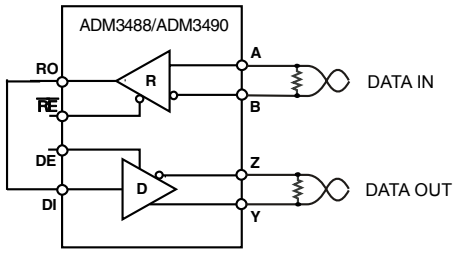


Figure 13. Line Repeater for ADM3488/ADM3490

OUTLINE DIMENSIONS

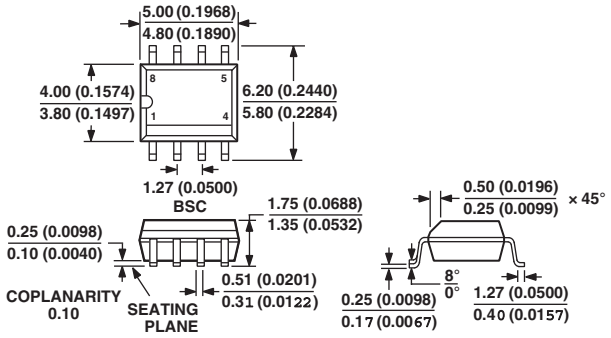


Figure 6. 8-Lead Standard Small Outline Package [SOIC]

(R-8)

Dimensions shown in millimeters

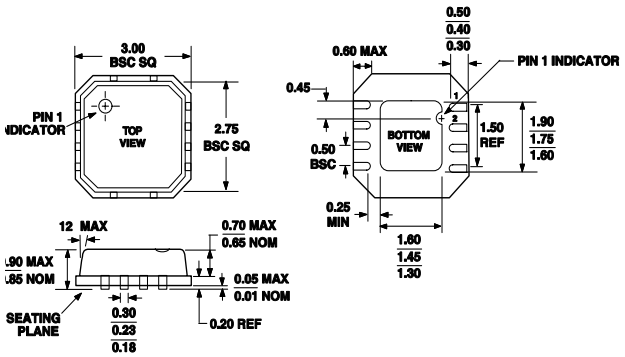


Figure 7. 8-Lead Lead Frame Chip Scale Package [LFCSP]

(CP-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Type	Branding
ADM3483AR	–40°C to +85°C	R-8	
ADM3483ACP	–40°C to +85°C	CP-8	
ADM3485AR	–40°C to +85°C	R-8	
ADM3485ACP	–40°C to +85°C	CP-8	
ADM3488AR	–40°C to +85°C	R-8	
ADM3490AR	–40°C to +85°C	R-8	

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