



Revision History

- **September 28, 1998**
Datasheet Released.

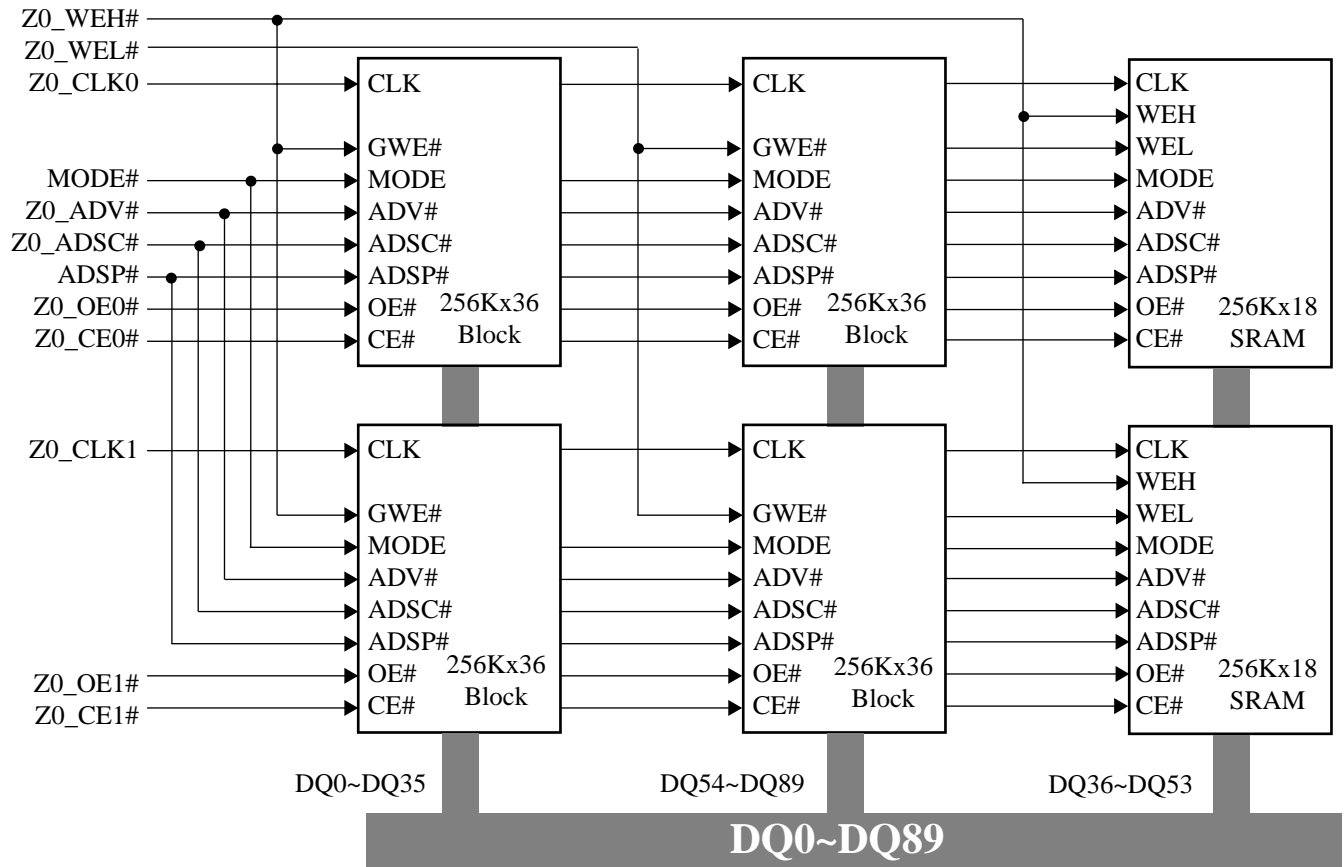


**4MByte (512K x 90) Synchronous Secondary Cache SRAM Module - 256Kx18 based
168-pin DIMM**

Features

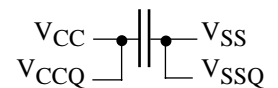
- Access Time : 10/15/20ns
- Operating Voltage : 3.3V
- Device Physicals : BGA
- Lead Finish : Gold
- Length x Height : 133.35mm x 22.22mm
- No. of sides : Double-sided

Functional Diagram



Notes :

1. Each 256Kx36 block comprises of two 256Kx18 SRAM devices.
2. A0~A17 to all SRAM devices.
3. CE2 & CE2# of all devices are tied active.
4. All other unused control signals are tied inactive except for BWE signal on parity devices, which is tied active.



Decoupling capacitors to all devices.

(All specifications of this device are subject to change without notice.)



Pin Name

| | | | |
|------------------|--------------------------------|------------------------|------------------------|
| A0~A17 | Addresses | AV0_CE0_N#, AV0_CE1_N# | Control Select Signals |
| DQ0~DQ89 | Data Inputs/Outputs | AV1_CE0_N#, AV1_CE1_N# | |
| Z0_CLK0, Z0_CLK1 | Clock Inputs | Z0_OE0#, Z0_OE1# | Output Enable Inputs |
| Z0_WEH#, Z0_WEL# | Write Enable Inputs | Z0_CE0#, Z0_CE1# | Chip Enable Inputs |
| Z0_ADSC# | Cache Address Status Input | MSIZE0_N#, MSIZE1_N# | Presence Detects |
| Z0_ADV# | Burst Address Advance Input | V _{CC} | Power Supply |
| ADSP# | Processor Address Status Input | V _{SS} | Ground |
| | | NC | No Connection |

| Pin No. | Pin Designation | Pin No. | Pin Designation | Pin No. | Pin Designation | Pin No. | Pin Designation |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 1 | V _{SS} | 43 | Z0_ADV# | 85 | V _{SS} | 127 | Z0_ADSC# |
| 2 | DQ0 | 44 | Z1_ADV# / NC | 86 | DQ9 | 128 | Z1_ADSC# / NC |
| 3 | DQ1 | 45 | V _{SS} | 87 | DQ10 | 129 | V _{SS} |
| 4 | DQ2 | 46 | Z0_CLK0 | 88 | DQ11 | 130 | Z0_CLK1 |
| 5 | DQ3 | 47 | V _{SS} | 89 | DQ12 | 131 | V _{SS} |
| 6 | DQ4 | 48 | Z1_CLK0 | 90 | DQ13 | 132 | Z1_CLK1 / NC |
| 7 | V _{CC} | 49 | V _{SS} | 91 | V _{CC} | 133 | V _{SS} |
| 8 | DQ5 | 50 | DQ36 | 92 | DQ14 | 134 | DQ45 |
| 9 | DQ6 | 51 | DQ37 | 93 | DQ15 | 135 | DQ46 |
| 10 | DQ7 | 52 | DQ38 | 94 | DQ16 | 136 | DQ47 |
| 11 | DQ8 | 53 | DQ39 | 95 | DQ17 | 137 | DQ48 |
| 12 | DQ18 | 54 | DQ40 | 96 | DQ27 | 138 | DQ49 |
| 13 | V _{SS} | 55 | V _{CC} | 97 | V _{SS} | 139 | V _{CC} |
| 14 | DQ19 | 56 | DQ41 | 98 | DQ28 | 140 | DQ50 |
| 15 | DQ20 | 57 | DQ42 | 99 | DQ29 | 141 | DQ51 |
| 16 | DQ21 | 58 | DQ43 | 100 | DQ30 | 142 | DQ52 |
| 17 | DQ22 | 59 | DQ44 | 101 | DQ31 | 143 | DQ53 |
| 18 | DQ23 | 60 | DQ54 | 102 | DQ32 | 144 | DQ63 |
| 19 | V _{CC} | 61 | V _{CC} | 103 | V _{CC} | 145 | V _{CC} |
| 20 | DQ24 | 62 | DQ55 | 104 | DQ33 | 146 | DQ64 |
| 21 | DQ25 | 63 | DQ56 | 105 | DQ34 | 147 | DQ65 |
| 22 | DQ26 | 64 | DQ57 | 106 | DQ35 | 148 | DQ66 |
| 23 | MSIZE0_N# | 65 | DQ58 | 107 | MSIZE1_N# | 149 | DQ67 |
| 24 | A0 | 66 | DQ59 | 108 | A5 | 150 | DQ68 |
| 25 | A1 | 67 | V _{SS} | 109 | A6 | 151 | V _{SS} |
| 26 | A2 | 68 | DQ60 | 110 | A7 | 152 | DQ69 |
| 27 | A3 | 69 | DQ61 | 111 | A8 | 153 | DQ70 |
| 28 | A4 | 70 | DQ62 | 112 | A9 | 154 | DQ71 |
| 29 | V _{SS} | 71 | DQ72 | 113 | V _{SS} | 155 | DQ81 |
| 30 | A10 | 72 | DQ73 | 114 | A15 | 156 | DQ82 |
| 31 | A11 | 73 | V _{CC} | 115 | A16 | 157 | V _{CC} |
| 32 | A12 | 74 | DQ74 | 116 | A17 | 158 | DQ83 |
| 33 | A13 | 75 | DQ75 | 117 | A18/NC | 159 | DQ84 |
| 34 | A14 | 76 | DQ76 | 118 | A19/NC | 160 | DQ85 |
| 35 | V _{CC} | 77 | DQ77 | 119 | V _{CC} | 161 | DQ86 |
| 36 | Z0_CE0# | 78 | DQ78 | 120 | Z0_CE1# | 162 | DQ87 |
| 37 | Z1_CE0# / NC | 79 | V _{SS} | 121 | Z1_CE1# / NC | 163 | V _{SS} |
| 38 | Z0_WEL# | 80 | DQ79 | 122 | Z0_WEH# | 164 | DQ88 |
| 39 | Z1_WEL# / NC | 81 | DQ80 | 123 | Z1_WEH# / NC | 165 | DQ89 |
| 40 | ADSP# | 82 | AV0_CE0_N# | 124 | MODE# | 166 | AV1_CE0_N# |
| 41 | Z0_OE0# | 83 | AV0_CE1_N# | 125 | Z0_OE1# | 167 | AV1_CE1_N# |
| 42 | Z1_OE0# / NC | 84 | V _{CC} | 126 | Z1_OE1# / NC | 168 | V _{CC} |

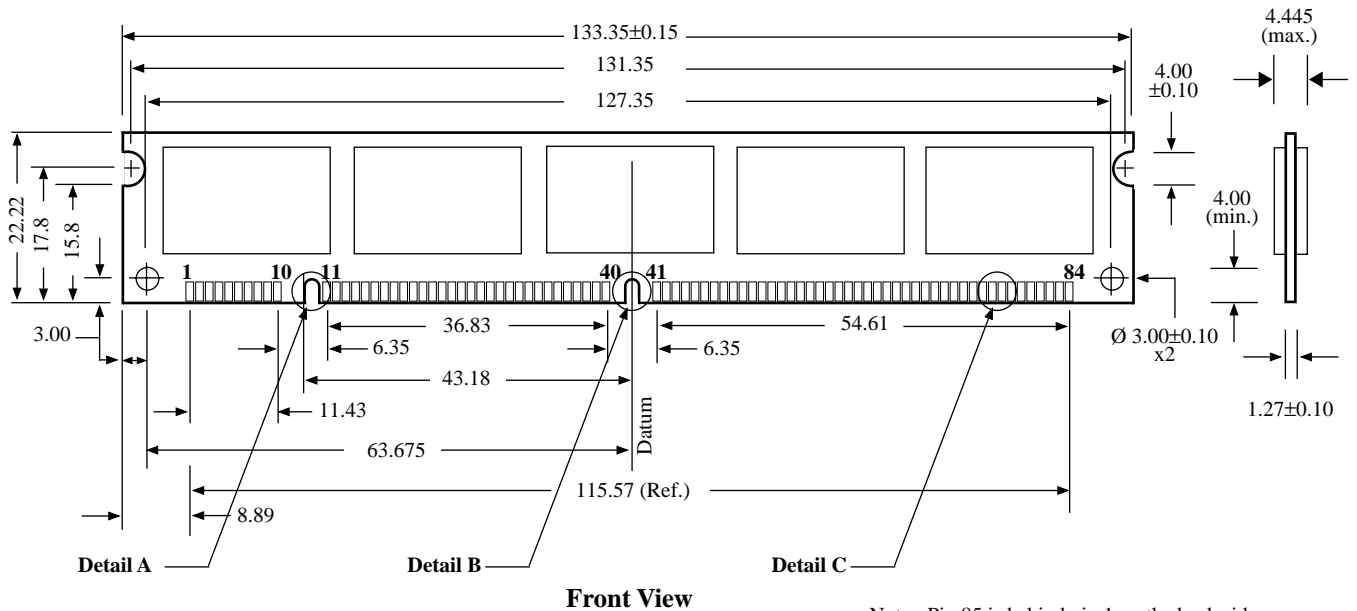
Note :

1. AV0_CE0_N#, MSIZE0_N#, and MSIZE1_N# are all grounded through a 10 ohms resistor.

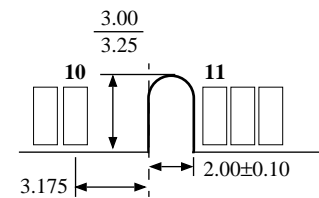


Physical Dimensions

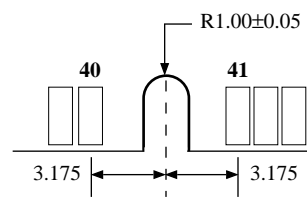
168-pin DIMM Module



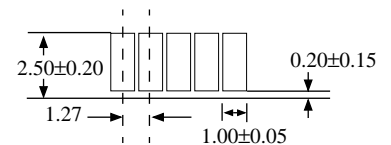
Note : Pin 85 is behind pin 1 on the back side.



Detail A : Position of Technology Notch



Detail B : Position of Voltage Notch



Detail C : Edge Connector

(All dimensions are in millimeters with ± 0.13 mm tolerance unless specified otherwise.)



Ordering Information

SM **3** **90** **H** **G** **SF** **N** **3** **U** **G** **UU**
 (1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11)

- (1) **SMART Modular Technologies**
- (2) **Product Category**
3 : SRAM SIMM / DIMM
- (3) **Module Data Bus Width**
90 : x90
- (4) **Module Address Depth**
H : 512K
- (5) **Device Data Width**
G : x18, BGA
- (6) **Device Feature / Customer**
S : Synchronous
F : Flow-through
- (7) **Tag Bits**
N : No Tag
- (8) **Voltage**
3 : 3.3V / Standard Power
- (9) **SRAM Device Manufacturer**
H : Hitachi
M : Micron
N : NEC
R : Sharp
S : Samsung
O : Motorola
- (10) **Module Lead Finish**
G : Gold
- (11) **Cycle Time**
10 : 10ns
15 : 15ns
20 : 20ns

Note : "U" in the part number should be replaced by user specified option.



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