Features

- **Temperature Ranges**
  - **— Commercial : 0°C to 70°C**
  - **— Industrial : −40°C to 85°C**
  - **— Automotive : −40°C to 125°C**
- **High speed: 55 ns and 70 ns**
- **70-ns speed bin offered in both Industrial and Automotive grades**
- **Wide voltage range: 2.7V-3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a standard 44-pin TSOP Type II (forward pinout) package**

Functional Description[1]

The CY62136V is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current.

This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}$ HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the Truth Table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram
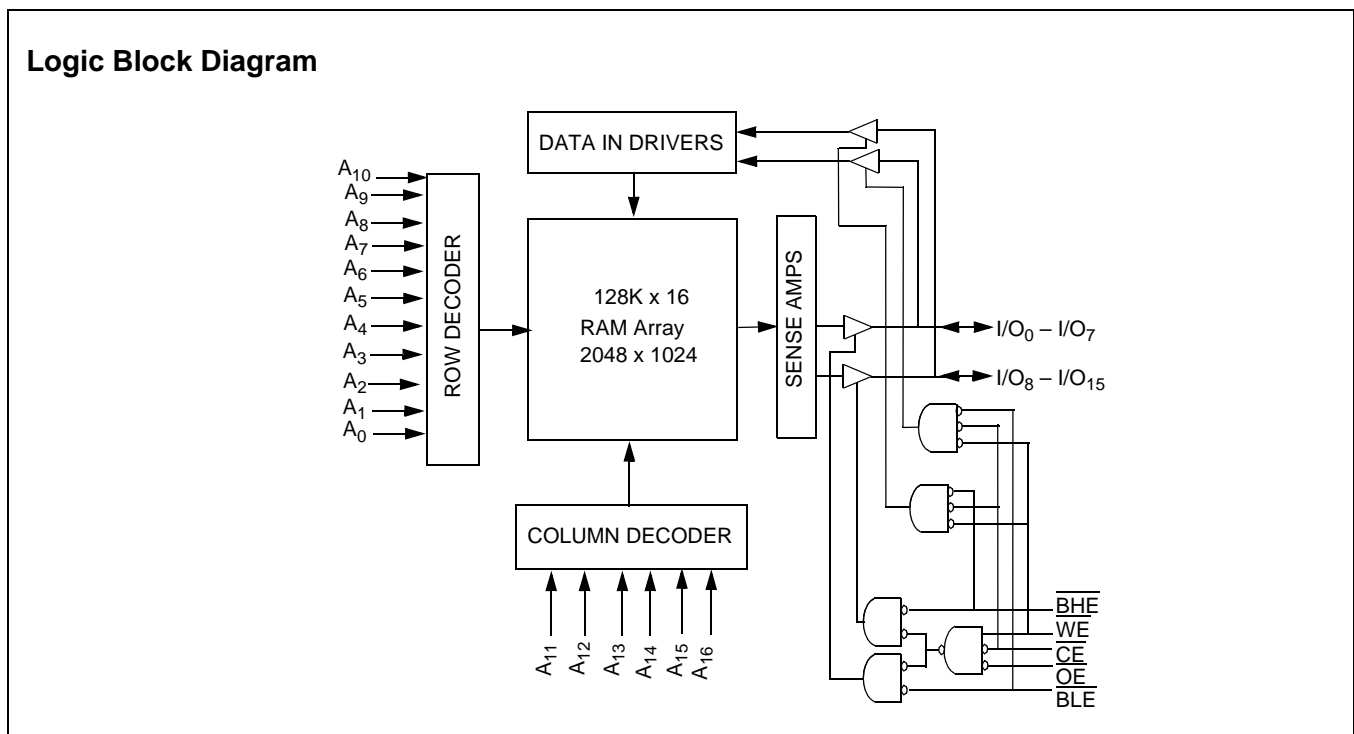
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Product Portfolio

Product	V_CC Range (V)			Speed	Grades	Power Dissipation (Industrial)			
						Operating, I_{CC} (mA)		Standby, I_{SB2} (μA)	
	Min	Typ.[2]	Max			Typ.[2]	Maximum	Typ.[2]	Maximum
CY62136VLL	2.7	3.0	3.6	55	Industrial	7	20	1	15
				70	Industrial	7	15	1	15
					Automotive	7	20	1	20
CY62136VSL				55	Industrial	7	20	1	5
				70	Industrial	7	15	1	5

Pin Configurations[3]

TSOP II (Forward)
Top View

Pin	#	#	Pin
A_4	1	44	A_5
A_3	2	43	A_6
A_2	3	42	A_7
A_1	4	41	$\overline{OE}$
A_0	5	40	$\overline{BHE}$
$\overline{CE}$	6	39	BLE
I/O_0	7	38	I/O_{15}
I/O_1	8	37	I/O_{14}
I/O_2	9	36	I/O_{13}
I/O_3	10	35	I/O_{12}
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
I/O_4	13	32	I/O_{11}
I/O_5	14	31	I/O_{10}
I/O_6	15	30	I/O_9
I/O_7	16	29	I/O_8
$\overline{WE}$	17	28	NC
A_{16}	18	27	A_8
A_{15}	19	26	A_9
A_{14}	20	25	A_{10}
A_{13}	21	24	A_{11}
A_{12}	22	23	NC

Notes:
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$ Typ, $T_A = 25°C$.
3. NC pins are not connected on the die

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied..−55°C to +125°C

Supply Voltage to Ground Potential ....−0.5V to +4.6V

DC Voltage Applied to Outputs
in High-Z State[4] ....−0.5V to V_{CC} + 0.5V

DC Input Voltage[4] ....−0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)........................... 20 mA

Static Discharge Voltage...> 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current..> 200 mA

Operating Range

Range	Ambient Temperature[T_A][6]	V_{CC}
Industrial	−40°C to +85°C	2.7V to 3.6V
Automotive	−40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			CY62136V-55 Min.	CY62136V-55 Typ.[2]	CY62136V-55 Max.	CY62136V-70 Min.	CY62136V-70 Typ.[2]	CY62136V-70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA	V_{CC} = 2.7V		2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V				0.4			0.4	V
V_{IH}	Input HIGH Voltage		V_{CC} = 3.6V		2.2		V_{CC}+0.5V	2.2		V_{CC}+0.5V	V
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V		−0.5		0.8	−0.5		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		Industrial	−1		+1	−1		+1	μA
				Automotive				−10		+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		Industrial	−1		+1	−1		+1	μA
				Automotive				−10		+10	μA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC},	V_{CC} = 3.6V, I_{OUT} = 0 mA, CMOS Levels	Industrial		7	20		7	15	mA
				Automotive					7	20	mA
		f = 1 MHz,				1	2		1	2	mA
I_{SB1}	Automatic CE Power-down Current— CMOS Inputs	CE ≥ V_{CC}−0.3V, V_{IN} ≥ V_{CC}−0.3V or V_{IN} ≤ 0.3V, f = f_{MAX}					100			100	μA
I_{SB2}	Automatic CE Power-down Current— CMOS Inputs	CE ≥ V_{CC}−0.3V V_{IN} ≥ V_{CC}−0.3V or V_{IN} ≤ 0.3V, f = 0	V_{CC} = 3.6V	Industrial(LL)		1	15		1	15	μA
				Industrial(SL)		1	5		1	5	μA
				Automotive					1	20	μA

Thermal Resistance

Parameter	Description	Test Conditions	TSOPII	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[5]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	60	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[5]		22	°C/W

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC}= $V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:
4. V_{IL}(min) = −2.0V for pulse durations less than 20 ns.
5. Tested initially and after any design or process changes that may affect these parameters.
6. T_A is the "Instant-On" case temperature.

AC Test Loads and Waveforms
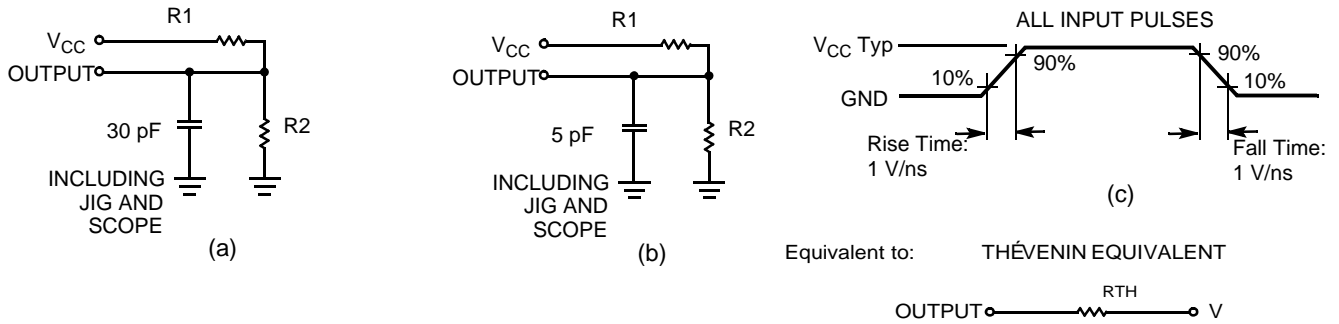
Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R$_{TH}$	645	Ohms
V$_{TH}$	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[8]		Min.	Typ.[2]	Max.	Unit
V$_{DR}$	V$_{CC}$ for Data Retention			1.0		3.6	V
I$_{CCDR}$	Data Retention Current	V$_{CC}$ = 1.0V, $\overline{CE} \geq$ V$_{CC}$ – 0.3V, V$_{IN} \geq$ V$_{CC}$ – 0.3V or V$_{IN} \leq$ 0.3V, No input may exceed V$_{CC}$ + 0.3V	LL		0.5	7.5	µA
			SL			5	
t$_{CDR}$[5]	Chip Deselect to Data Retention Time			0			ns
t$_R$[7]	Operation Recovery Time			70			ns

Data Retention Waveform
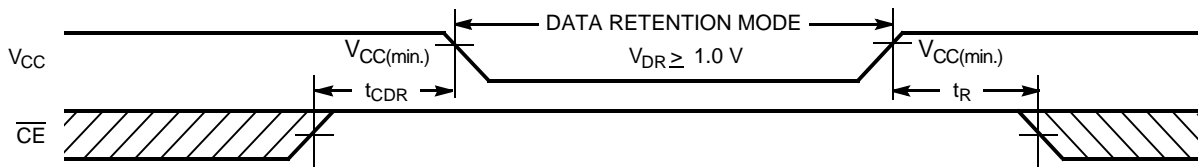
Switching Characteristics Over the Operating Range [8]

| Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t$_{RC}$	Read Cycle Time	55		70		ns
t$_{AA}$	Address to Data Valid		55		70	ns
t$_{OHA}$	Data Hold from Address Change	10		10		ns
t$_{ACE}$	$\overline{CE}$ LOW to Data Valid		55		70	ns
t$_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
t$_{LZOE}$	$\overline{OE}$ LOW to Low-Z[9]	5		5		ns

Notes:
7. Full device operation requires linear V$_{CC}$ ramp from V$_{DR}$ to V$_{CC(min)}$ $\geq$ 100 ms or stable at V$_{CC(min)}$ $\geq$ 100 ms.
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V$_{CC}$ typ., and output loading of the specified I$_{OL}$/I$_{OH}$ and 30-pF load capacitance.
9. At any given temperature and voltage condition, t$_{HZCE}$ is less than t$_{LZCE}$, t$_{HZOE}$ is less than t$_{LZOE}$, and t$_{HZWE}$ is less than t$_{LZWE}$ for any given device.
10. t$_{HZOE}$, t$_{HZCE}$, and t$_{HZWE}$ are specified with C$_L$ = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.

Switching Characteristics Over the Operating Range (continued)[8]

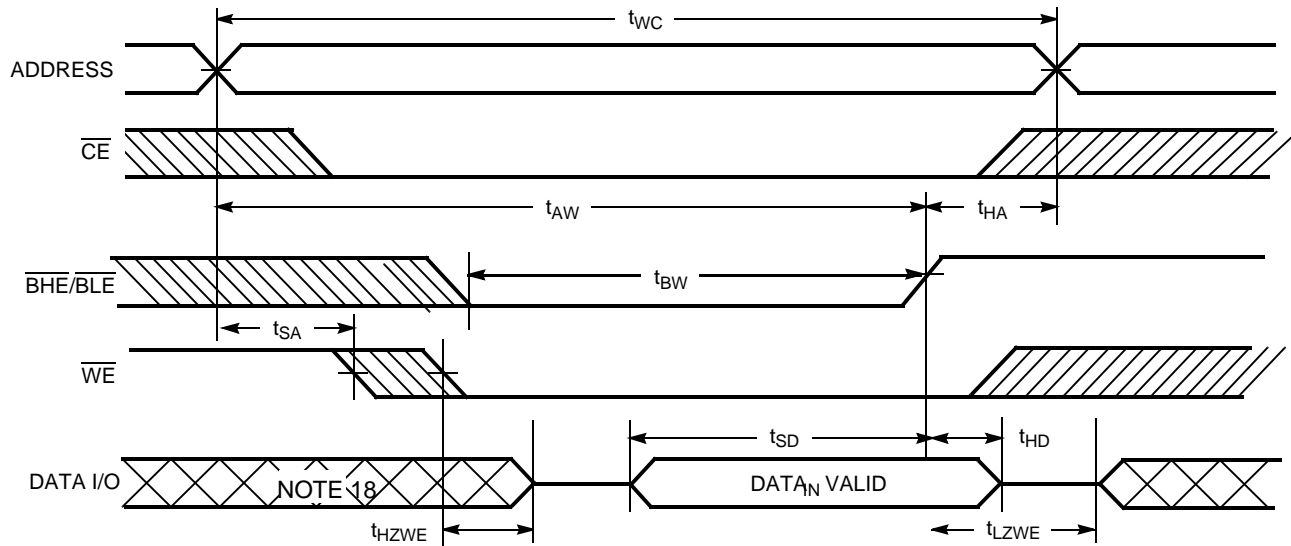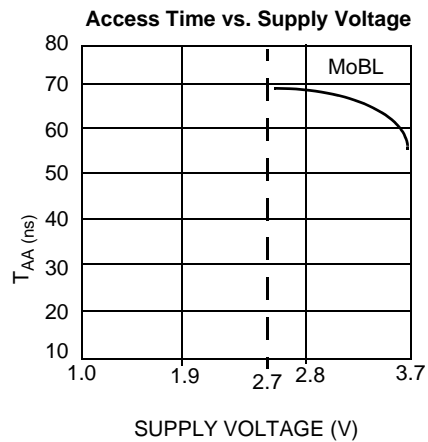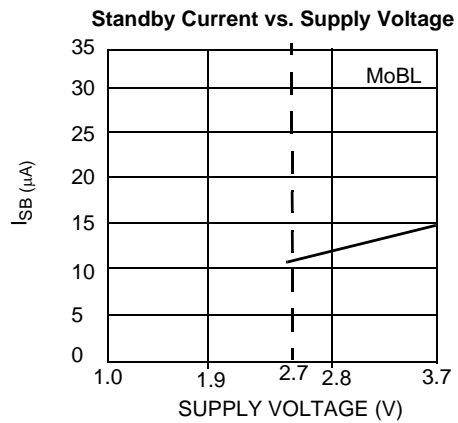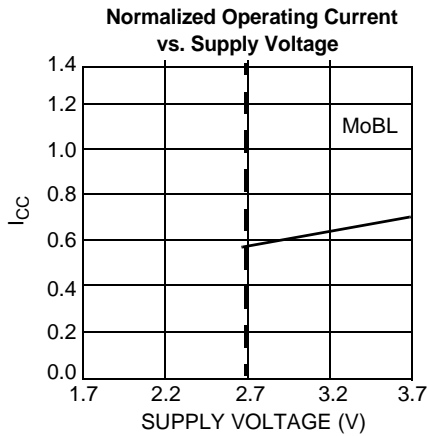| Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t_{HZOE}	OE HIGH to High-Z[9, 10]		25		25	ns
t_{LZCE}	CE LOW to Low-Z[9]	10		10		ns
t_{HZCE}	CE HIGH to High-Z[9, 10]		25		25	ns
t_{PU}	CE LOW to Power-up	0		0		ns
t_{PD}	CE HIGH to Power-down		55		70	ns
t_{DBE}	BLE / BHE LOW to Data Valid		25		35	ns
t_{LZBE}	BLE / BHE LOW to Low-Z[9, 10]	5		5		ns
t_{HZBE}	BLE / BHE HIGH to High-Z[11]		25		25	ns
Write Cycle[11, 12]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	CE LOW to Write End	45		60		ns
t_{AW}	Address Set-up to Write End	45		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	40		50		ns
t_{BW}	BLE / BHE LOW to Write End	50		60		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	WE LOW to High-Z[9, 10]		20		25	ns
t_{LZWE}	WE HIGH to Low-Z[9]	5		10		ns

Switching Waveforms

Read Cycle No. 1 [13, 14]
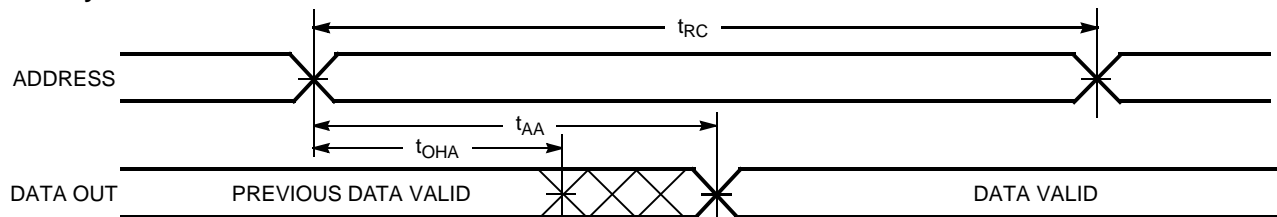
Notes:
11. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.
13. Device is continuously selected. OE, CE = V_{IL}.
14. WE is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 [14, 15]
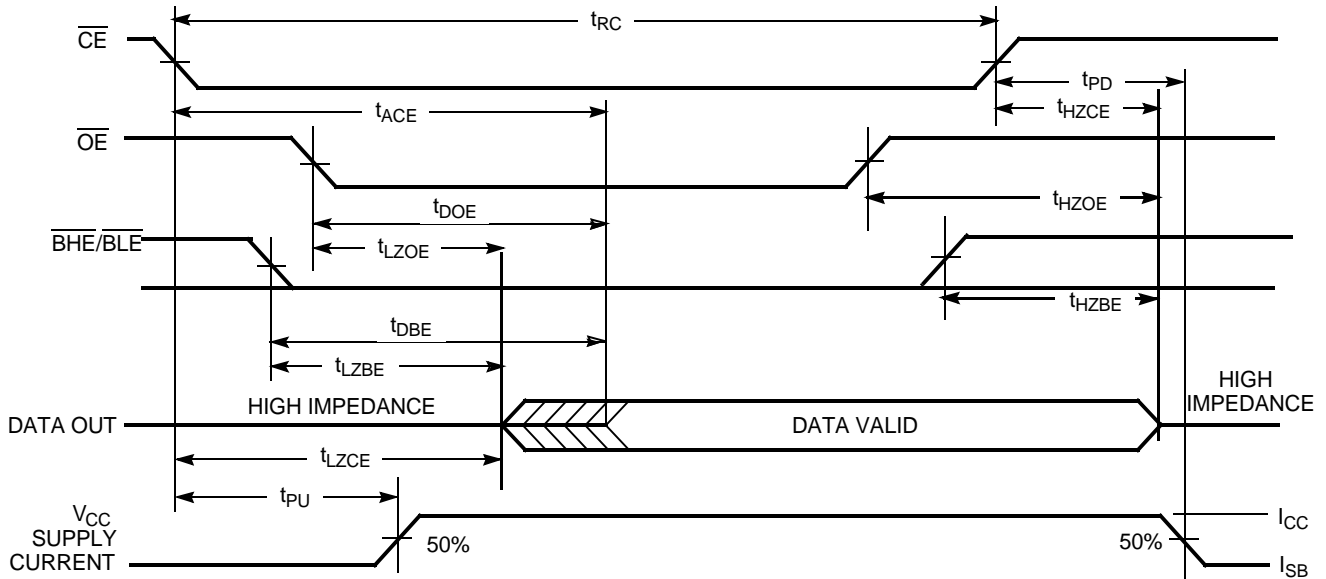
Write Cycle No. 1 (WE Controlled) [11, 16, 17]
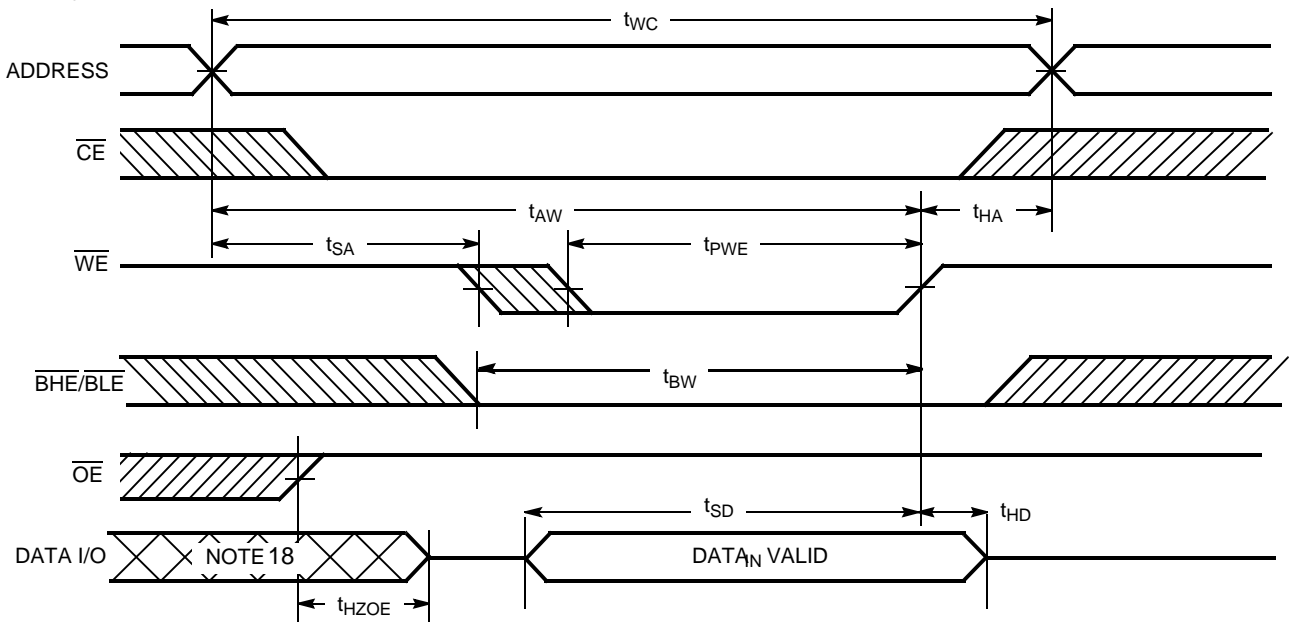
Notes:
15. Address valid prior to or coincident with CE transition LOW.
16. Data I/O is high impedance if OE = V_IH.
17. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

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Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled)[11, 16, 17]
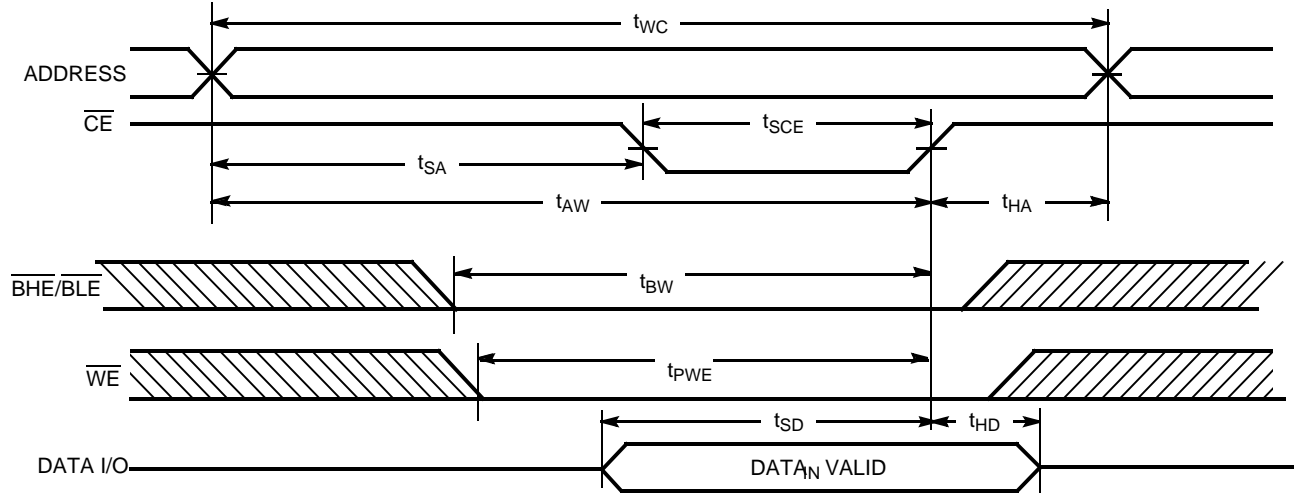
Write Cycle No. 3 (WE Controlled, OE LOW)[12, 17]

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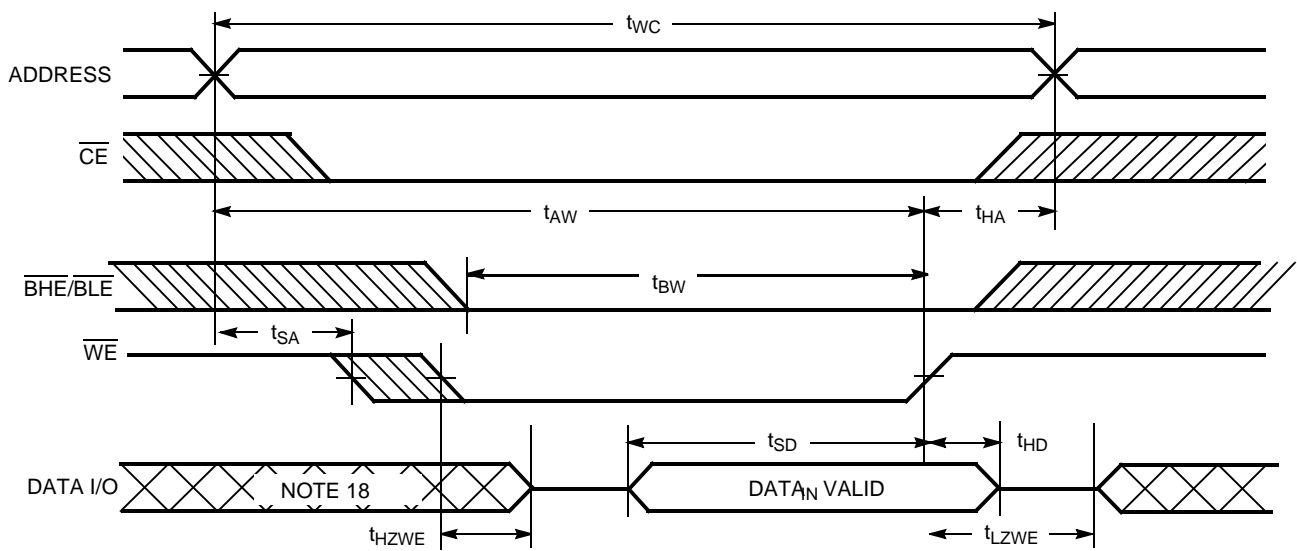
Switching Waveforms (continued)

Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[18]

Typical DC and AC Characteristics

Normalized Operating Current vs. Supply Voltage

Standby Current vs. Supply Voltage

Access Time vs. Supply Voltage

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Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	L	H	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62136VLL-55ZSI	ZS44	44-pin TSOP II	Industrial
	CY62136VSL-55ZSI			Industrial
70	CY62136VLL-70ZSI			Industrial
	CY62136VLL-70ZSE			Automotive
	CY62136VSL-70ZSI			Industrial

Package Diagrams

DIMENSION IN MM (INCH)
MAX
MIN.

44-pin TSOP II ZS44

TOP VIEW

BOTTOM VIEW

PIN 1 I.D.

22 ... 1

11.938 (0.470)
11.735 (0.462)

23 ... 44

10.262 (0.404)
10.058 (0.396)

EJECTOR PIN

0.800 BSC
(0.0315)

0.400 (0.016)
0.300 (0.012)

BASE PLANE

18.517 (0.729)
18.313 (0.721)

0.10 (.004)

SEATING
PLANE

1.194 (0.047)
0.991 (0.039)

0.150 (0.0059)
0.050 (0.0020)

10.262 (0.404)
10.058 (0.396)

0°-5°

0.210 (0.0083)
0.120 (0.0047)

0.597 (0.0235)
0.406 (0.0160)
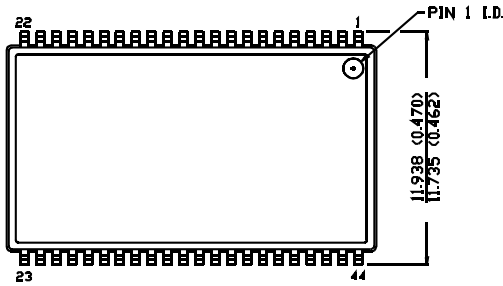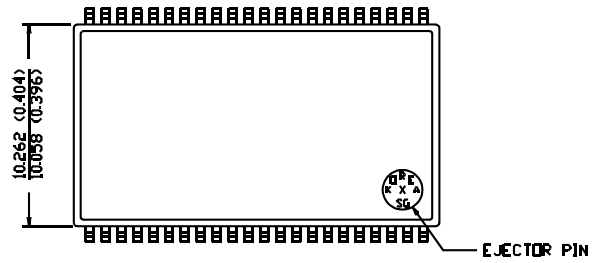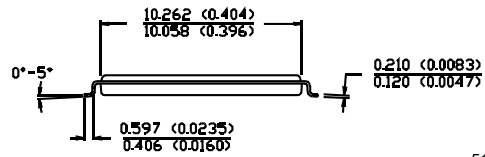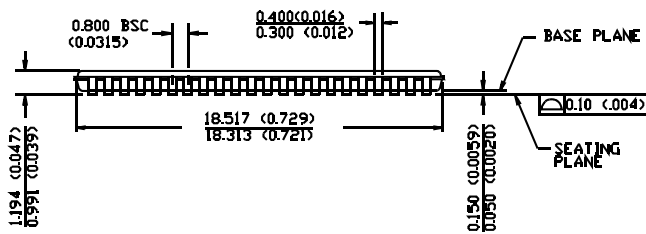
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Document History Page

Document Title: CY62136V MoBL® 2-Mbit (128K x 16) Static RAM
Document Number: 38-05087

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107347	05/25/01	SZV	Changed from Spec #: 38-00728 to 38-05087
*A	116509	09/04/02	GBI	Added footnote 1 Added SL power bin Deleted fBGA package; replacement fBGA package available in CY62136CV30
*B	269729	See ECN	SYT	Added Automotive Information for 70-ns Speed Bin. Added Footnotes # 3 and # 6. Corrected Typo in Electrical Characteristics for I_{CC}(Max)-55 ns from 15 to 20 mA. Added SL row for I_{SB2} in the Electrical Characteristics table. Changed Package Name from Z44 to ZS44. Replaced 'Z' with 'ZS' in the Ordering Code.