

**FEATURES**

- 3.3 W Into 4Ω from 5.5V power supply at THD+N=10% (Typ).
- 2.0 W Into 8Ω from 5.5V power supply at THD+N=10% (Typ).
- 2.5V~5.5V power supply.
- Low shutdown current.
- Low quiescent current.
- Minimum external components.
- No output filter required for inductive loads.
- Output pin short-circuit protection and automatic recovery.  
(short to output pin, short to GND, short to VDD)
- Low noise during turn-on and turn-off transitions.
- **Easy upgrade Class AB (LY8891) to Class D (Pin to Pin Replace).**
- Lead free and green package available. (RoHS Compliant)
- Space Saving Package  
- 8-pin MSOP package.

**GENERAL DESCRIPTION**

The LY8006 is a high efficiency, 3.3 W mono class D audio power amplifier. It is a low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplify design.

The LY8006 is designed to meet of portable electronic devices. The LY8006 is a single 5.5V power supply, it is capable of driving 4Ω speaker load at a continuous average output of 3.3 W with 10% THD+N.

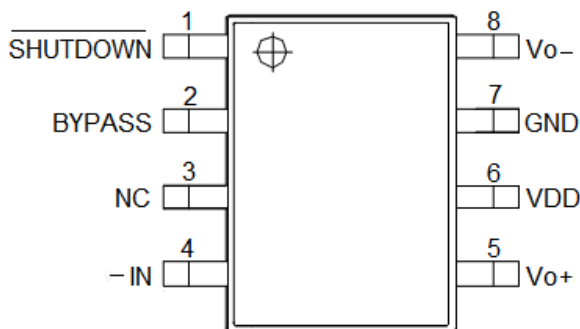
In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the LY8006. The gain of the LY8006 is externally configurable which allows independent gain control from multiple sources by summing the signals. Output pin short circuit ( short to output pin, short to ground and short to VDD ) protection prevent the device from damage during fault conditions.

**APPLICATION**

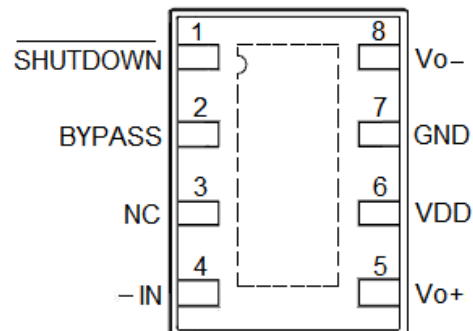
- Portable electronic devices
- Mobile Phones
- PDAs

**PIN CONFIGURATION**

**LY8006 MSOP8 pin configuration (TOP VIEW)**



**LY8006 DFN8 pin configuration (TOP VIEW)**





#### PIN DESCRIPTION

SYMBOL	Pin No.	DESCRIPTION
	MSOP	
SHUTDOWN	1	Shutdown the device. (when <b>LOW</b> level is shutdown mode).
BYPASS	2	Bypass pin
NC	3	No Internal connection
-IN	4	Negative input
Vo-	5	Positive BTL output
V <sub>DD</sub>	6	Power supply
GND	7	Ground
Vo+	8	Negative BTL output

#### ORDERING INFORMATION

Ordering Code	Speaker Channels	Pin/ Package	Output Power (THD+N=10%)	Input Type	Output Type
LY8006UL	Mono	MSOP8	3.3W/4Ω @5.5V_BTL 2.7W/4Ω @5.0V_BTL 2.0W/8Ω @5.5V_BTL 1.6W/8Ω @5.0V_BTL	SE	BTL

**APPLICATION CIRCUIT**

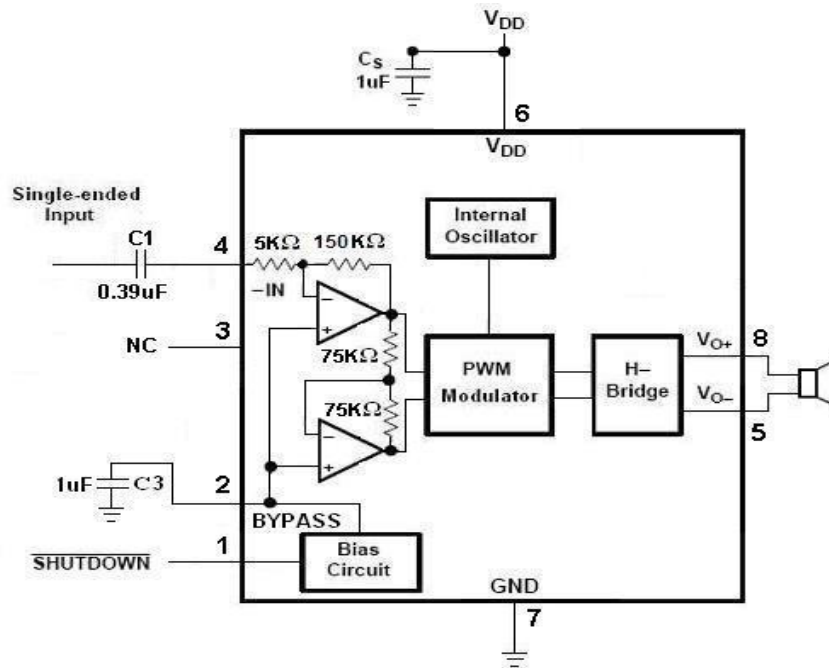


Figure 1. Application Schematic With Single-Ended Input Configuration  
 Single-End Input With Pre-Amplifier Gain =  $(150\text{ K}\Omega / 5\text{ K}\Omega) * 2 = 60$

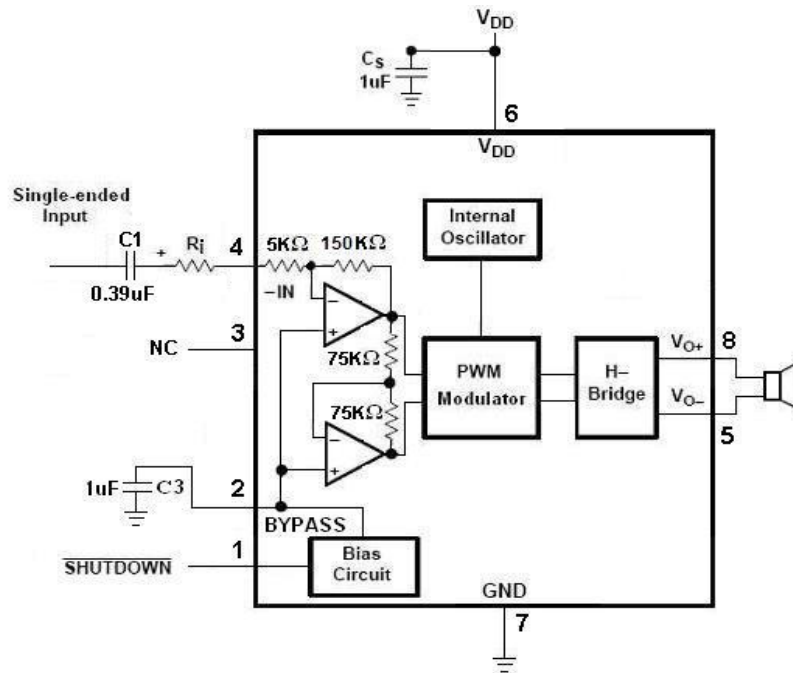


Figure 2. Application Schematic With Single-Ended Input Configuration  
 Single-End Input With Pre-Amplifier Gain =  $[150\text{ K}\Omega / (5\text{ K}\Omega + R_i)] * 2$

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	6.0	V
Operating Temperature	T <sub>A</sub>	-40 to 85 ( I grade)	°C
Input Voltage	V <sub>I</sub>	-0.3V to V <sub>DD</sub> +0.3V	V
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	Internally Limited	W
ESD Susceptibility	V <sub>ESD</sub>	2000	V
Junction Temperature	T <sub>JMAX</sub>	150	°C
Soldering Temperature (under 10 sec)	T <sub>SOLDER</sub>	260	°C

**ELECTRICAL CHARACTERISTICS** (T<sub>A</sub> = 25°C, Unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>2</sup>	MAX.	UNIT
Supply voltage	V <sub>DD</sub>		2.5	-	5.5	V
High-level input voltage	V <sub>IH</sub>	Shutdown	1.3	-	V <sub>DD</sub>	
Low-level input voltage	V <sub>IL</sub>	Shutdown	0	-	0.35	
Output offset voltage (measured differentially)	V <sub>OS</sub>	V <sub>I</sub> = 0 V, A <sub>v</sub> = 2 V/V, V <sub>DD</sub> = 2.5 V to 5.5 V	-	-	25	mV
Power supply rejection ratio	PSRR	V <sub>DD</sub> = 5.0 V, R <sub>L</sub> = 4Ω, Inputs = GND, A <sub>v</sub> = 2, V <sub>pp</sub> = 200mV, C <sub>s</sub> = Delete. f = 217Hz	-	-55	--	dB
Quiescent Current	I <sub>Q</sub>	V <sub>DD</sub> = 5.5V, No Load	-	3.5	4.5	mA
		V <sub>DD</sub> = 3.6V, No Load	-	3.0	-	
		V <sub>DD</sub> = 2.5V, No Load	-	2.5	3.2	
Shutdown Current	I <sub>SD</sub>	V <sub>SHUTDOWN</sub> ≤ 0.5V, V <sub>DD</sub> = 2.5V to 5.5V	-	0.1	2.0	μA
Total Gain (*)		V <sub>DD</sub> = 2.5V to 5.5V R <sub>L</sub> = 8Ω	[300KΩ / (5KΩ + R <sub>i</sub> )] x 2			V/V

(\*1) The audio amplifier's gain is determined by :

$$\text{Pre-Amplifier Gain} = [150\text{K}\Omega / (5\text{K}\Omega + R_i)] \times 2$$

$$\text{Total Gain} = \{ [150\text{K}\Omega / (5\text{K}\Omega + R_i)] \times 2 \} \times 2$$

where R<sub>i</sub> is the external serial resistance at the input pin.

(\*2) Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C



#### **OPERATING CHARACTERISTICS** (TA = 25°C, Unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>2</sup>	MAX.	UNIT	
Out Power	Po	THD+N= 10%, f = 1 kHz, RL= 4Ω	VDD=5.5V	-	3.3	-	W
			VDD=5.0V	-	2.75	-	
			VDD=3.6V	-	1.4	-	
			VDD=2.5V	-	0.6	-	
		THD+N= 1%, f = 1 kHz, RL= 4Ω	VDD=5.5V	-	2.6	-	
			VDD=5.0V	-	2.15	-	
			VDD=3.6V	-	1.1	-	
		THD+N= 10%, f = 1 kHz, RL= 8Ω	VDD=5.5V	-	2.0	-	
			VDD=5.0V	-	1.6	-	
			VDD=3.6V	-	0.8	-	
		THD+N= 1%, f = 1 kHz, RL= 8Ω	VDD=5.5V	-	1.6	-	
			VDD=5.0V	-	1.3	-	
VDD=3.6V	-		0.7	-			
Signal-to-noise ratio	SNR	RL = 48Ω, Input=GND, 1.0W=0dB	VDD=5.0V	-	88	-	dB
Output voltage noise	Vn	Input=GND, RL=4Ω, Av=2 f = 20 Hz to 20 kHz,	VDD=5.0V	-	79.4	-	uVRMS
Frequency	Fc	VDD = 2.5V~5.5V		-	250	-	kHz
Start-up time from shutdown	Zi	VDD = 5.0V	Cbypass = 1.0μF	-	360	-	ms
			Cbypass = 0.47μF	-	180	-	
			Cbypass = 0.33μF	-	144	-	
			Cbypass = 0.22μF	-	104	-	
			Cbypass = 0.1μF	-	48	-	
			Cbypass =None	-	32	-	
		VDD = 3.7V	Cbypass = 1.0μF	-	250	-	
			Cbypass = 0.47μF	-	128	-	
			Cbypass = 0.33μF	-	108	-	
			Cbypass = 0.22μF	-	72	-	
Cbypass = 0.1μF	-	48	-				
Cbypass =None	-	32	-				

(\*2)Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at VCC = VCC(TYP.) and TA = 25°C



#### TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3  
Total Harmonic Distortion + Noise vs Output Power (4Ω)

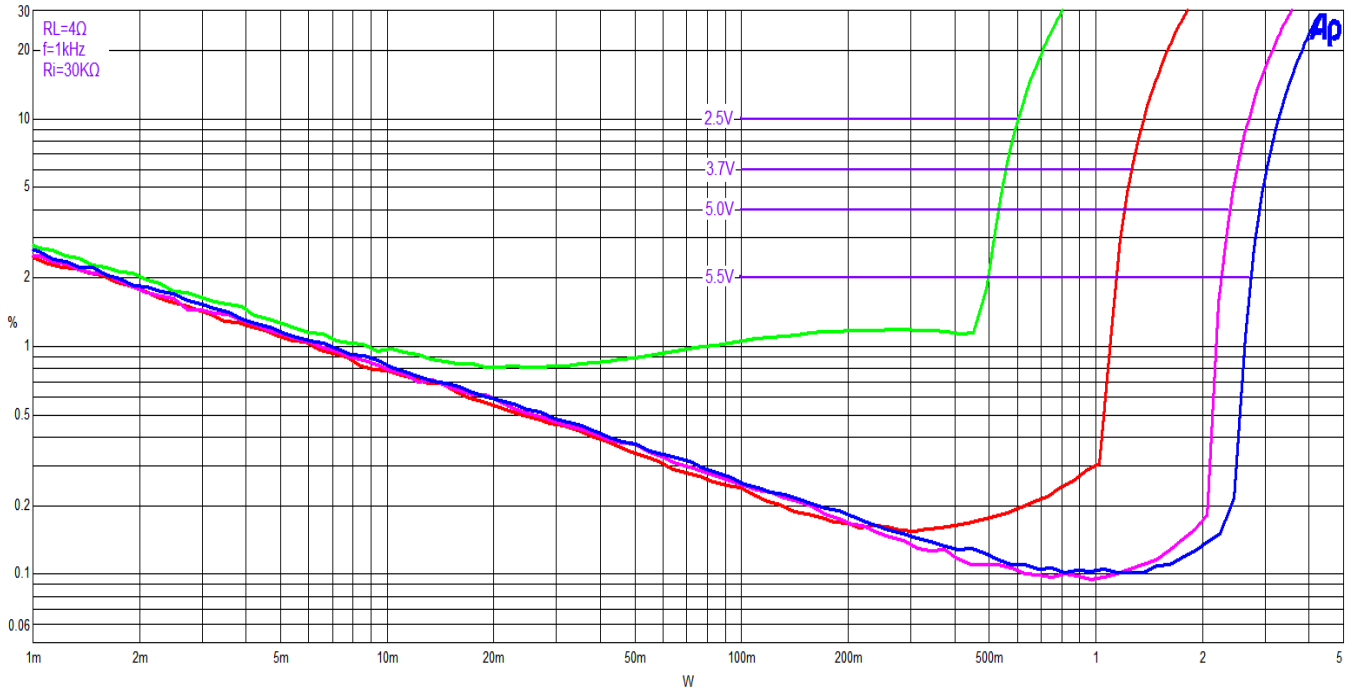


Figure 4  
Total Harmonic Distortion + Noise vs Output Power (8Ω)

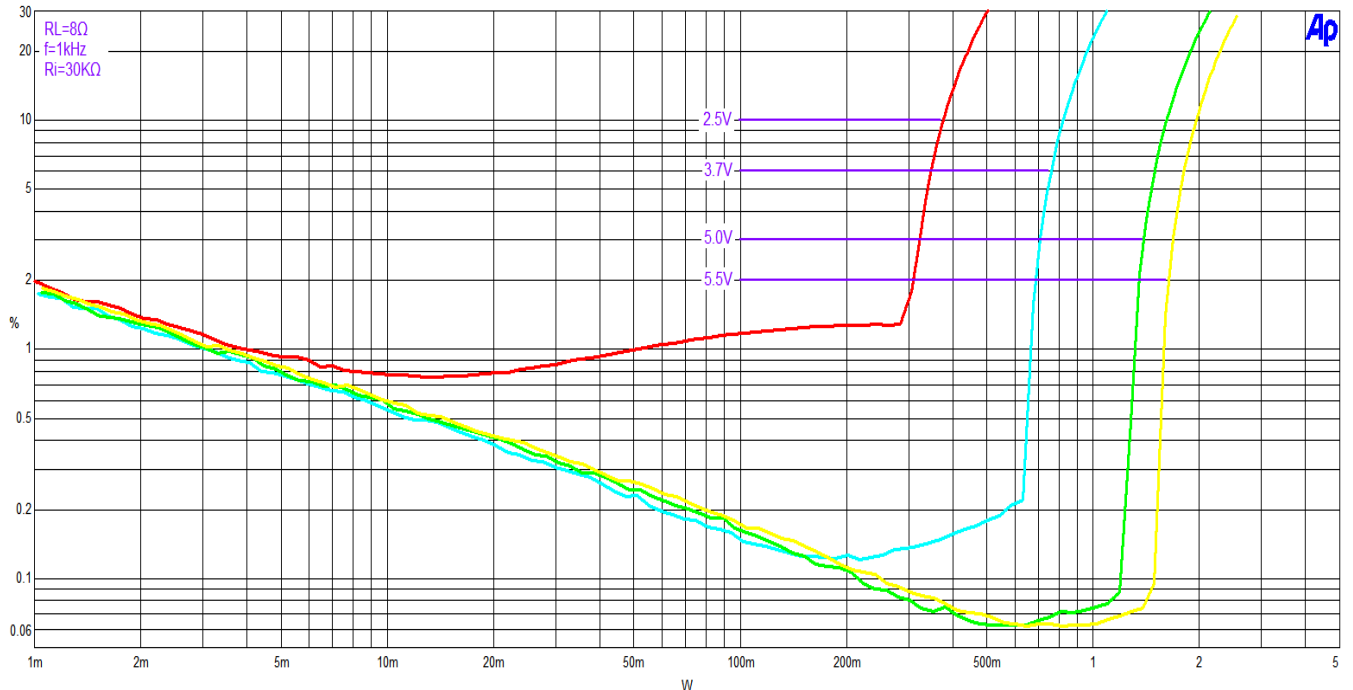


Figure 5  
Noise Level

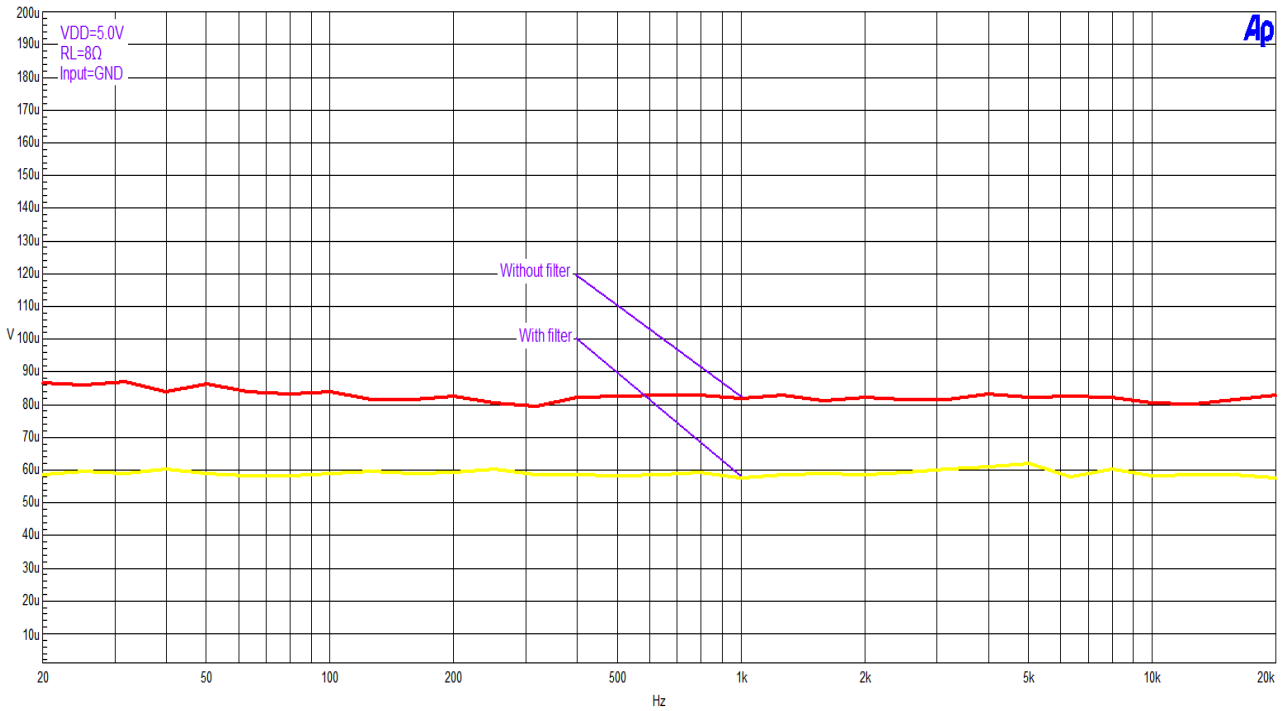
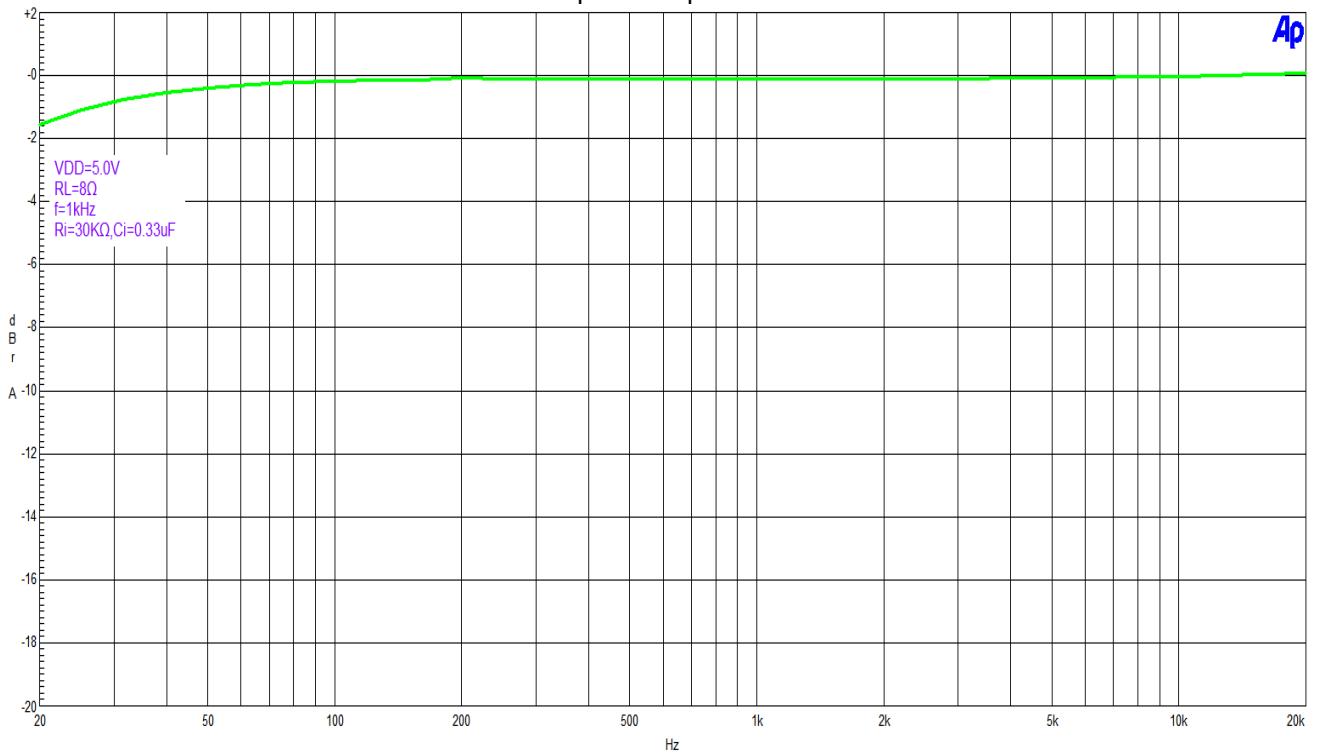
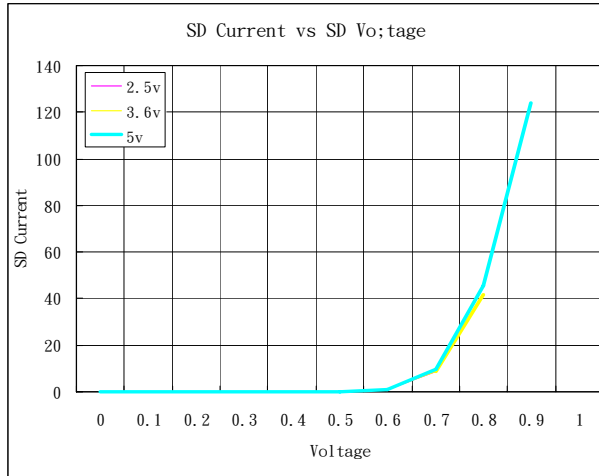


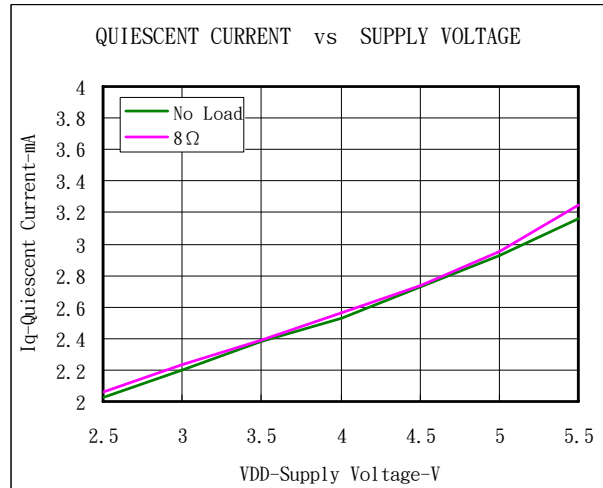
Figure 6  
Freq. vs. Response



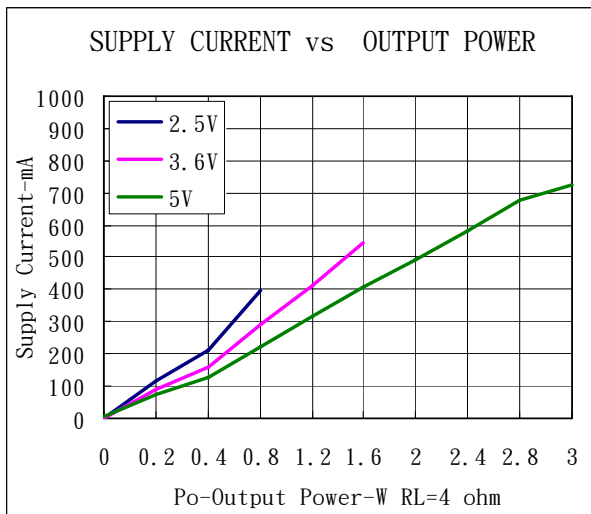
SD Current vs SD Voltage



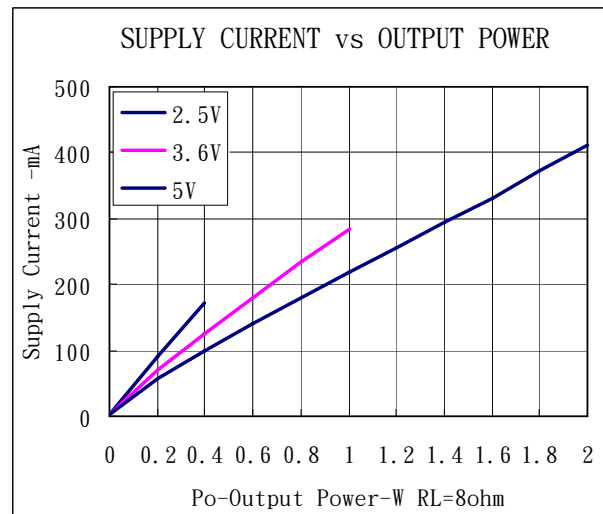
Quiescent vs Supply voltage



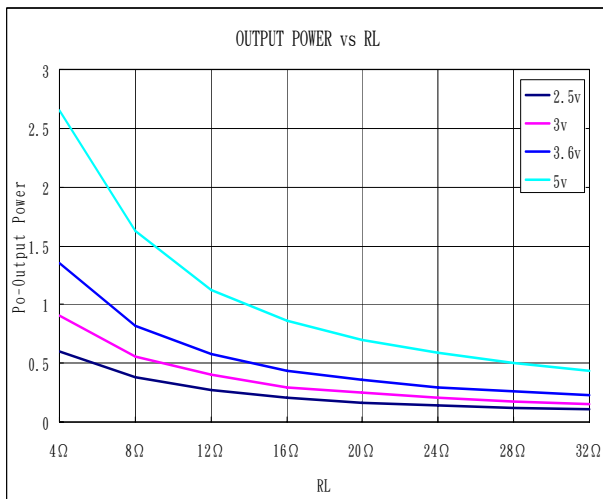
Supply Current vs Output Power (RL=4Ω)



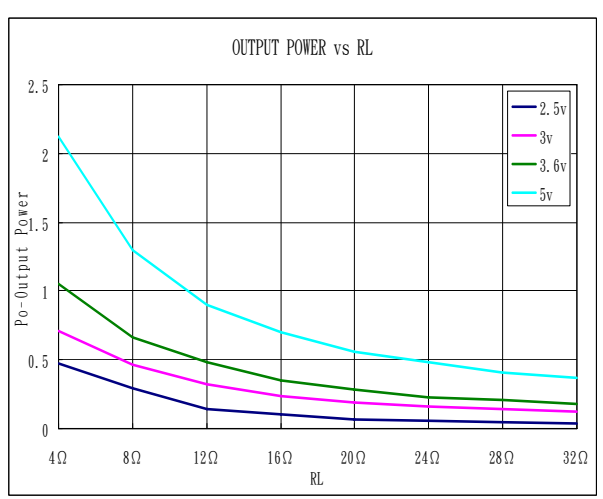
Supply Current vs Output Power (RL=8Ω)



Load Resistance vs Output Power (THD+N=10%)

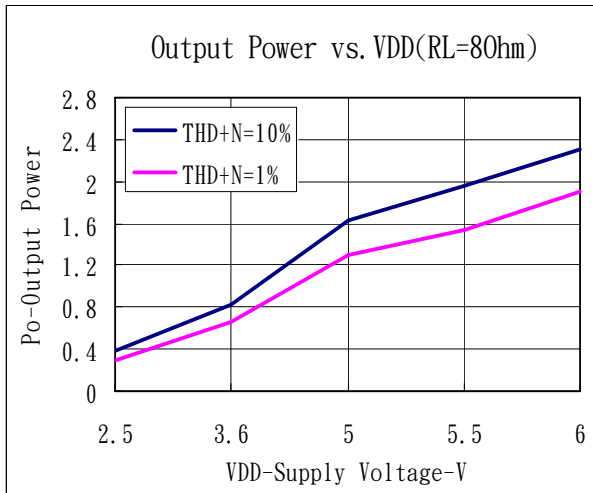


Load Resistance vs Output Power (THD+N=1%)

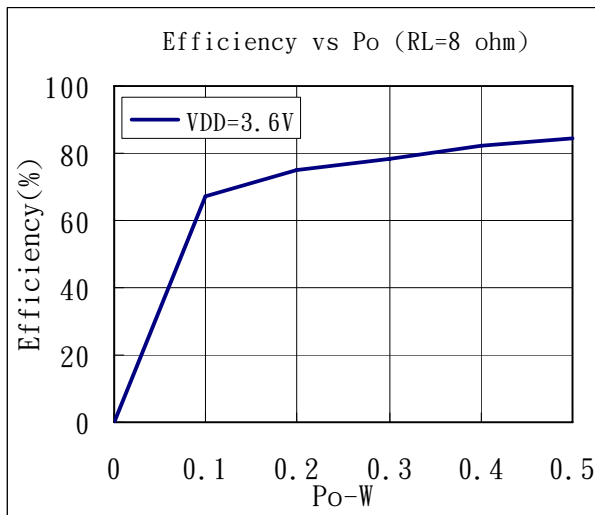




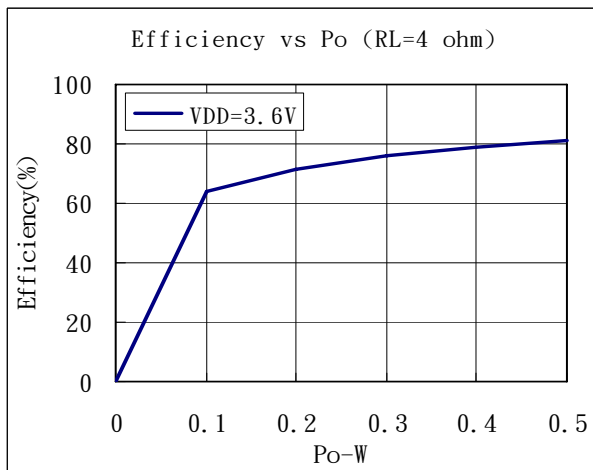
Output Power vs VDD (RL=80Ohm)



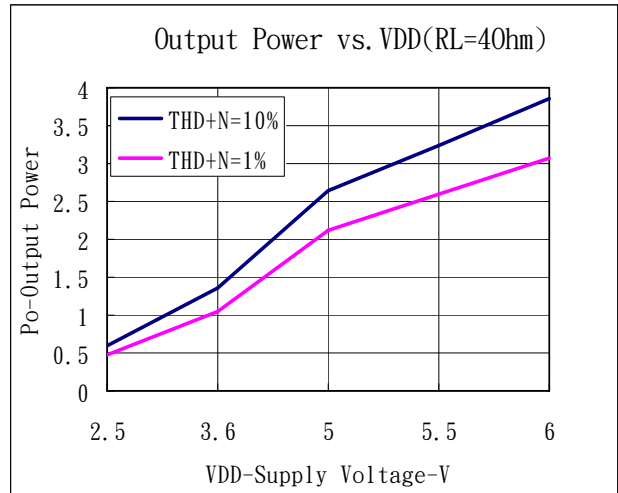
Efficiency and Output Power (80Ohm) 3.6V



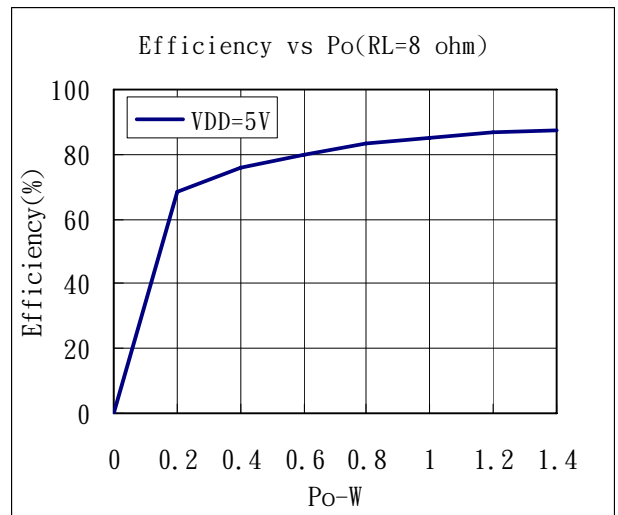
Efficiency and Output Power (40Ohm) 3.6V



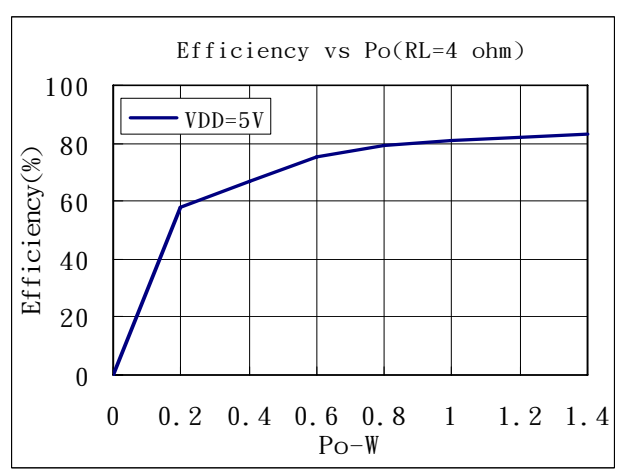
Output Power vs VDD (RL=40Ohm)

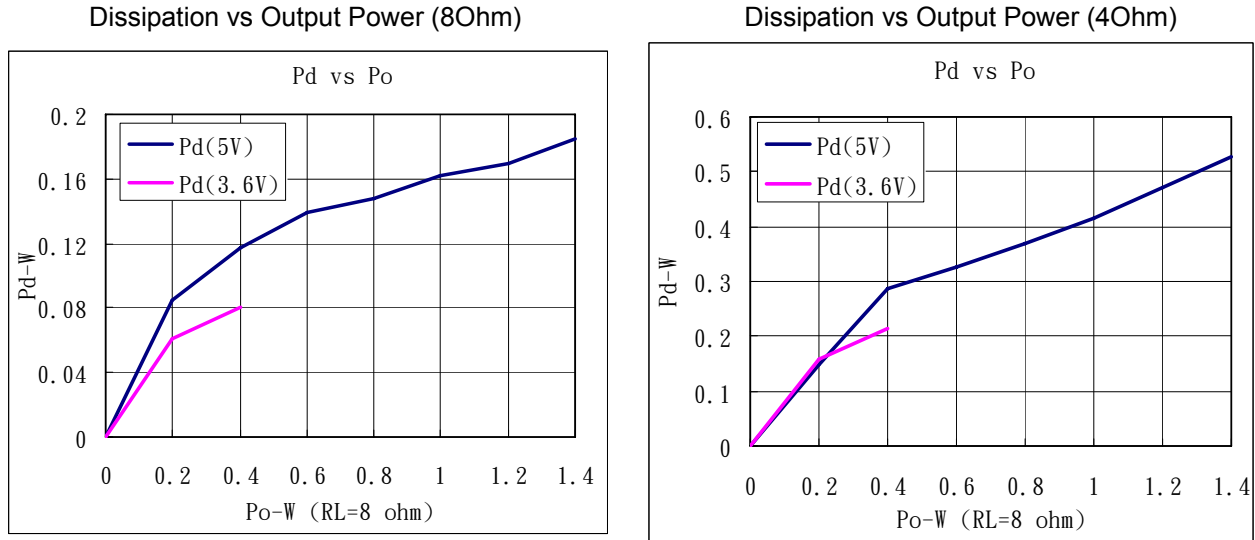


Efficiency and Output Power (80Ohm) 5.0V

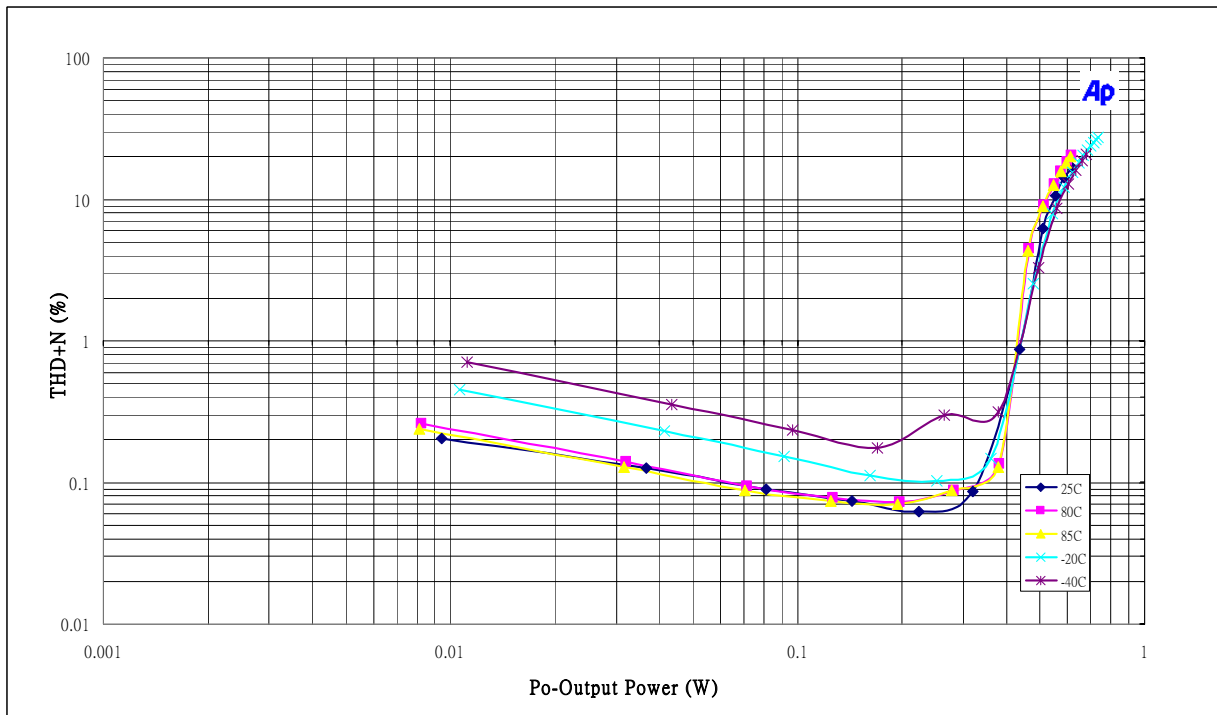


Efficiency and Output Power (40Ohm) 5.0V

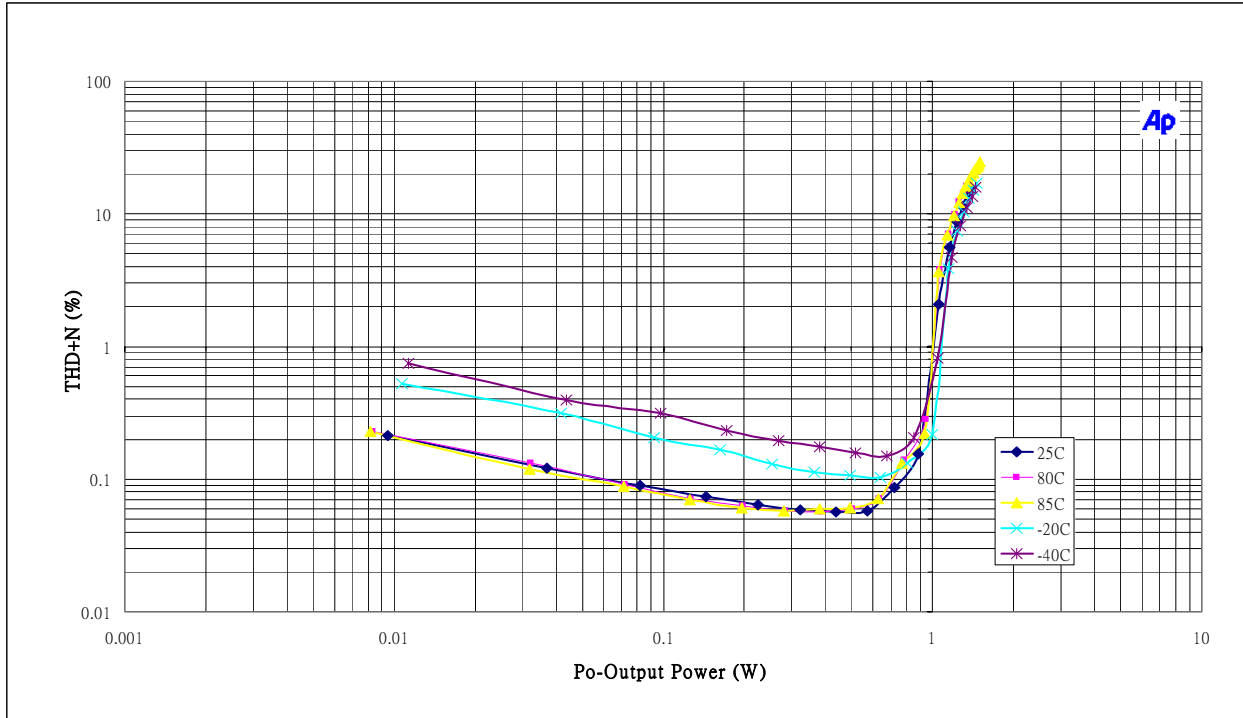




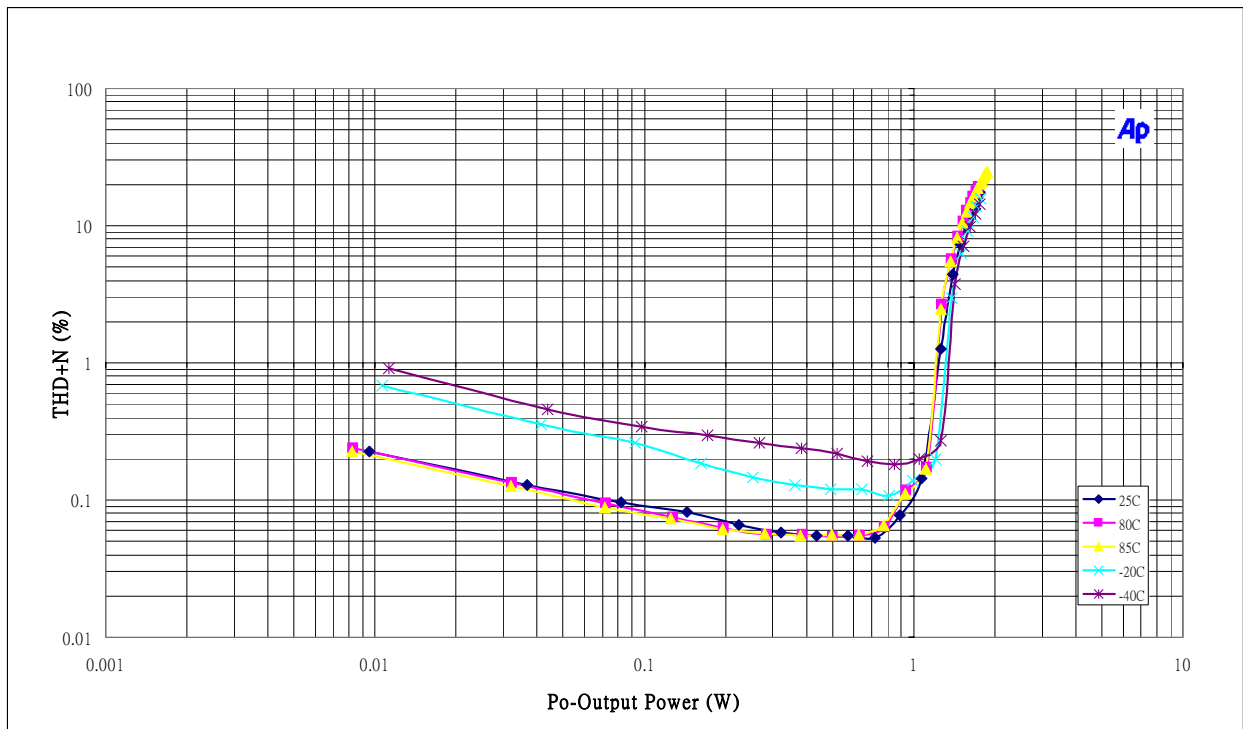
**Figure 7**  
**THD+N & Output Power vs Temperature (VDD=3V, RL=8Ω)**



**Figure 8**  
THD+N & Output Power vs Temperature (VDD=4.5V, RL=8Ω)



**Figure 9**  
THD+N & Output Power vs Temperature (VDD=5.0V, RL=8Ω)



## **APPLICATION INFORMATION**

### **Input Resistors (Ri) and Gain**

The input resistors (Ri) set the gain of the amplifier according to the equation.

$$\text{Pre-Amplifier Gain} = (R_f / R_i) \times 2 = [150\text{K}\Omega / (5\text{K}\Omega + R_i)] \times 2$$

$$\text{Total Gain} = [(R_f / R_i) \times 2] \times 2 = \{[150\text{K}\Omega / (5\text{K}\Omega + R_i)] \times 2\} \times 2$$

$$A_{VD} = 20 \times \log \{2 \times [(R_f / R_i) \times 2]\}$$

The resistor matching is very important in the amplifiers. Balance of the output on the reference voltage depends on matched ratio of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance.

Resistor arrays with 1% matching can be used with a tolerance greater than 1%. Place the input resistors very close to the LY8006 to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the LY8006 to operate at its best,

### **For example**

**Table 1. Typical Total Gain and Avd Values**

Rf (KΩ)	150	150	150	150	150	150
Ri (KΩ)	300	150	100	75	50	37.5
Pre AMP. Gain	1	2	3	4	6	8
Total Gain	2	4	6	8	12	16
Avd (db)	6.02	12.04	15.56	18.06	21.58	24.08

### **Input Capacitors (Ci)**

The LY8006 using a single-ended source, So the input coupling capacitors are required. The input capacitors and input resistors form a high-pass filter with the corner frequency( $f_c$ ), determined in the equation.

$$f_c = 1 / (2 \pi R_i C_i)$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Equation is reconfigured to solve for the input coupling capacitance.

$$C_i = 1 / (2 \pi R_i f_c)$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of  $\pm 10\%$  or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

**For example**

In the table 2 shows the external components. Rin in connect with Cin to create a high-pass filter.

**Table 2. Typical Component Values**

Reference	Description	Note
Ri	150KΩ	1% tolerance resistors
Ci	0.22uF	80%/–20%

$$C_i = 1 / ( 2 \pi R_i f_c )$$

$$C_i = 1 / ( 2 \pi * 150K\Omega * 4.8Hz ) = 0.221\mu F \cdot \text{Use } 0.22\mu F$$

**Two Single-Ended Input Signals**

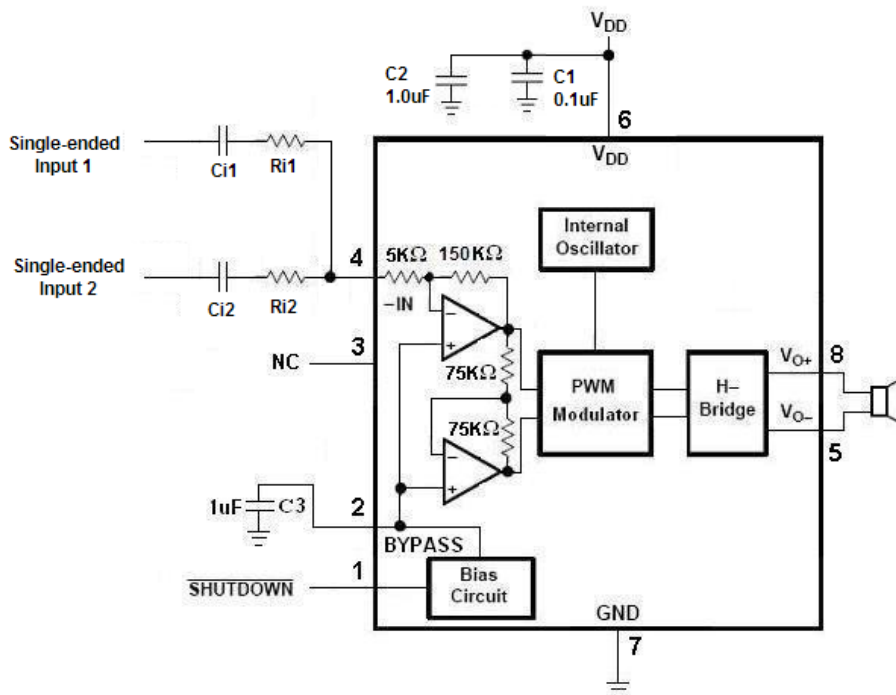
Two resistors and two capacitors are needed for summing single-ended input signals. The gain and corner frequencies ( $f_{c1}$  and  $f_{c2}$ ) for each input source can be set independently.

$$\text{Pre-Amplifier Gain } 1 = [ 150K\Omega / ( 5K\Omega + R_{i1} ) ] \times 2$$

$$\text{Pre-Amplifier Gain } 2 = [ 150K\Omega / ( 5K\Omega + R_{i2} ) ] \times 2$$

$$C_{i1} = 1 / ( 2 \pi R_{i1} f_{c1} )$$

$$C_{i2} = 1 / ( 2 \pi R_{i2} f_{c2} )$$


**Figure 10. Application Schematic With Two Single-Ended Inputs Configuration**

**PCB Layout**

All the external components must place very close to the LY8006. The input resistors need to be very close to the LY8006 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the LY8006. Then place the decoupling capacitor Cs, close to the LY8006 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Making the high current traces going to VDD, GND, Vo+ and Vo- pins of the LY8006 should be as wide as possible to minimize trace resistance. If these traces are too thin, the LY8006's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

**LY8006UL Demo Board Artwork**

**Demo Board Application Circuit**

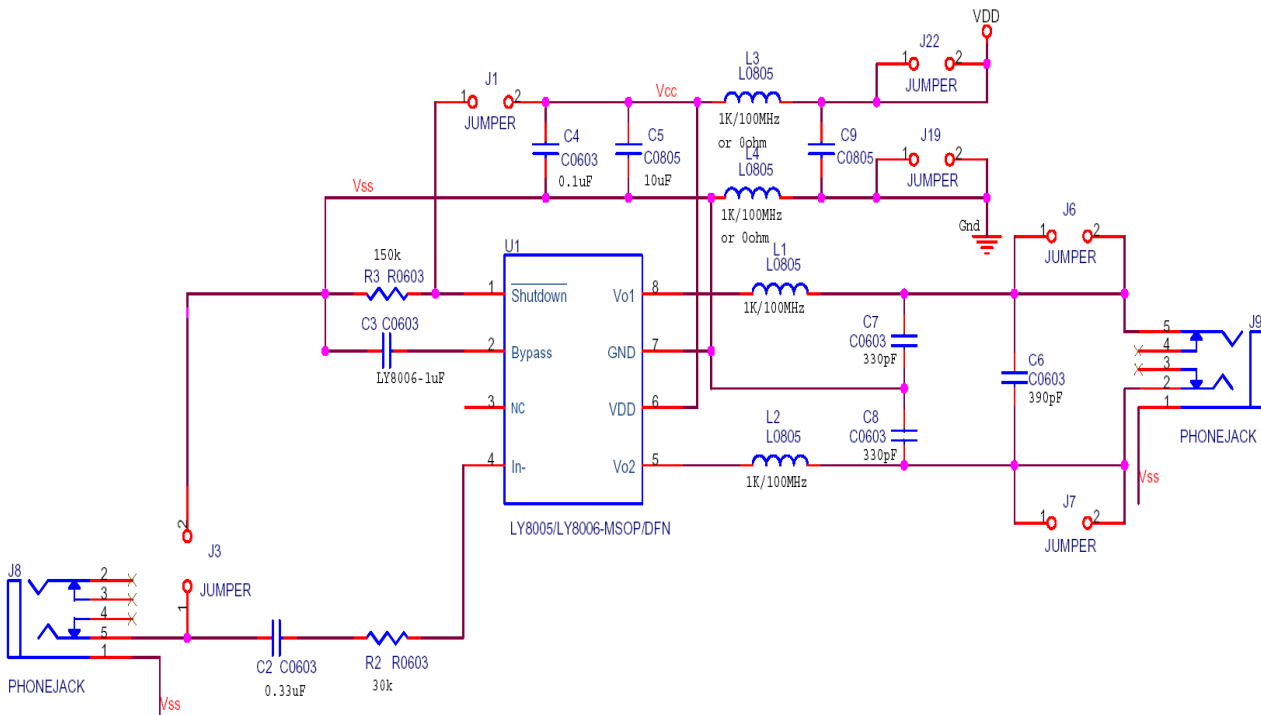


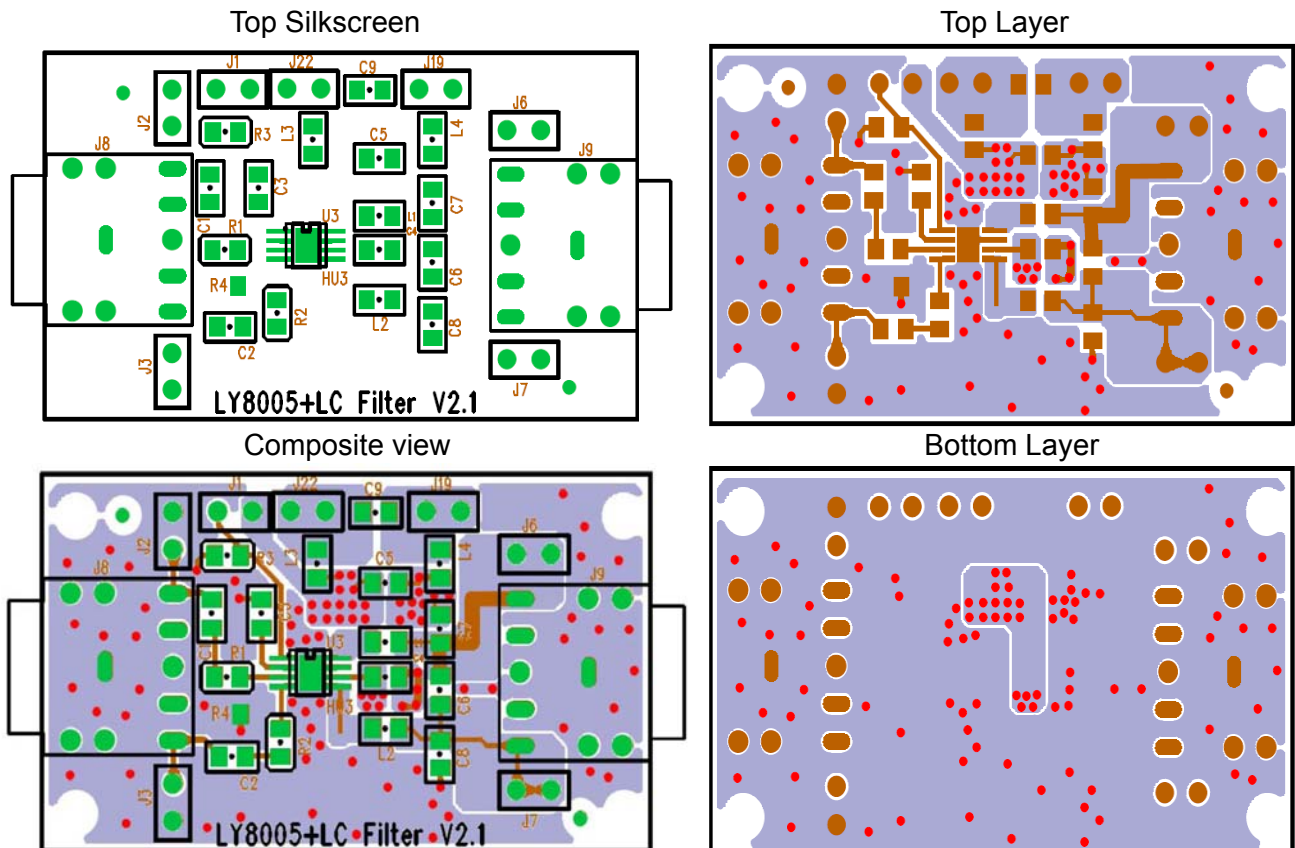
Figure 11. Demo Board Application Circuit

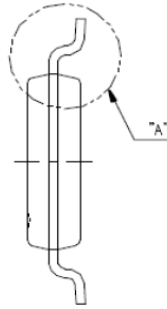
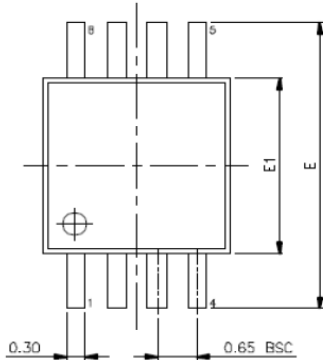
#### Demo Board BOM List

*LY8006 V2.1 BOM List*

No.	Description	Reference	Note
1	Resistor, 30KΩ	R2	1/16W,1%
2	Resistor, 150KΩ	R3	1/16W,1%
3	Capacitor, 330pF(Option)	C7,C8	80%/-20%, nonpolarized
4	Capacitor, 390pF(Option)	C6	80%/-20%, nonpolarized
5	Capacitor, 0.1uF	C4	80%/-20%, nonpolarized
6	Capacitor, 0.33uF	C2	80%/-20%, nonpolarized
7	Capacitor, 1.0uF	C3	80%/-20%, nonpolarized
8	Capacitor, 10.0uF	C5	80%/-20%, 6.3 V
9	Chip Bead 1KΩ/100MHz(Option)	L1,L2,L3,L4	1000Ω(1KΩ)±25%/100MHz
10	IC	U1	LY8006UL, MSOP8
11	1*2 Pin Header	J1	J1, Open → shutdown Mode

#### Demo Board Artwork



**PACKAGE OUTLINE DIMENSION**
**8 Pin MSOP Package Outline Dimension**


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.10
A1	0.00	–	0.15
A2	0.75	0.85	0.95
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
$\theta^\circ$	0	–	8

UNIT : MM

**NOTES:**

1. JEDEC OUTLINE : MO-187 AA
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION '0.22' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE '0.22' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE  $\square$ .

