Synchronous Buck PWM Controller

Features

- **Simple Single-Loop Control Design**
  - **Voltage-Mode PWM Control**
- **Fast Transient Response**
  - **Full 0–100% Duty Ratio**
- **Excellent Output Voltage Regulation**
  - **0.8V Internal Reference**
  - **± 1% Over Line Voltage and Temperature**
- **Over Current Fault Monitor**
  - **Uses Upper MOSFETs $R_{DS(ON)}$**
- **Converter Can Source and Sink Current**
- **Small Converter Size**
  - **200kHz Free-Running Oscillator**
  - **Programmable from 70kHz to 800kHz**
- **14-Lead SOIC Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APW7062B is a voltage mode and synchronous PWM controller which drives dual N-Channel MOSFETs. It integrates the control, monitoring, and protection functions into a single package, provides one controlled power outputs with under-voltage and over-current protection.

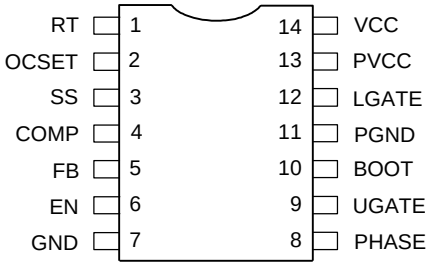
APW7062B provides excellent regulation for output load variation. An internal 0.8V temperature-compensated reference voltage is designed to meet the requirement of low output voltage applications. It includes a 200kHz free-running triangle-wave oscillator that is adjustable from 70kHz to 800kHz.

The power-on-reset (POR) circuit monitors the VCC, EN, and OCSET input voltage to start-up or shutdown the IC. The over-current protection (OCP) monitors the output current by using the voltage drop across the upper MOSFET's $R_{DS(ON)}$, eliminating the need for a current sensing resistor. The under-voltage protection (UVP) monitors the voltage of the FB pin for short-circuit protection. The over-current protection trip cycle the soft-start function until the fault events be removed. Under-voltage protection will shutdown the IC directly.

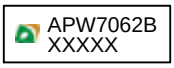
Applications

- **Graphic Cards**
- **DDR Memory Power Supply**
- **DDR Memory Termination Voltage**
- **Low-Voltage Distributed Power Supplies**

Pin Configuration



Ordering and Marking Information

APW7062B □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-14 Operating Ambient Temperature Range C : 0 to 70 °C Handling Code TR : Tape & Reel Assembly Material L : Lead Free Device G : Halogen and Lead Free Device
APW7062B K : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC to GND	30	V
V_{BOOT}	BOOT to GND	30	V
V_{PHASE}	PHASE to GND	30	V
	Operating Junction Temperature	0~150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1 : Stresses above those listed in bsolute Maximum Ratings may cause permanent damage to the device.

Electrical Characteristics

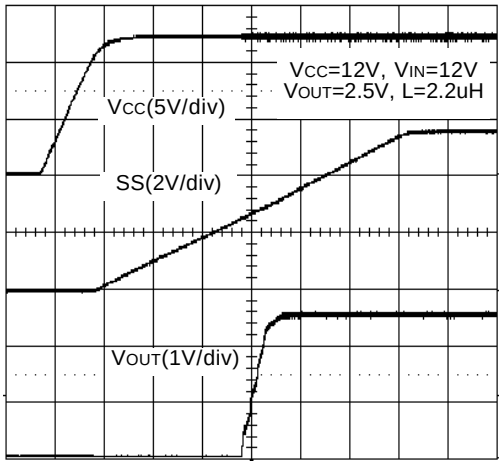
Symbol	Parameter	Test Conditions	APW7062B			Unit
			Min.	Typ.	Max.	
V_{CC} SUPPLY CURRENT						
I_{CC}	Nominal Supply	EN=V_{CC}; UGATE and LGATE Open	-	2	-	mA
	Shutdown Supply	EN=0V	-	250	350	μA
POWER-ON-RESET						
	Rising V_{CC} Threshold	V_{OCSET}=4.5V_{DC}	-	-	10.4	V
	Falling V_{CC} Threshold	V_{OCSET}=4.5V_{DC}	8.8	-	-	V
	Enable-Input Threshold Voltage	V_{OCSET}=4.5V_{DC}	0.8	-	2.0	V
	Rising V_{OCSET} Threshold		-	1.27	-	V
OSCILLATOR						
	Free Running Frequency	R_T=OPEN, V_{CC}=12	170	200	230	kHz
	Total Variation	6kΩ < RT to GND < 200kΩ	-15	-	+15	%
ΔV_{OSC}	Ramp Amplitude	R_T=OPEN	-	1.9	-	VP-P
REFERENCE VOLTAGE ACCURACY						
ΔV_{REF}	Reference Voltage Tolerance		-1	-	+1	%
V_{REF}	PWM Error Amplifier		-	0.80	-	V

Electrical Characteristics (Cont.)

Symbol	Parameter	Test Conditions	APW7062B			Unit
			Min.	Typ.	Max.	
GATE DRIVERS						
I_{UGATE}	Upper Gate Source	V_{BOOT}=12V, V_{UGATE}=6V	650	800	-	mA
R_{UGATE}	Upper Gate Sink	I_{LGATE}=0.3A	-	4	7	Ω
I_{LGATE}	Lower Gate Source	P_{VCC}=12V, V_{LGATE}=6V	550	700	-	mA
R_{LGATE}	Lower Gate Sink	I_{LGATE}=0.3A	-	4	7	Ω
T_D	Dead Time	V_{OUT}=2.5V, I_{OUT}=1A, R_T=OPEN	-	50	-	ns
PROTECTION						
	FB Under Voltage		-	50	-	%
I_{OCSET}	OCSET Current Source	V_{OCSET}=4.5V_{DC}	170	200	230	µA
I_{SS}	Soft-Start Current		8	10	12	µA

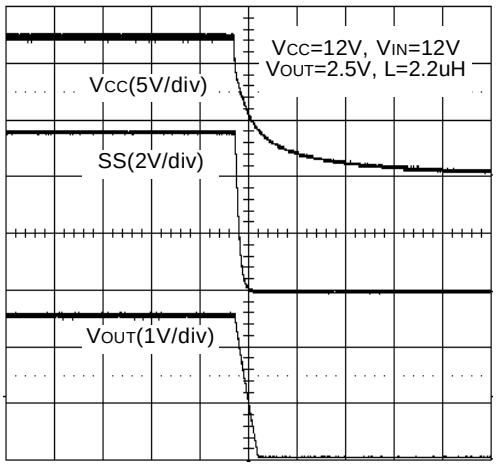
Typical Operating Characteristics

Power Up



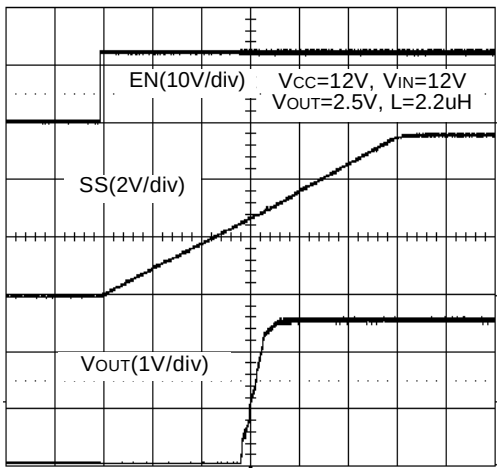
Time(10μs/div)

Power Down



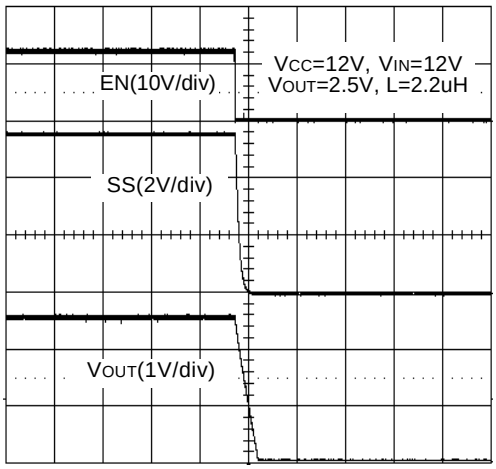
Time(10μs/div)

Enable (EN = VCC)



Time(10μs/div)

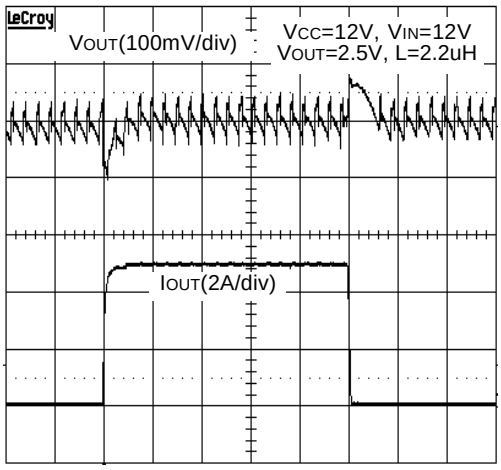
Shutdown (EN=GND)



Time(2μs/div)

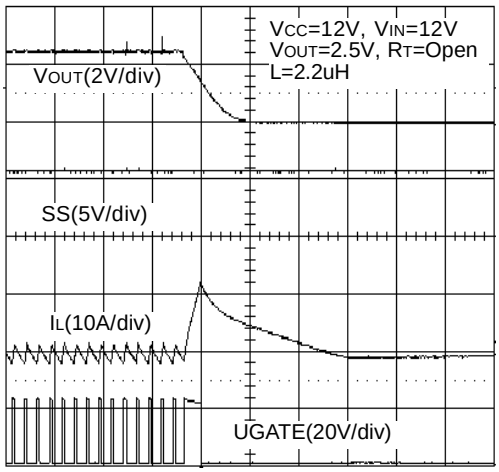
Typical Operating Characteristics (Cont.)

Load Transient Response



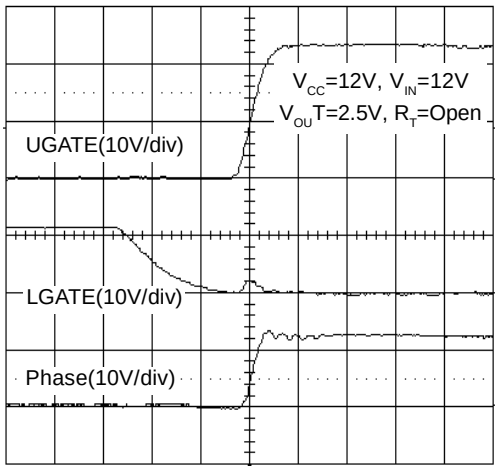
Time(20μs/div)

Under Voltage Protection



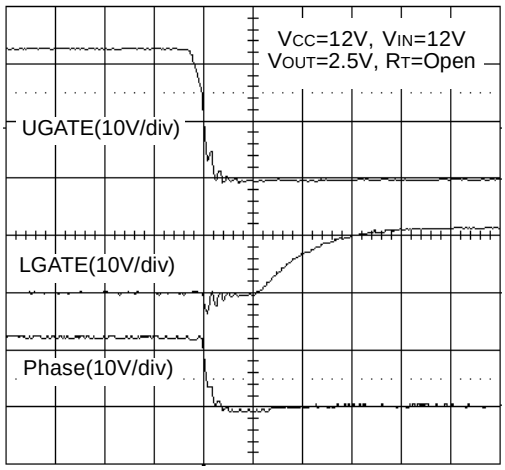
Time(20μs/div)

UGATE Rising



Time(50μs/div)

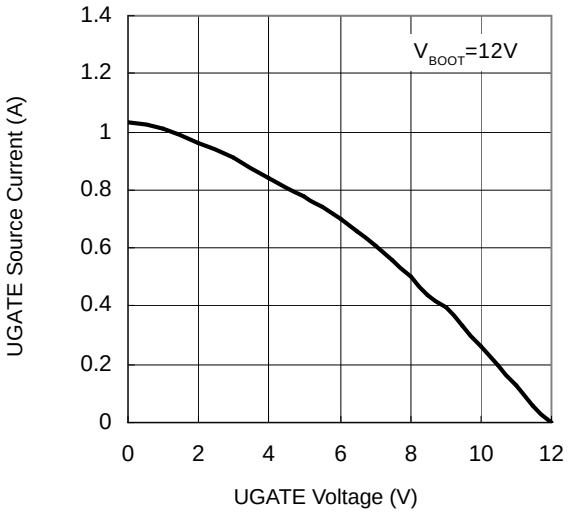
UGATE Falling



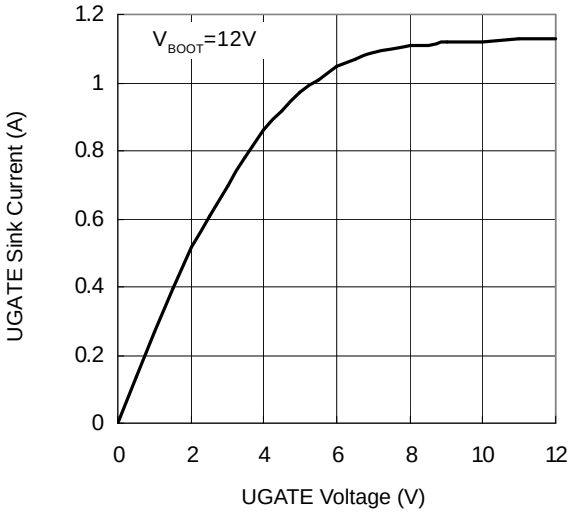
Time(50μs/div)

Typical Operating Characteristics (Cont.)

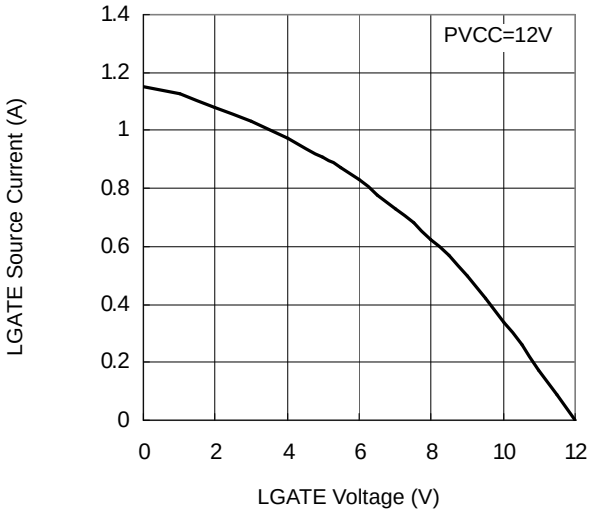
UGATE Source Current vs. UGATE Voltage



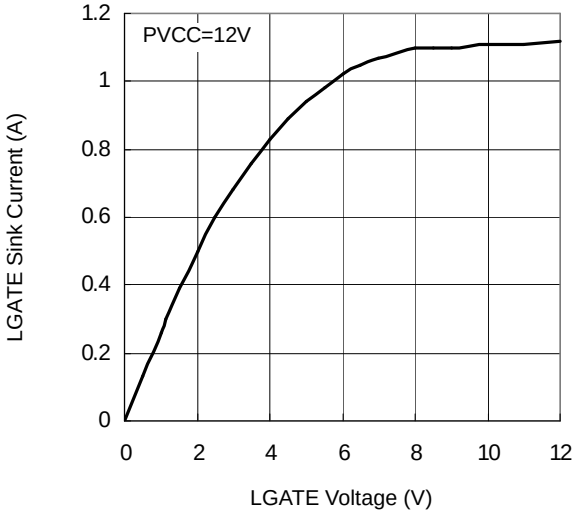
UGATE Sink Current vs. UGATE Voltage



LGATE Source Current vs. LGATE Voltage

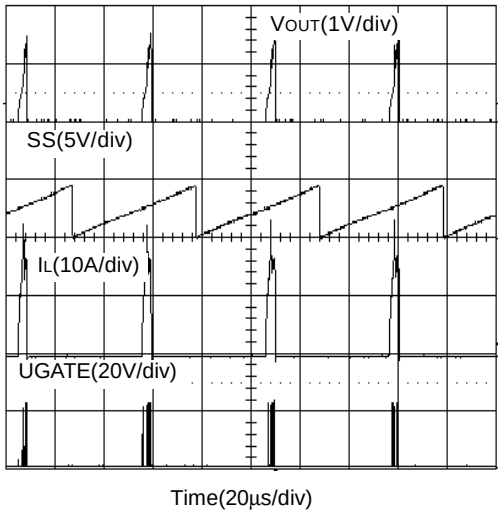


LGATE Sink Current vs. LGATE Voltage



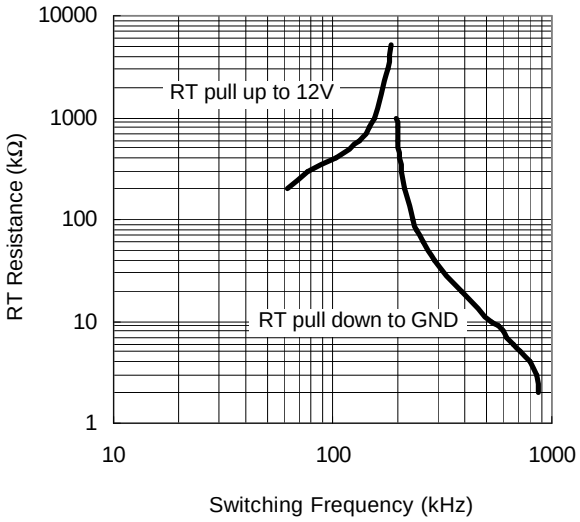
Typical Operating Characteristics (Cont.)

Over Current Protection

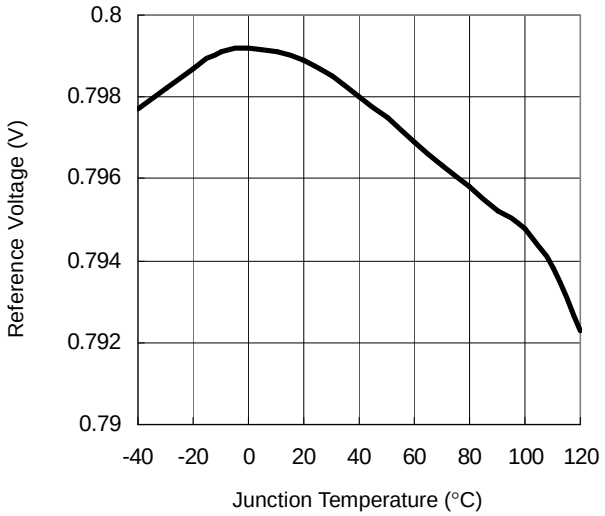


V_{CC}=12V, V_{IN}=12V, V_{OUT}=2.5V,
R_{OCEST}=1KΩ, R_T=Open, $R_{DS(ON)}$=14mΩ,
I_{OUT}=16.3A, L=2.2uH, L_{OUT}=16.3A

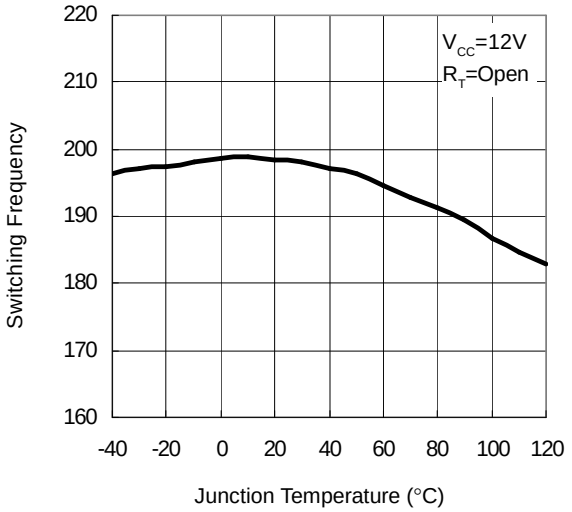
RT Resistance vs. Switching Frequency



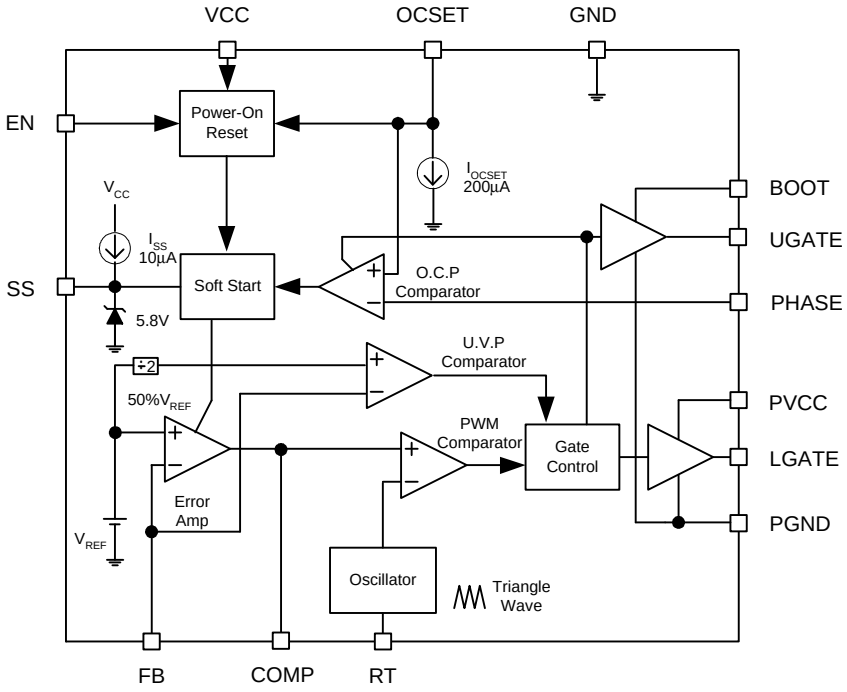
Reference Voltage vs. Junction Temperature



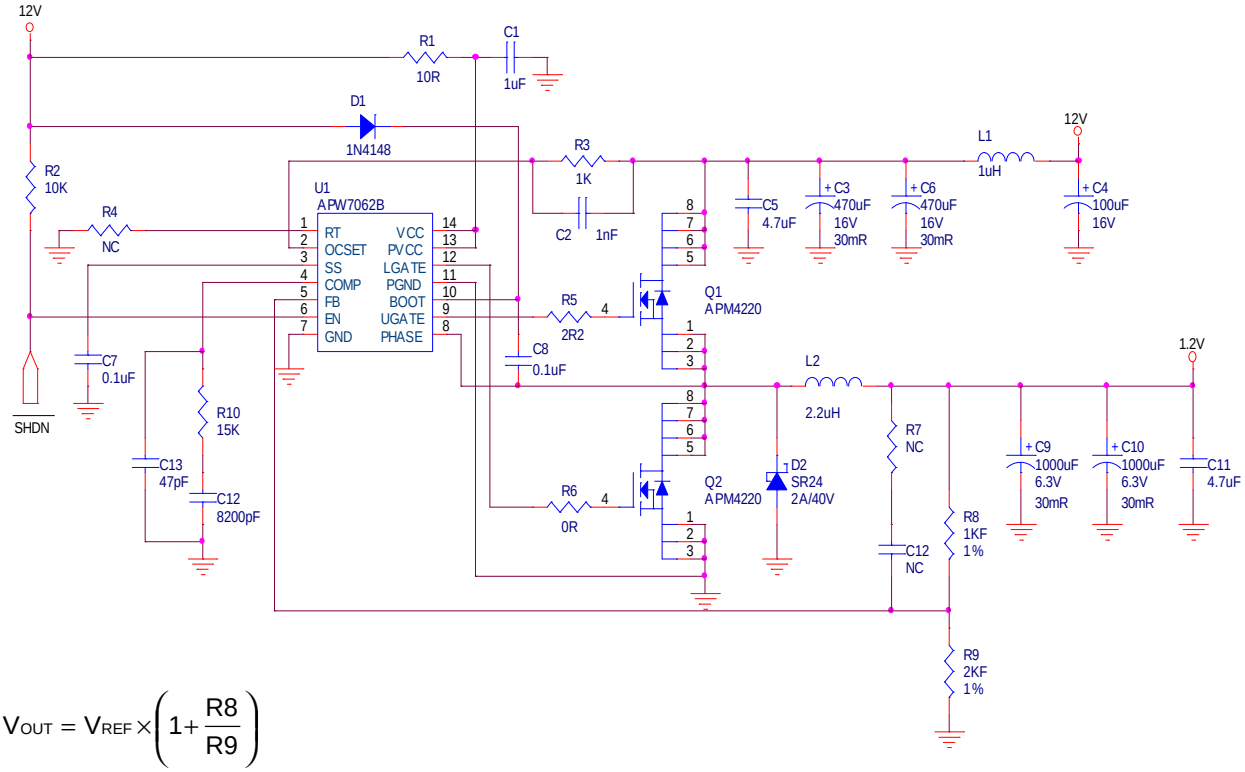
Switching Frequency vs. Junction Temperature



Block Diagram



Typical Application Circuit



$$V_{OUT} = V_{REF} \times \left(1 + \frac{R8}{R9}\right)$$

Function Pin Description

RT (Pin1)

This pin can adjust the switching frequency. Connect a resistor from the RT to the GND for increasing the switching frequency:

$$F_S = 200kHz + \frac{4.15\times10^6}{RT}$$

(RT to GND, F_S = 200kHz to 400kHz)

Conversely, connect a resistor from the RT to the V_{CC} for decreasing the switching frequency:

$$F_S = 200kHz - \frac{3.51\times10^7}{RT}$$

(RT to V_{CC}, F_S = 200kHz to 75kHz)

OCSET (Pin2)

This pin serves two functions: a shutdown control and the setting of over current-limit threshold. Pulling this pin below 1.27V will shutdown the controller, forcing the UGATE and LGATE signals to be at 0V.

A resistor (R_{ocset}) connected between this pin and the drain of the high side MOSFET will determine the over current limit. An internal 200µA current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the high side MOSFET. The threshold of the over current limit is therefore given by:

$$I_{PEAK} = \frac{I_{OCSET}(200uA)\times R_{OCSET}}{R_{DS(ON)}}$$

To avoid the noise interference from switching transient, a delay time is designed in the OCP comparator.

The over-current protection is active only when the high side MOSFET is turned on longer than 300ns.

SS (Pin3)

Connect a capacitor from the pin to the GND to set the soft-start interval of the converter. An internal 10µA current source charges this capacitor to 5.8V. The SS voltage clamps the error amplifier output, and Figure1 shows the soft-start interval. At t1, the SS voltage reaches the valley of the oscillator's triangle wave. The PWM comparator starts to generate a PWM signal to control logic, and the output is rising rapidly. Until the output is in regulation at t2, the clamp on the COMP is released. This method provides a rapid and controlled output voltage rise.

When over-current protection occurs, the VOUT is shutdown, and re-soft-start again, if the over current condition still exists in soft-start, the VOUT is shutdowned again. After the SS reaches 4.5V, the SS is discharged to zero. The soft-start is recurring until the over current condition is eliminated.

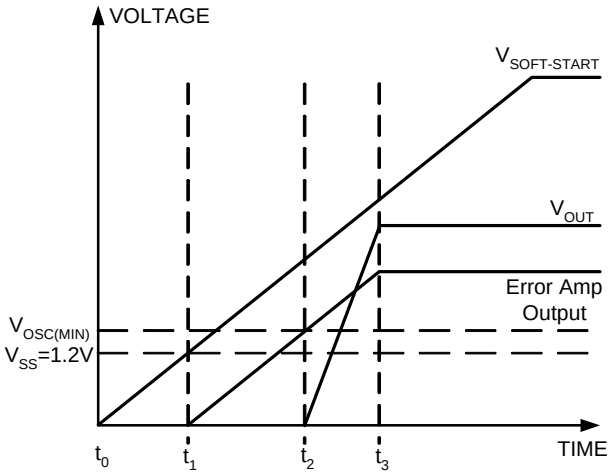


Figure 1. Soft-Start Interval

$$t_2 = \frac{C_{SS}}{I_{SS}}\times(V_{OSC(MIN)} + t_1)$$

$$t_{SoftStart} = t_3 - t_2 = \frac{C_{SS}}{I_{SS}}\times\frac{V_{OUT\,SteadyState}}{V_{IN}}\times\Delta V_{OSC}$$

Where :

t_1=1.2V
C_{SS} = Soft-Start Capacitor
I_{SS} = Soft-Start Current = 10µA
$V_{OSC(MIN)}$ = Bottom of Oscillator = 1.35V
V_{IN} = Input Voltage
ΔV_{osc} = Peak to Peak Oscillator Voltage = 1.9V
ΔV_{OUT}SteadyState = Steady State Output Voltage

Function Pin Description (Cont.)

COMP (Pin4)

This pin is the output of the error amplifier. Add an external resistor and capacitor network to provide the loop compensation for the PWM converter (see Application Information).

FB (Pin5)

FB pin is the inverter input of the error amplifier and it receives the feedback voltage from an external resis-tive divider across the output (V_{OUT}). The output voltage is determined by:

$$V_{OUT} = 0.8V \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

Where R_{OUT} is the resistor connected from the V_{OUT} to the FB and R_{GND} is the resistor connected from the FB to the GND.
If the FB voltage is under 50% V_{REF} because of the short circuit or other influence , it will cause the under-voltage protection, and the device is shutdowned. Remove the error condition and restart the VCC voltage or pull the EN from low to high once, the device can be enabled again.

EN (Pin6)

Pull the pin higher than 2V to enable the device, and pull the pin lower than 0.8V to shutdown the device. In shutdown, the SS is discharged and the UGATE and LGATE pins are held low. The EN pin is the open-collector, and it will not be floating.

GND (Pin7)

Signal ground for the IC.

PHASE (Pin8)

This pin is connected to the source of the high-side MOSFET and is used to monitor the voltage drop across the high-side MOSFET for over-current protection.

UGATE (Pin9)

Connect the pin to external MOSFET, and provides the gate drive for the upper MOSFET.

BOOT (Pin 10)

This pin provides the supply voltage to the high side MOSFET driver. For driving logic level N-channel MOSEFT, a bootstrap circuit can be used to create a suitable driver's supply.

PGND (Pin11)

Power ground for the gate diver. Connect the lower MOSFET source to this pin.

LGATE (Pin 12)

Connect the pin to the external MOSFET, and provides the gate drive signal for the lower MOSFET.

PVCC (Pin13)

This pin provides a supply voltage for the lower gate drive, connect it to the VCC pin in common use.

VCC (Pin14)

This pin provides a supply voltage for the device. When the VCC is above the rising threshold 10.4V, the device is turned on; conversely, when the VCC is below the falling threshold, the device is turned off.

Application Information

Component Selection Guidelines

Output Capacitor Selection

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore, select high performance low ESR capacitors that are intended for switching regulator applications. In some applications, multiple capacitors have to be paralled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

For high frequency decoupling, a ceramic capacitor between 0.1µF to 1µF can be connected between the V_{CC} and the ground pin.

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

where Fs is the switching frequency of the regulator.

There is a tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Compensation

The output LC filter introduces a double pole, which contributes with –40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between the COMP pin and the ground should be added. The simplest loop compensation network is shown in Figure 5.

The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR + 1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

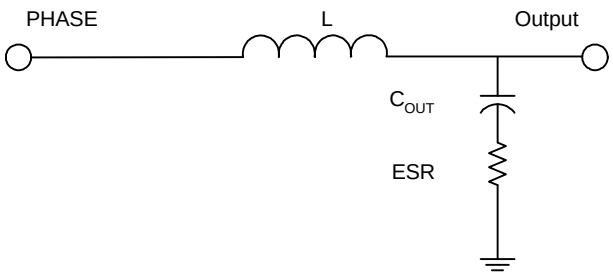


Figure 2. The Output LC Filter

Application Information (Cont.)

Compensation (Cont.)

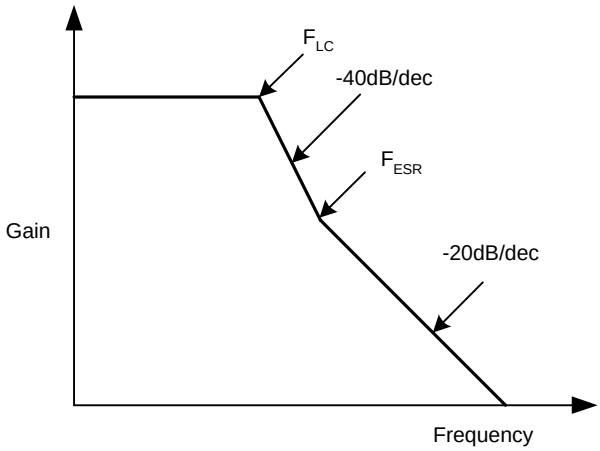


Figure 3. The Output LC Filter Gain & Frequency

The PWM modulator is shown in Figure 4. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

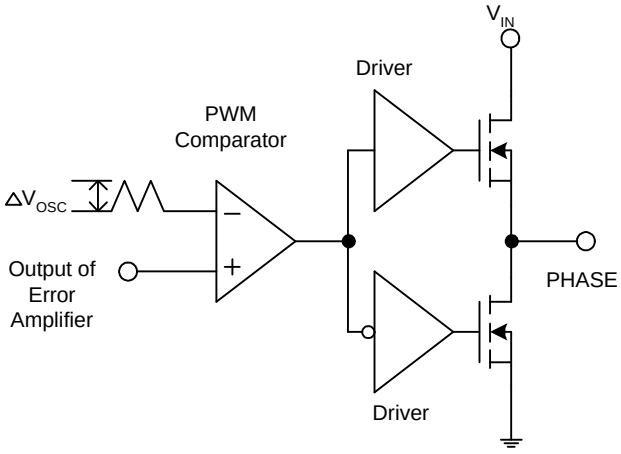


Figure 4. The PWM Modulator

The compensation circuit is shown in Figure 5. R3 and C1 introduce a zero and C2 introduces a pole to reduce the switching noise. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = gm \times Zo = gm \times \left[\left(R_3 + \frac{1}{sC_1}\right) // \frac{1}{sC_2}\right]$$

$$= gm \times \frac{(R_3 sC_1 + 1)}{s \times \left(s + \frac{C_1 + C_2}{R_3 \times C_1 \times C_2}\right)}$$

The poles and zero of the compensation network are:

$$F_P = \frac{1}{2 \times \pi \times R_3 \times \frac{C_1 \times C_2}{C_1 + C_2}}$$

$$F_Z = \frac{1}{2 \times \pi \times R_3 \times C_1}$$

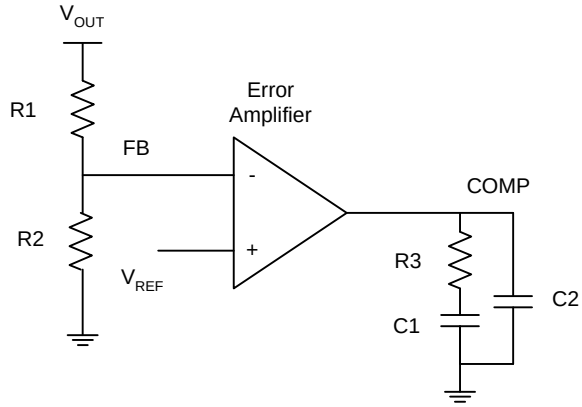


Figure 5. Compensation Network

Application Information (Cont.)

Compensation (Cont.)

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times \frac{R2}{R1+R2} \times GAIN_{AMP}$$

Figure 6 shows the converter gain and the following guidelines will help to design the compensation network.

1.Select the desired zero crossover frequency F_O:

$(1/5 \sim 1/10) \times F_S > F_O > F_Z$

Use the following equation to calculate R_3:

$$R_3 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_{ESR}}{F_{LC}^2} \times \frac{R_1+R_2}{R_2} \times \frac{F_O}{gm}$$

Where:

gm=900μA/V

2.Place the zero F_Z before the LC filter double poles F_{LC}:

$F_Z = 0.75 \times F_{LC}$

Calculate the C_1 by the equation:

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times F_{LC} \times 0.75}$$

3. Set the pole at the half the switching frequency:

$F_P = 0.5 \times F_S$

Calculate the C_2 by the equation:

$$C_2 = \frac{C_1}{\pi \times R_3 \times C_1 \times F_S - 1}$$

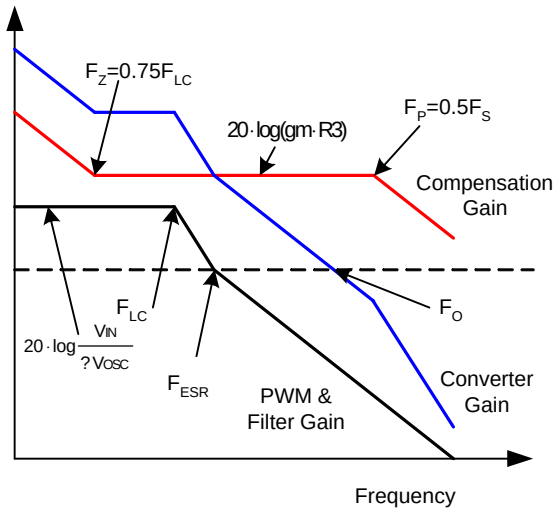


Figure 6. Converter Gain & Frequency

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement.The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following :

$P_{UPPER} = I_{out}^2 (1+ TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_S$

$P_{LOWER} = I_{out}^2(1+ TC)(R_{DS(ON)})(1-D)$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{sw} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET include an additional transition loss. The switching internal, t_{sw}, is the function of the reverse transfer capacitance C_{RSS}. Figure 7 illustrates the switching waveform internal of the MOSFET.

The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedances should be minimized by using short and wide printed circuit traces. Signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. Figure 8 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. There fore keep traces to these nodes as short as possible.
- The ground return of C_{IN} must return to the combine C_{OUT} (-) terminal.
- Capacitor C_{BOOT} should be connected as close to the BOOT and PHASE pins as possible.

Application Information (Cont.)

Layout Consideration (Cont.)

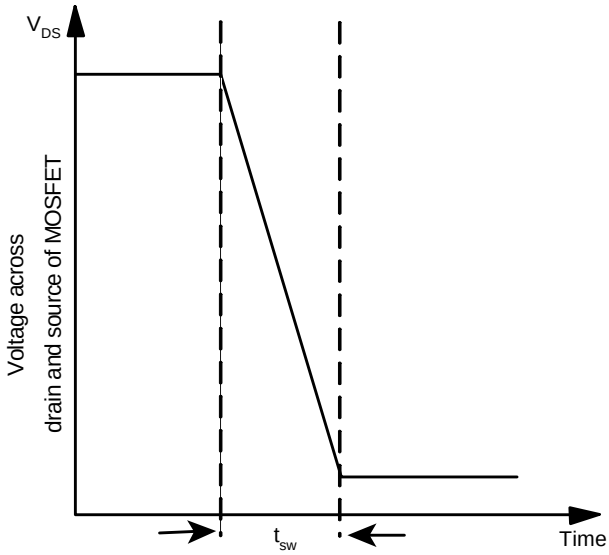


Figure 7. Switching waveform across MOSFET

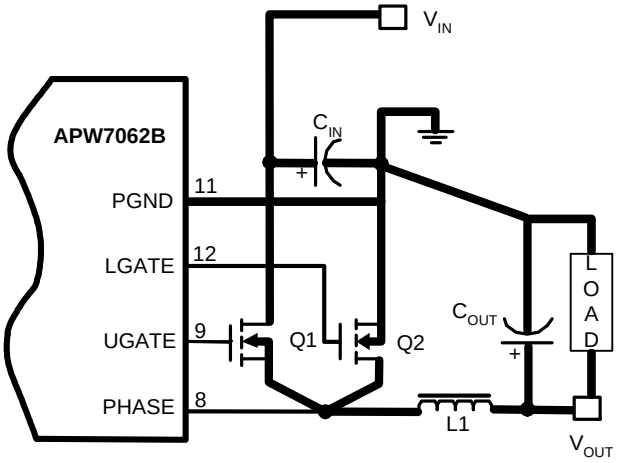
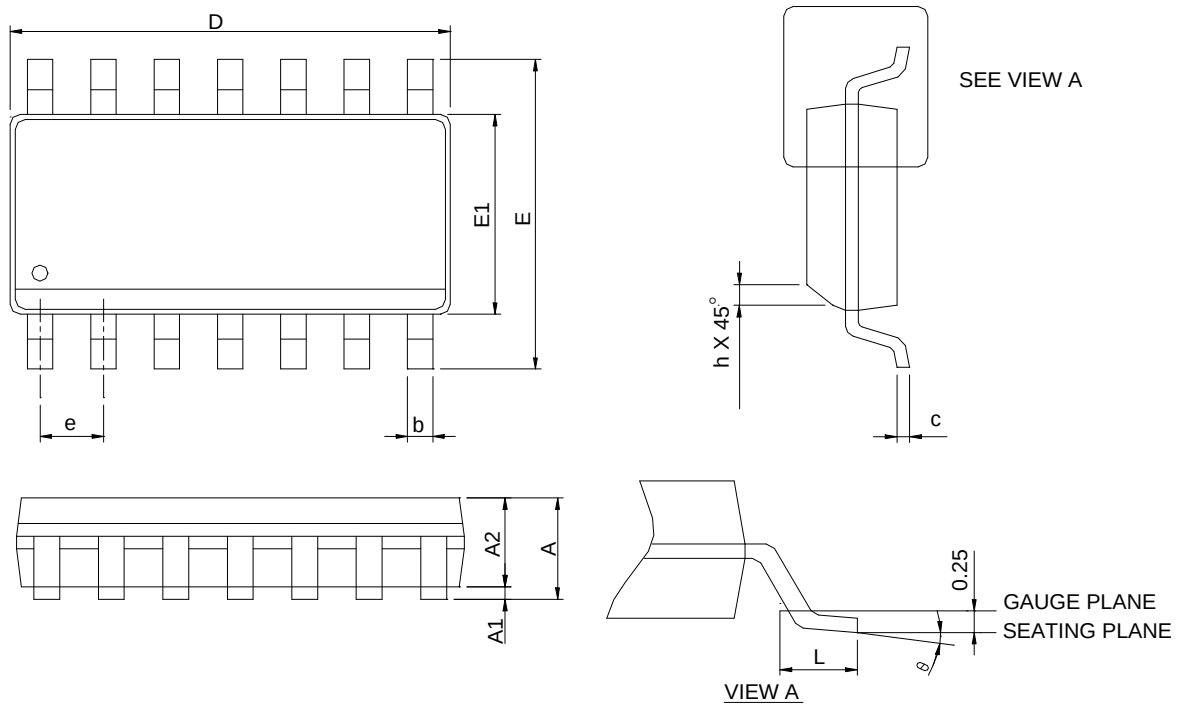


Figure 8. Recommended Layout Diagram

Package Information

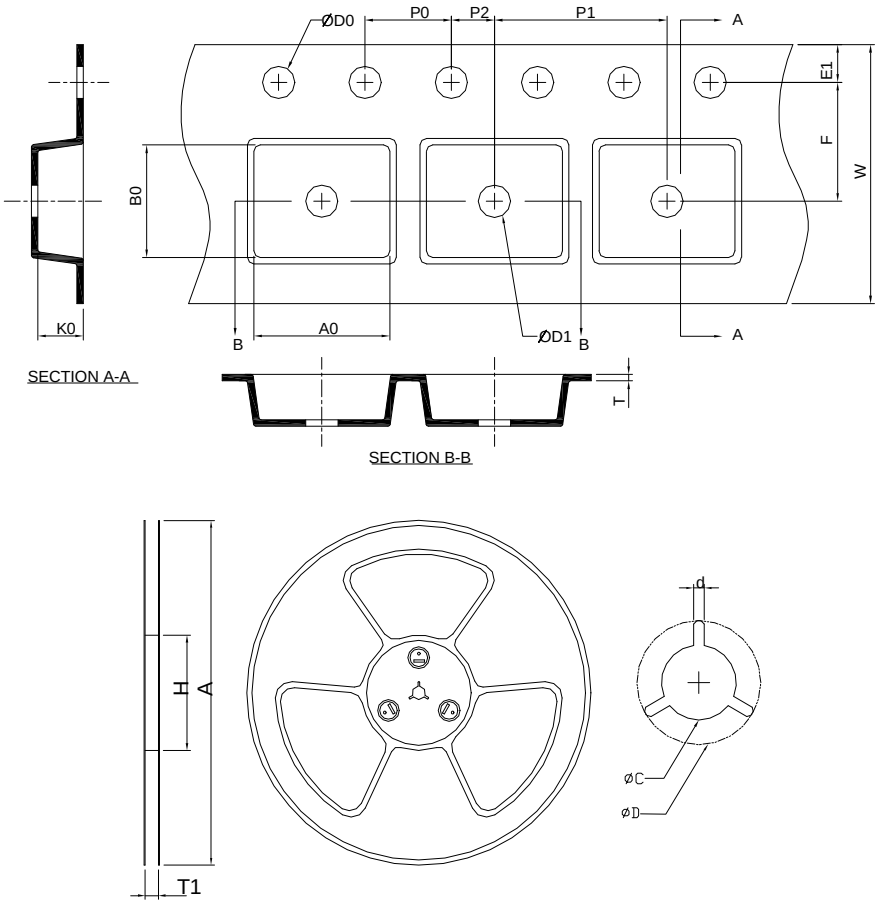
SOP-14



SYMBOL	SOP-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AB.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-14	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	9.00±0.20	2.10±0.20

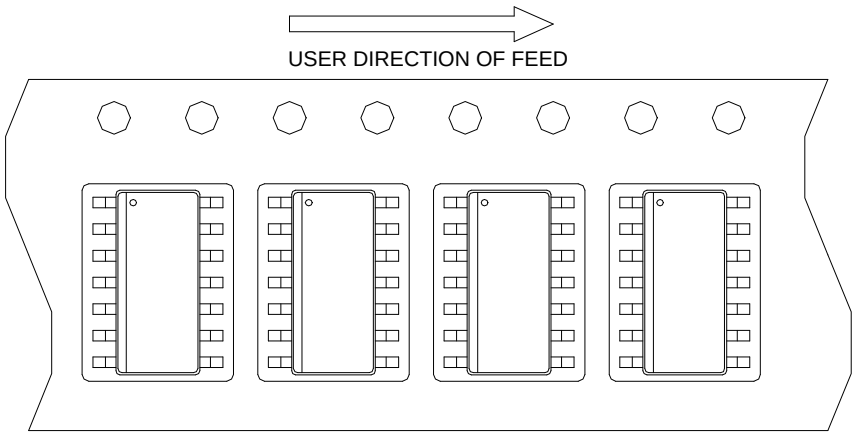
(mm)

Devices Per Unit

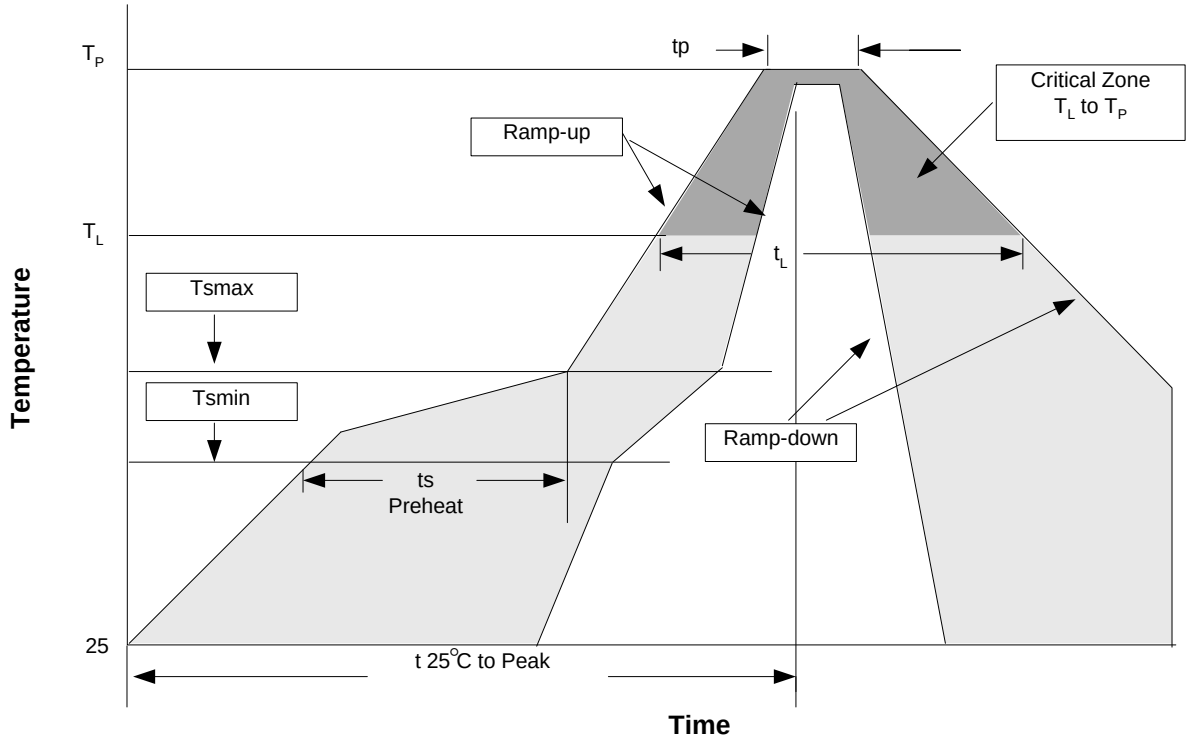
Package Type	Unit	Quantity
SOP-14	Tape & Reel	2500

Taping Direction Information

SOP-14



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838