Bt102

75 MHz Monolithic CMOS Single 8-bit VIDEODAC™

Distinguishing Features

- 75 MHz Pipelined Operation
- ±1/4 LSB Differential Linearity Error
- ±1/2 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Output
- 0, 7, or 10 IRE Programmable Setup
- +5 V CMOS Monolithic Construction
- 24-pin 0.3" DIP Package
- Typical Power Dissipation: 550 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Conventional D/A

Product Description

The Bt102 is an 8-bit multifunction VIDEODAC, designed specifically for color graphics and conventional D/A converter applications.

Available control inputs include sync, blank, reference white, and 10% overbright. Additional features include a threshold set input to configure the digital inputs to be either TTL or CMOS compatible, and a setup input to specify one of three available setups in the analog output.

An external 1.2 V voltage reference and a single resistor control the full-scale output current. The sync, blank, reference white, and 10% overbright inputs are pipelined to maintain synchronization with the input data.

The Bt102 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. The differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ±1/4 LSB and ±1/2 LSB, respectively, over the full temperature range.

Functional Block Diagram
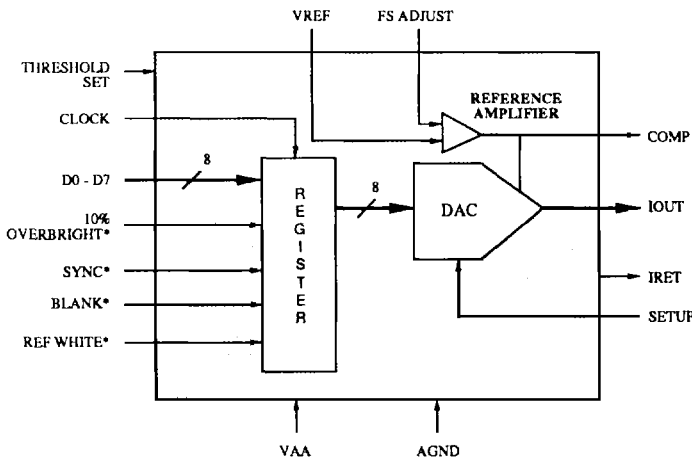
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Circuit Description

As illustrated in the functional block diagram, the Bt102 contains a single 8-bit D/A converter, input registers, and a reference amplifier.

The THRESHOLD SET input controls the logic thresholds of the digital inputs. If it is left floating, the logic thresholds are TTL compatible; if connected to VAA, the thresholds are CMOS compatible.

On the rising edge of each clock cycle, as shown below in Figure 1, 8 bits of data (D0–D7) are latched into the device and presented to the 8-bit D/A converter. The REF WHITE* input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF, regardless of the value of the D0–D7 inputs.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC*, BLANK*, and 10% OVERBRIGHT* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs modify the output level.

The SETUP input is used to control the difference between the black and blanking level. Available setups include 10 IRE (SETUP = VAA), 7 IRE (SETUP = float), and 0 IRE (SETUP = AGND). A setup of 0 IRE specifies that the blanking level is the same as the black level.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. The VREF input requires an external 1.2 V (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converter on the Bt102 uses a segmented architecture in which bit currents are routed to either the output or IRET by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt102 is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.
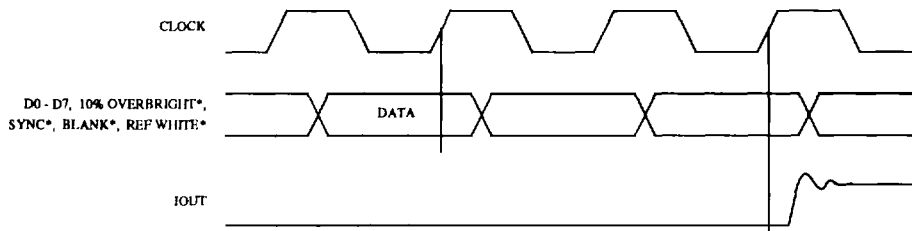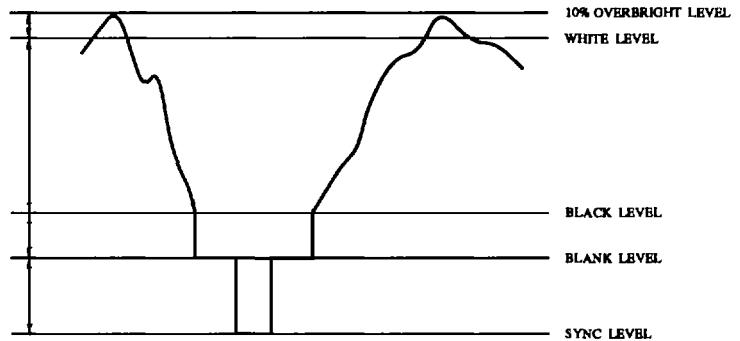

Figure 1.   Input/Output Timing.

Circuit Description (continued)

RSET = 1130 SETUP = VAA		RSET = 1110 SETUP = FLOAT		RSET = 1050 SETUP = AGND	
IRE	MA	IRE	MA	IRE	MA
9.5	28.90 27.01	10	28.74 26.81	10.75	29.00 26.97
90		92.9		100	
10	9.59 7.65	7.1	9.09 7.72	0	8.23 8.23
39.5	0.00	40.5	0.00	44	0.00

Note: 75 Ω doubly terminated load, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform.

Description	IOUT (mA)	10% OVERBRIGHT*	REF WHITE*	SYNC*	BLANK*	DAC Input Data
WHITE +10%	28.74	0	1	1	1	$FF
WHITE	26.81	1	0	1	1	$xx
WHITE	26.81	1	1	1	1	$FF
DATA +10%	data + 11.0	0	1	1	1	data
DATA	data + 9.09	1	1	1	1	data
DATA - SYNC	data + 1.37	1	1	0	1	data
BLACK	9.09	1	1	1	1	$00
BLACK - SYNC	1.37	1	1	0	1	$00
BLANK	7.72	x	x	1	0	$xx
SYNC	0	x	x	0	0	$xx

Note: Typical with white level current = 26.81 mA. RSET = 1110 Ω, VREF = 1.235 V, SETUP = float.

Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL/CMOS compatible). A logical zero drives the output to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0–D7, REF WHITE*, and 10% OVERBRIGHT* inputs are ignored.
SYNC*	Composite sync control input (TTL/CMOS compatible). A logical zero on this input switches off a current source on the output equal to approximately 30% of the full-scale current (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE*	Reference white control input (TTL/CMOS compatible). A logical zero on this input forces the output to the white level, regardless of the D0–D7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
10% OVERBRIGHT*	Overbright control input (TTL/CMOS compatible). A logical zero on this input causes the output current to increase by approximately 10 IRE units as shown in Table 1 and Figure 2. It is latched on the rising edge of CLOCK.
D0–D7	Data inputs (TTL/CMOS compatible). D0 is the least significant data bit. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL/CMOS compatible). The rising edge of CLOCK latches the D0–D7, SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL or CMOS buffer to avoid reflection-induced jitter.
SETUP	Setup control input. This pin controls the difference between the black level and the blanking level. Available setups include 10 IRE units (SETUP = VAA), 7 IRE units (SETUP = float), and 0 IRE units (SETUP = AGND).
THRESHOLD SET	Threshold control input. This pin controls the logic thresholds of the digital inputs. If connected to VAA through a 0.1 µF ceramic capacitor, the logic thresholds are TTL compatible. If connected directly to VAA, the thresholds are CMOS compatible.
IOUT	Current output. This high-impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3).
IRET	Current return. This pin must be connected to AGND through a ferrite bead, as illustrated in Figure 3.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name	Description

COMP | Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

FS ADJUST | Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 3). Note that the IRE relationships in Figure 3 are maintained regardless of the full-scale output current.

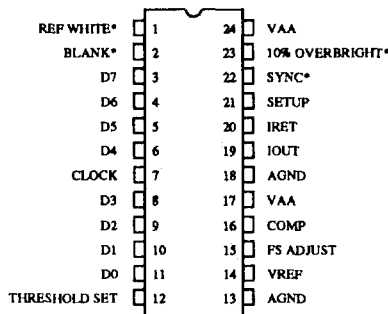The relationship between RSET and the white level output current is:

$$RSET\ (\Omega) = K1 * VREF\ (V) / IOUT\ (mA)$$

The amount of additional current generated to achieve the overbright level is:

$$IOUT\ (mA) = K2 * VREF\ (V) / RSET\ (\Omega)$$

K1 and K2 are defined as follows:

	SETUP		
	float	VAA	AGND
K1	24,096	24,713	22,930
K2	1,735	1,729	1,726

```
REF WHITE*   [  1        24 ]  VAA
    BLANK*   [  2        23 ]  10% OVERBRIGHT*
       D7    [  3        22 ]  SYNC*
       D6    [  4        21 ]  SETUP
       D5    [  5        20 ]  IRET
       D4    [  6        19 ]  IOUT
    CLOCK    [  7        18 ]  AGND
       D3    [  8        17 ]  VAA
       D2    [  9        16 ]  COMP
       D1    [ 10        15 ]  FS ADJUST
       D0    [ 11        14 ]  VREF
THRESHOLD SET [ 12       13 ]  AGND
```

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt102 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible so as to minimize inductive ringing.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk. The analog ground plane should include all Bt101 ground pins, all reference circuitry and decoupling, power supply bypass circuitry for the Bt101, analog output traces, and the video output connector.

Power Planes

The Bt102 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt102.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt102 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that, while the Bt102 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt102 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt102 should be avoided to reduce noise pickup.

Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The Bt102 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch.

The video output signal should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog output should have a 75 Ω load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt102 to minimize reflections.

PC Board Layout Considerations (continued)
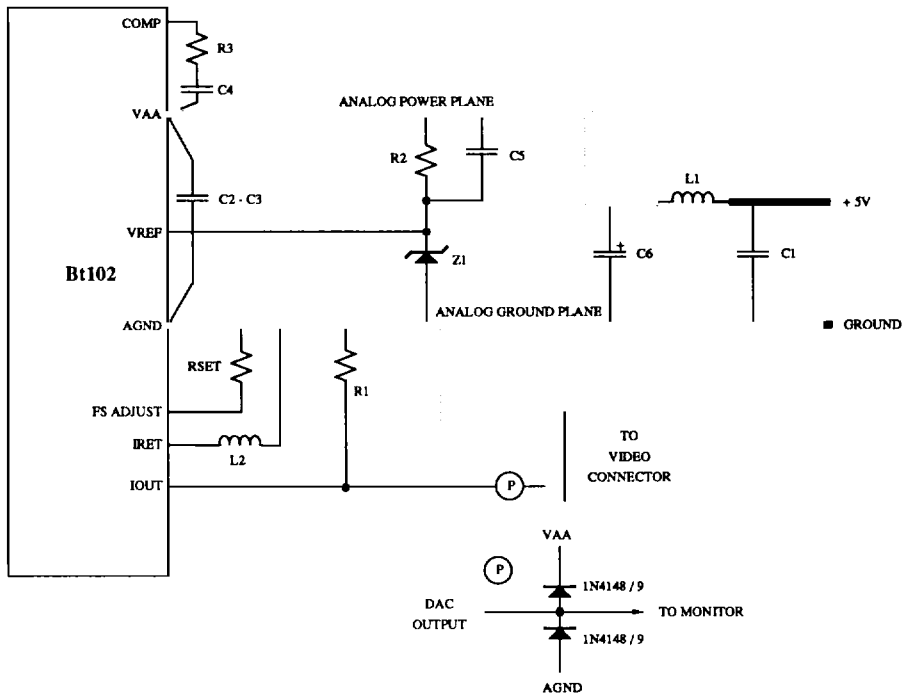
Location	Description	Vendor Part Number
C1, C2, C3, C5	0.1 μF ceramic capacitor	Erie RPE112Z5U104M50V
C4	0.01 μF ceramic capacitor	Erie RPE110Z5U103M50V
C6	10 μF tantalum capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	75 Ω 1% metal film resistor	Dale CMF-55C
R2	1000 Ω 1% metal film resistor	Dale CMF-55C
R3	27 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt102.

Figure 3.   Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly terminated 75 Ω load be used with the SETUP pin floating and an RSET value of about 1594 Ω. If the Bt102 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75 Ω and singly terminated 75 Ω loads.

If driving a large capacitive load (load RC > $1/(20 f_c\pi))$*, it is recommended that an output buffer be used to drive a doubly terminated 75 Ω load.

Color Applications

Note that in color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may always be a logical zero. If SYNC* is always a logical zero, the relationship between RSET and the full-scale output current is:

$$IOUT (mA) = K * VREF (V) / RSET (\Omega)$$

where K is equal to 17,714; 17,158; or 15,933 for SETUP = VAA, float, and AGND, respectively.

Using Multiple Devices

If located close together on the same PC board, multiple Bt102 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt102 must still have its individual RSET resistor, IOUT termination resistor (R1 in Figure 3), IRET ferrite bead (L3 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R3 in Figure 3).

At high clock rates, individual ground beads (L2 in Figure 3) may be required to maintain TTL thresholds due to the high current return.

Non-Video Applications

The Bt102 may be used in non-video applications by disabling the video-specific control inputs. SYNC* should be a logical zero, while REF WHITE*, 10% OVERBRIGHT*, and BLANK* should be a logical one. SETUP should be connected to AGND. The output current will be determined solely by the D0–D7 inputs.

*(f_c = clock frequency)

The relationship between RSET and the full-scale output current in this configuration is as follows:

$$RSET (\Omega) = 15,933 * VREF (V) / IOUT (mA)$$

The BLANK* input may optionally be used as a "force to zero" control, and the REF WHITE* input may optionally be used as a "force to full-scale" control.

COMP Resistor

To optimize the settling time of the Bt102, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 27 Ω, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Analog Output Protection

The Bt102 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	–25		+85	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on Any Signal Pin*		AGND – 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1/2	LSB
Differential Linearity Error	DL			±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
TTL-Compatible Mode					
Input High Voltage	VIH				
CLOCK		3.0		VAA + 0.5	Volts
Other		2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND − 0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH	−200		−1200	μA
Input Low Current (Vin = 0.4 V)	IIL	−200		−1200	μA
Input Capacitance	CIN		10		pF
CMOS-Compatible Mode					
Input High Voltage	VIH	3.5		AGND + 0.5	Volts
Input Low Voltage	VIL	AGND − 0.5		0.8	Volts
Input High Current (Vin = 3.5 V)	IIH			2	μA
Input Low Current (Vin = 1.5 V)	IIL			2	μA
Input Capacitance	CIN		10		pF
Analog Output					
Gray Scale Current Range		15		20.5	mA
Output Current					
Overbright Relative to White		1.60	1.93	2.40	mA
White Level Relative to Blank		17.90	19.09	20.31	mA
White Level Relative to Black		16.80	17.72	18.61	mA
Black Level Relative to Blank					
SETUP = float		1.10	1.37	1.70	mA
SETUP = AGND		0	5	50	μA
SETUP = VAA		1.6	1.93	2.4	mA
Blanking Level		7.2	7.72	8.3	mA
Sync Level		0	5	50	μA
LSB Size			69.5		μA
Output Compliance	VOC	−1.0		+1.4	Volts
Output Impedance	ROUT		33		KΩ
Output Capacitance	COUT		20		pF
Voltage Reference Input Current	IREF			10	μA
Power Supply Rejection Ratio (COMP = 0.01 μF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with SETUP = float, RSET = 1110 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			75	MHz
Data and Control Setup Time	TSU	4			ns
Data and Control Hold Time	TH	1			ns
Clock Cycle Time	TCYC	13.33			ns
Clock Pulse Width Low	TCLKH	5			ns
Clock Pulse Width High	TCLKL	6			ns
Analog Output Delay	TDLY		20		ns
Analog Output Rise/Fall Time	TVRF		6		ns
Analog Output Settling Time*	TS				
to ± 1/2 LSB			15		ns
to ± 1 LSB			12		ns
Clock and Data Feedthrough*			−20		dB
Glitch Impulse*			100		pV - sec
Differential Gain Error	DG		1		% Gray Scale
Differential Phase Error	DP		1		Degree
Pipeline Delay		3	3	3	Clocks
VAA Supply Current**	IAA		110	175	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1110 Ω, VREF = 1.235 V. THRESHOLD SET = TTL mode, SETUP = float. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 27 Ω. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, −3 dB test bandwidth = 150 MHz.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Ordering Information

| Model Number	Speed	Package	Ambient Temperature Range
Bt102BC	75 MHz	24-pin 0.3" CERDIP	–25° to +85° C
Bt102EVM	Evaluation Board for the Bt102		

Timing Waveforms
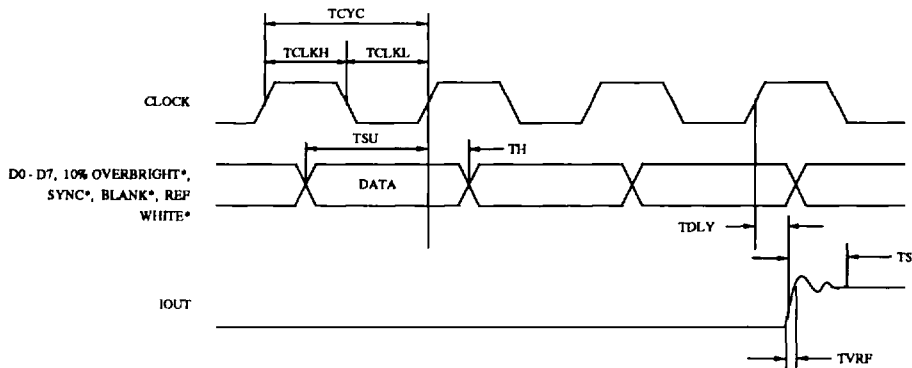
Note 1:   Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2:   Settling time measured from the 50% point of full-scale transition to the output remaining within ±1/2 LSB or ±1 LSB.

Note 3:   Output rise/fall time measured between the 20% and 80% points of full-scale transition.

Figure 4.   Input/Output Timing.

Device Circuit Data
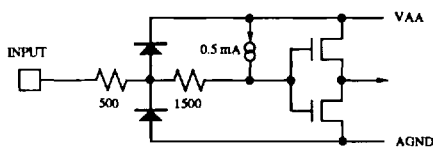
High-speed operation is accomplished through pipelining and a unique (patent pending) TTL input buffer. This input buffer features a resistive level shifter that uses a temperature and process-compensated current source.

The 0.5 mA bias current is disabled when THRESHOLD SET is connected to VAA, resulting in a standard high-impedance CMOS input.

Equivalent Circuit of the Digital Inputs.
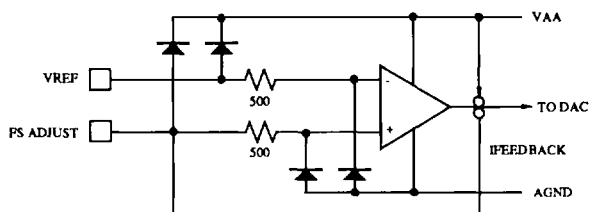
Equivalent Circuit of the Reference Amplifier.
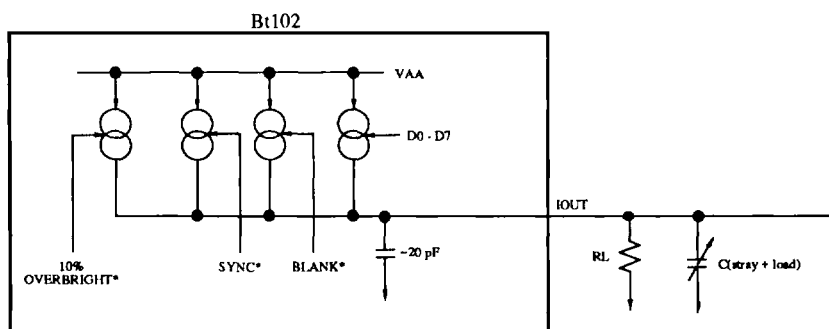
Equivalent Circuit of the Current Output.