WHITE ELECTRONIC DESIGNS

# 512Kx32 SRAM MODULE, SMD 5962-94611

FEATURES

- Access Times of 15*, 17, 20, 25, 35, 45, 55ns

- Packaging

  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400).

  - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") (Package 502)[1]

  - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880") square (Package 510) 3.56mm (0.140") height.

  - 68 lead, Hermetic CQFP (G2L), 22.4mm (0.880") square, 5.08mm (0.200") high (Package 528).

  - 68 lead, Hermetic CQFP (G1U)[1], 23.9mm (0.940") square (Package 519) 3.57mm (0.140") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3).

  - 68 lead, Hermetic CQFP (G1T), 23.9mm (0.940") square (Package 524) 4.06mm (0.160") height.

- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8

- Commercial, Industrial and Military Temperature Ranges

- TTL Compatible Inputs and Outputs

- 5 Volt Power Supply

- Low Power CMOS

- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

- Weight
  WS512K32N-XH1X - 13 grams typical
  WS512K32-XG2UX - 8 grams typical
  WS512K32-XG1UX[1] - 5 grams typical
  WS512K32-XG1TX - 5 grams typical
  WS512K32-XG4TX[1] - 20 grams typical
  WS512K32-XG2LX - 8 grams typical

*15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.
Note 1: Package Not Recommended For New Design

FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH1X

TOP VIEW
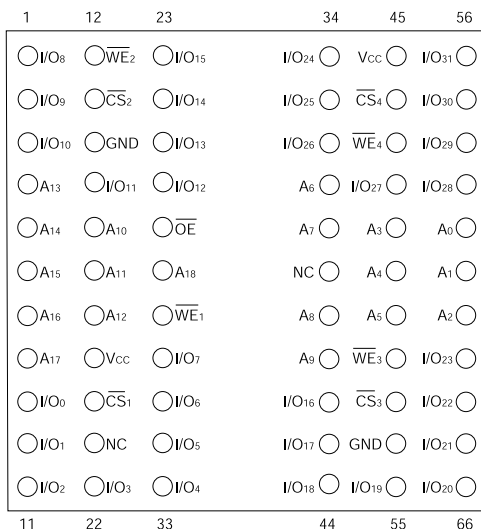
PIN DESCRIPTION

Pin	Description
I/O_{0-31}	Data Inputs/Outputs
A_{0-18}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM
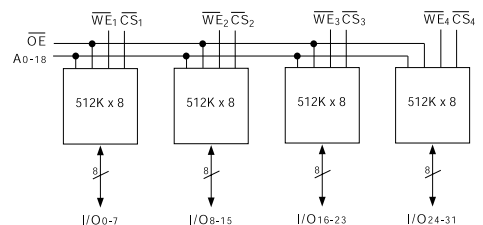
FIG. 2   PIN CONFIGURATION FOR WS512K32-XG4TX[1]

TOP VIEW

PIN DESCRIPTION

I/O$_{0-31}$	Data Inputs/Outputs
A$_{0-18}$	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM
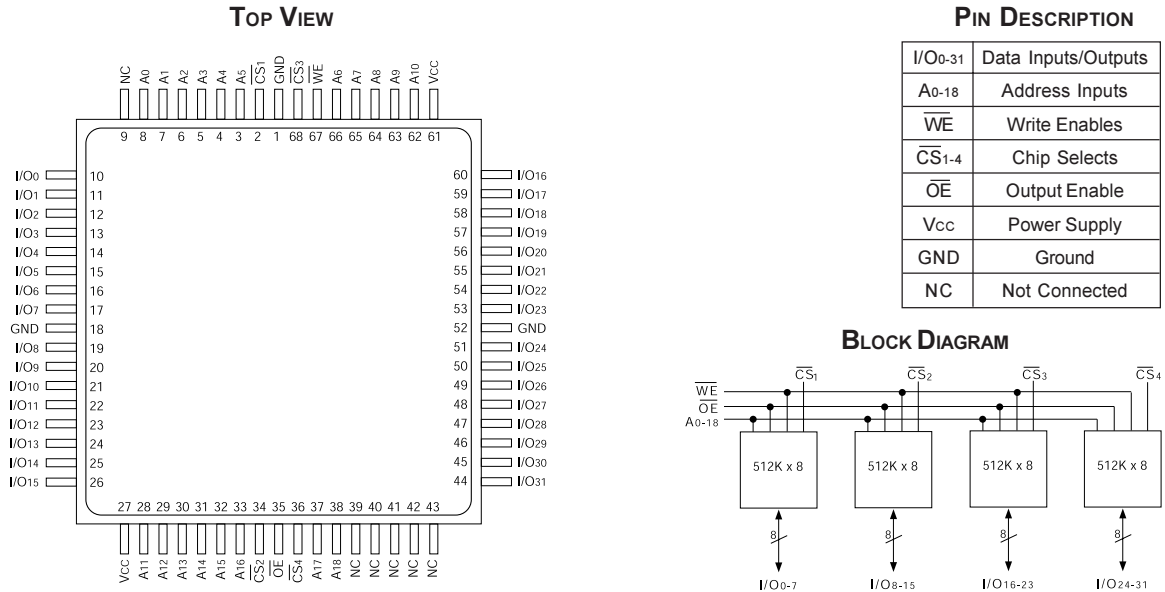
Note 1: Package Not Recommended For New Design

FIG. 3   PIN CONFIGURATION FOR WS512K32-XG2UX, WS512K32-XG2LX, WS512K32-XG1TX AND WS512K32-XG1UX[1]

TOP VIEW

PIN DESCRIPTION

I/O$_{0-31}$	Data Inputs/Outputs
A$_{0-18}$	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM
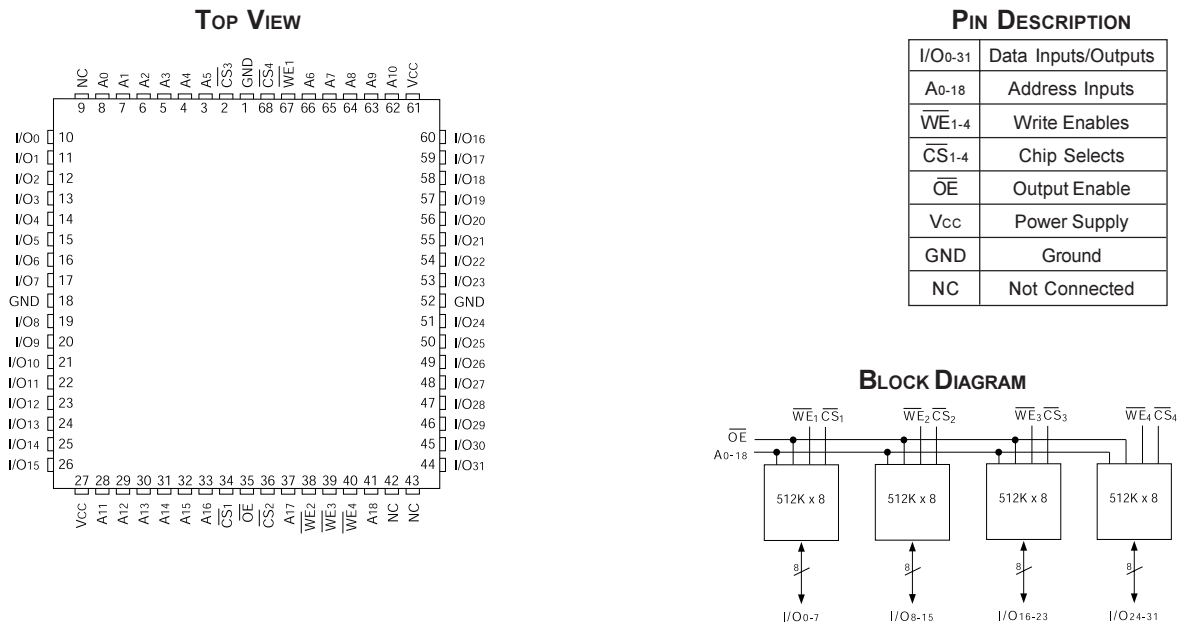
Note 1: Package Not Recommended For New Design

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

CAPACITANCE
(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4T			50	
CQFP G2U/G1U/G1T/G2L			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to Vcc		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to Vcc		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		660	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		80	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA for 15 - 35ns, I_{OL} = 2.1mA for 45 - 55ns, Vcc = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA for 15 - 35ns, I_{OH} = -1.0mA for 45 - 55ns, Vcc = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = Vcc -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS
(T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq$ Vcc − 0.2V	2.0	5.5	V
Data Retention Current	I_{CCDR1}	Vcc = 3V		28	mA
Low Power Data Retention Current (WS512K32L-XXX)	I_{CCDR2}	Vcc = 3V		16	mA

AC CHARACTERISTICS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter Read Cycle	Symbol	-15* Min	-15* Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	-35 Min	-35 Max	-45 Min	-45 Max	-55 Min	-55 Max	Units
Read Cycle Time	tRC	15		17		20		25		35		45		55		n s
Address Access Time	tAA		15		17		20		25		35		45		55	n s
Output Hold from Address Change	tOH	0		0		0		0		0		0		0		n s
Chip Select Access Time	tACS		15		17		20		25		35		45		55	n s
Output Enable to Output Valid	tOE		8		9		10		12		25		25		25	n s
Chip Select to Output in Low Z	tCLZ[1]	2		2		2		2		4		4		4		n s
Output Enable to Output in Low Z	tOLZ[1]	0		0		0		0		0		0		0		n s
Chip Disable to Output in High Z	tCHZ[1]		12		12		12		12		15		20		20	n s
Output Disable to Output in High Z	tOHZ[1]		12		12		12		12		15		20		20	n s

*15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
### (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter Write Cycle	Symbol	-15* Min	-15* Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	-35 Min	-35 Max	-45 Min	-45 Max	-55 Min	-55 Max	Units
Write Cycle Time	tWC	15		17		20		25		35		45		55		n s
Chip Select to End of Write	tCW	13		15		15		17		25		35		50		n s
Address Valid to End of Write	tAW	13		15		15		17		25		35		50		n s
Data Valid to End of Write	tDW	10		11		12		13		20		25		25		n s
Write Pulse Width	tWP	13		15		15		17		25		35		40		n s
Address Setup Time	tAS	2		2		2		2		2		2		2		n s
Address Hold Time	tAH	0		0		0		0		0		5		5		n s
Output Active from End of Write	tOW[1]	2		2		3		4		4		5		5		n s
Write Enable to Output in High Z	tWHZ[1]		8		9		11		13		15		20		20	n s
Data Hold Time	tDH	0		0		0		0		0		0		0		n s

*15ns Access Time available only in Commercial and Industrial Temperature. This speed is not fully characterized and is subject to change without notice.

1. This parameter is guaranteed by design but not tested.

2. The Address Setup Time of minimum 2ns is for the G2U, G1U and H1 packages. tAS minimum for the G4T package is 0ns.

FIG. 4 AC TEST CIRCUIT
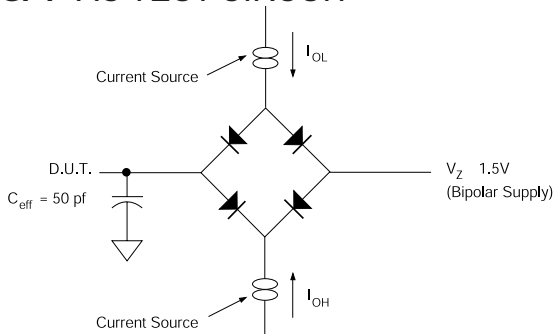
AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 ý.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.
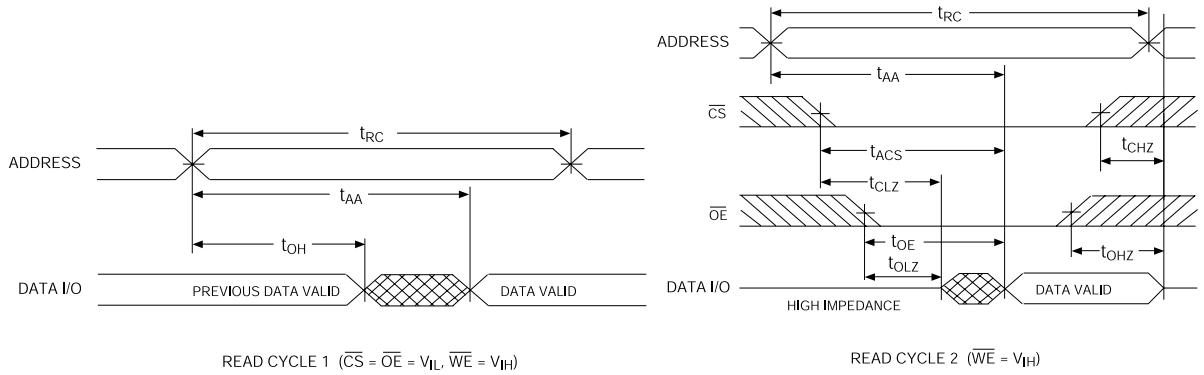
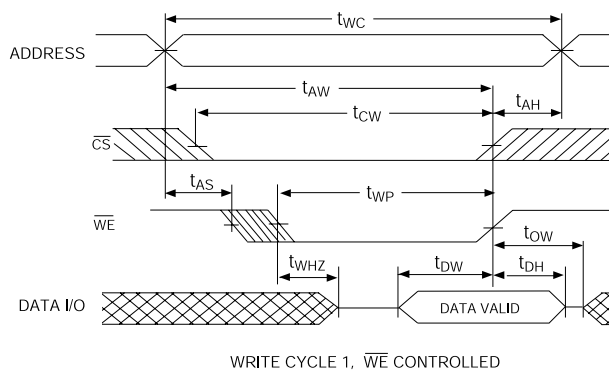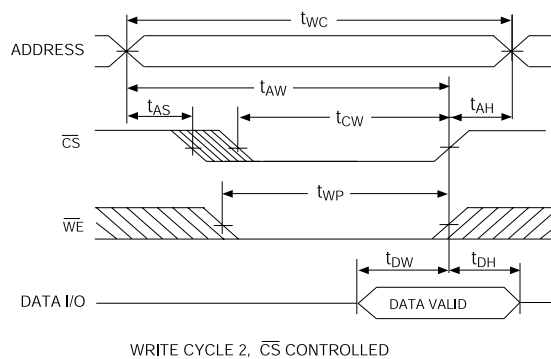## FIG. 5   TIMING WAVEFORM - READ CYCLE

READ CYCLE 1 ($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)

READ CYCLE 2 ($\overline{WE} = V_{IH}$)

FIG. 6   WRITE CYCLE - $\overline{WE}$ CONTROLLED

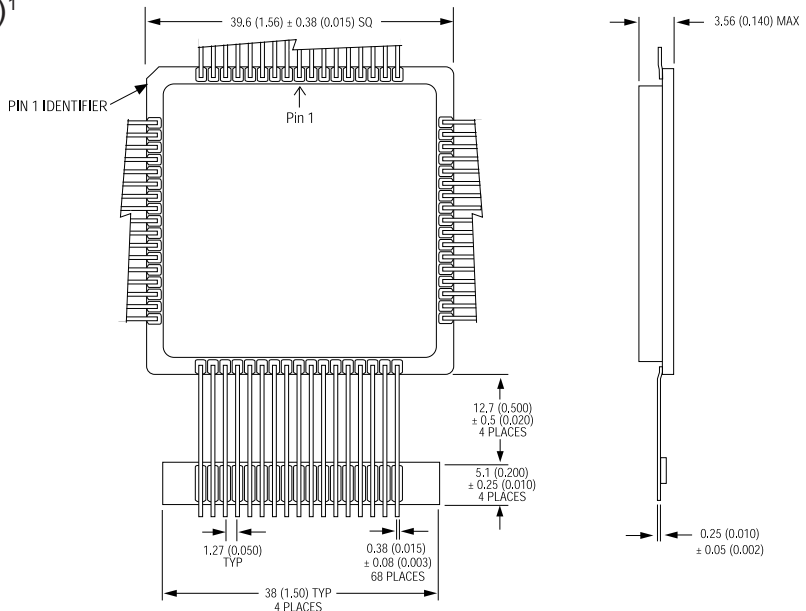WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 7   WRITE CYCLE - $\overline{CS}$ CONTROLLED

WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)

27.3 (1.075) ± 0.25 (0.010) SQ

PIN 1 IDENTIFIER
SQUARE PAD
ON BOTTOM

25.4 (1.0) TYP

4.34 (0.171) MAX

3.81 (0.150) ± 0.13 (0.005)

2.54 (0.100) TYP

15.24 (0.600) TYP

1.42 (0.056) ± 0.13 (0.005)

0.76 (0.030) ± 0.13 (0.005)

1.27 (0.050) TYP DIA

0.46 (0.018) ± 0.05 (0.002) DIA

25.4 (1.0) TYP
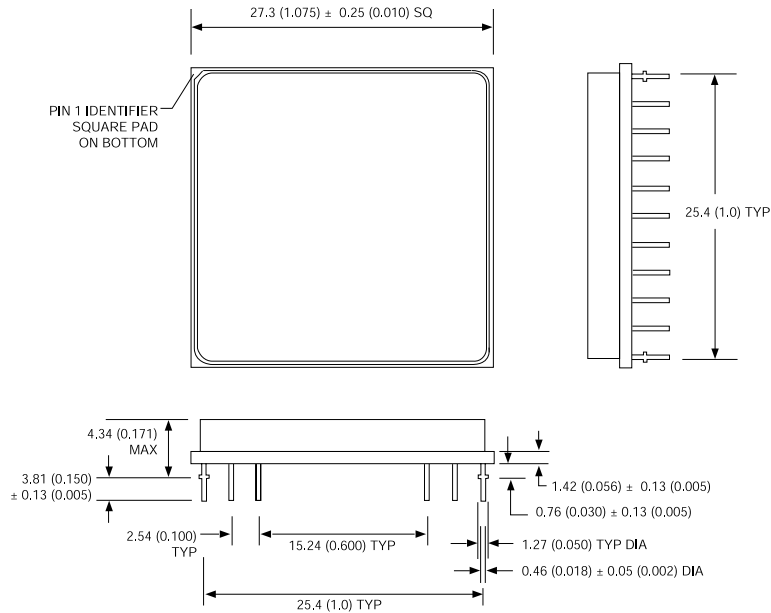
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)[1]

39.6 (1.56) ± 0.38 (0.015) SQ

3.56 (0.140) MAX

PIN 1 IDENTIFIER

Pin 1

12.7 (0.500) ± 0.5 (0.020) 4 PLACES

5.1 (0.200) ± 0.25 (0.010) 4 PLACES

0.25 (0.010) ± 0.05 (0.002)

1.27 (0.050) TYP

0.38 (0.015) ± 0.08 (0.003) 68 PLACES
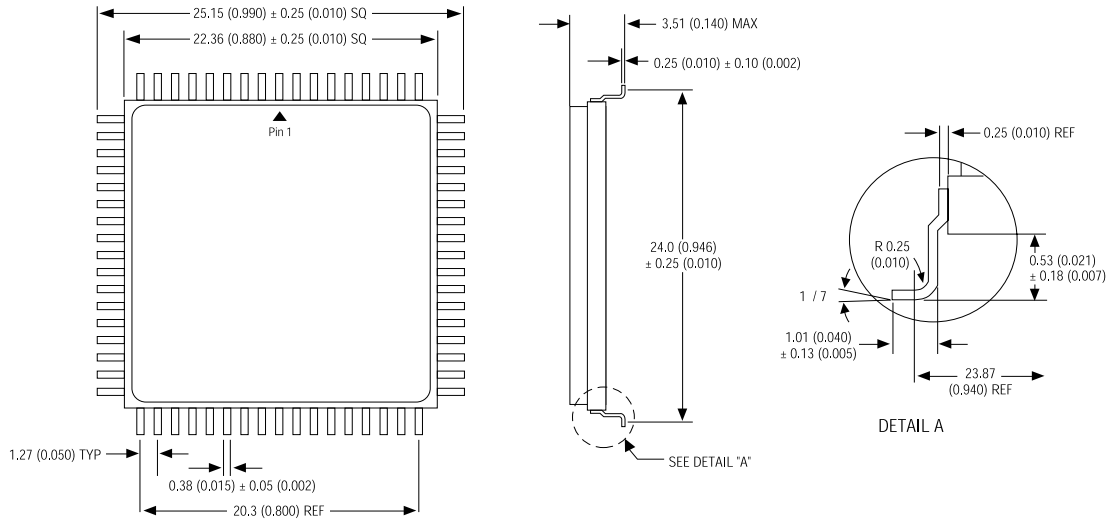
38 (1.50) TYP 4 PLACES

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note 1: Package Not Recommended For New Design

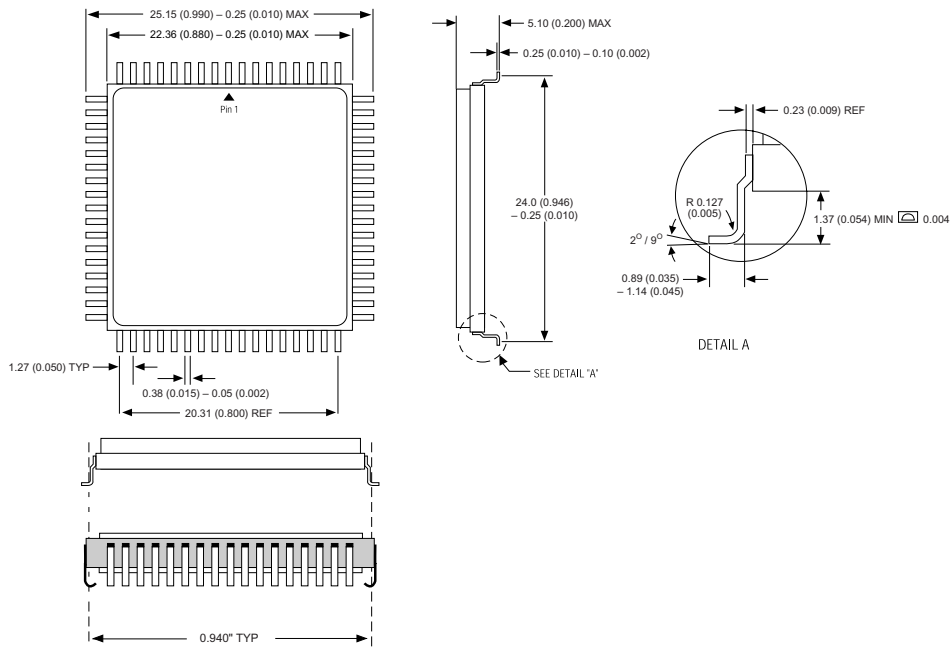## PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)

25.15 (0.990) ± 0.25 (0.010) SQ

22.36 (0.880) ± 0.25 (0.010) SQ

Pin 1

3.51 (0.140) MAX

0.25 (0.010) ± 0.10 (0.002)

24.0 (0.946) ± 0.25 (0.010)

SEE DETAIL "A"

0.25 (0.010) REF

R 0.25 (0.010)

1 / 7

1.01 (0.040) ± 0.13 (0.005)

0.53 (0.021) ± 0.18 (0.007)

23.87 (0.940) REF

DETAIL A

1.27 (0.050) TYP

0.38 (0.015) ± 0.05 (0.002)

20.3 (0.800) REF

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 528: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)

25.15 (0.990) − 0.25 (0.010) MAX

22.36 (0.880) − 0.25 (0.010) MAX

Pin 1

5.10 (0.200) MAX

0.25 (0.010) − 0.10 (0.002)

24.0 (0.946) − 0.25 (0.010)

SEE DETAIL "A"

0.23 (0.009) REF

R 0.127 (0.005)

$2^\circ / 9^\circ$

0.89 (0.035) − 1.14 (0.045)

1.37 (0.054) MIN   0.004

DETAIL A

1.27 (0.050) TYP

0.38 (0.015) − 0.05 (0.002)

20.31 (0.800) REF

0.940" TYP

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)[1]
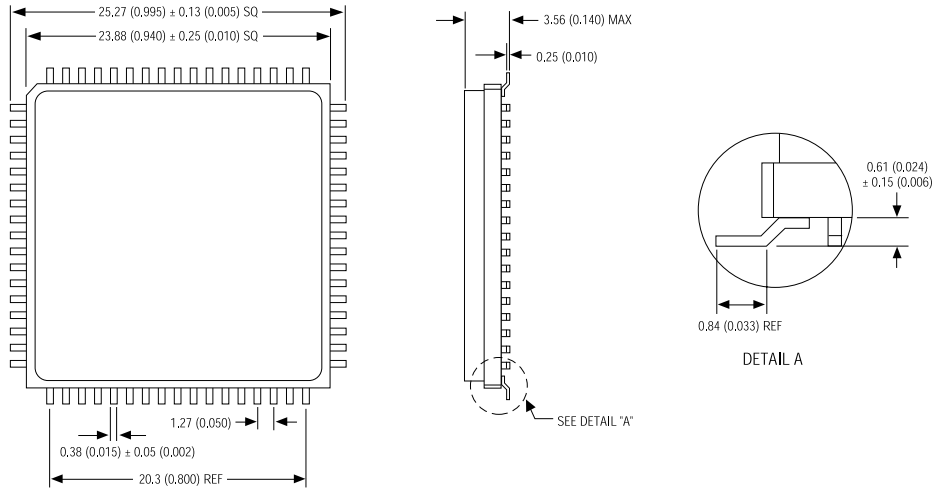
25,27 (0.995) ± 0.13 (0.005) SQ

23,88 (0.940) ± 0.25 (0.010) SQ

3.56 (0.140) MAX

0,25 (0.010)

0,61 (0.024) ± 0.15 (0.006)

0,84 (0.033) REF

DETAIL A

SEE DETAIL "A"

1.27 (0.050)
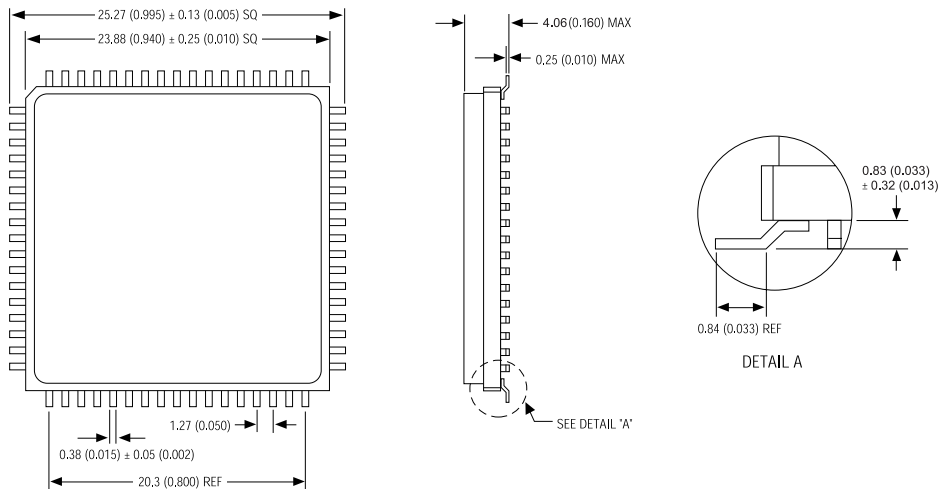
0,38 (0.015) ± 0.05 (0.002)

20.3 (0.800) REF

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

Note1: Package Not Recommended For New Design

PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)

25.27 (0.995) ± 0.13 (0.005) SQ

23.88 (0.940) ± 0.25 (0.010) SQ

4.06 (0.160) MAX

0.25 (0.010) MAX

0.83 (0.033) ± 0.32 (0.013)

0.84 (0.033) REF

DETAIL A

1.27 (0.050)

0.38 (0.015) ± 0.05 (0.002)

20.3 (0.800) REF

SEE DETAIL 'A'

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S   512K 32 X - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial   -40°C to 85°C

C = Commercial   0°C to +70°C

PACKAGE TYPE:

H1 = Ceramic Hex-In-line Package, HIP (Package 400)

G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)

G2L = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 528)

G4T[1] = 40mm Low Profile CQFP (Package 502)

G1U[1] = 23.9mm Low Profile CQFP (Package 519)

G1T = 23.9mm Low Profile CQFP (Package 524)

ACCESS TIME (ns)

IMPROVEMENT MARK:

Blank = Standard Power

N = No Connect at pin 21 and 39 in HIP for Upgrades

L = Low Power Data Retention

ORGANIZATION, 512Kx32

User configurable as 1Mx16 or 2Mx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.

Note 1: Package Not Recommended For New Design

WHITE ELECTRONIC DESIGNS

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-94611 05HTX
512K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-94611 06HTX
512K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-94611 07HTX
512K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-94611 08HTX
512K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-94611 09HTX
512K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-94611 10HTX
512K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 05HYX
512K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 06HYX
512K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 07HYX
512K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 08HYX
512K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 09HYX
512K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 10HYX
512K x 32 SRAM Module	55ns	68 lead CQFP (G2U)	5962-94611 05HMX
512K x 32 SRAM Module	45ns	68 lead CQFP (G2U)	5962-94611 06HMX
512K x 32 SRAM Module	35ns	68 lead CQFP (G2U)	5962-94611 07HMX
512K x 32 SRAM Module	25ns	68 lead CQFP (G2U)	5962-94611 08HMX
512K x 32 SRAM Module	20ns	68 lead CQFP (G2U)	5962-94611 09HMX
512K x 32 SRAM Module	17ns	68 lead CQFP (G2U)	5962-94611 10HMX
512K x 32 SRAM Module	55ns	68 lead CQFP (G1U)[1]	5962-94611 05H9X
512K x 32 SRAM Module	45ns	68 lead CQFP (G1U)[1]	5962-94611 06H9X
512K x 32 SRAM Module	35ns	68 lead CQFP (G1U)[1]	5962-94611 07H9X
512K x 32 SRAM Module	25ns	68 lead CQFP (G1U)[1]	5962-94611 08H9X
512K x 32 SRAM Module	20ns	68 lead CQFP (G1U)[1]	5962-94611 09H9X
512K x 32 SRAM Module	17ns	68 lead CQFP (G1U)[1]	5962-94611 10H9X
512K x 32 SRAM Module	55ns	68 lead CQFP (G2L)	5962-94611 05HAX
512K x 32 SRAM Module	45ns	68 lead CQFP (G2L)	5962-94611 06HAX
512K x 32 SRAM Module	35ns	68 lead CQFP (G2L)	5962-94611 07HAX
512K x 32 SRAM Module	25ns	68 lead CQFP (G2L)	5962-94611 08HAX
512K x 32 SRAM Module	20ns	68 lead CQFP (G2L)	5962-94611 09HAX
512K x 32 SRAM Module	17ns	68 lead CQFP (G2L)	5962-94611 10HAX

Note 1: Package Not Recommended For New Design

Document Title

512K x 32 SRAM Multi-Chip Package

Revision History

Rev #   History

		Release Date	Status
	Initial	October 1996	Preliminary
	Change (Pg. 1, 3) 1.1 Change Operation Supply Current from 520mA To 540mA 1.2 Change Data Retention Current from 12mA to 28mA.	January 1997	Preliminary
	Change (Pg. 1, 2, 8, 10, 11) 1.1 Delete G2 Package	November 1997	Preliminary
	Change (Pg. 1, 9) 1.1 Add SMD Case Outline M for G2T	February 1998	Preliminary
	Change (Pg. 1, 3, 8) 1.1 Remove Low Capacitance package option	April 1998	Preliminary
	Change (Pg. 1, 6, 8) 1.1 Add H1 package	December 1998	Preliminary
	Change (Pg. 1, 4, 6, 9, 10) 1.1 Remove H2 package 1.2 Change logo to WEDC logo	March 1999	Preliminary
Rev 2	Change (Pg. 1, 3, 4, 8) 1.1 Change status from Preliminary to Final 1.2 Make package descriptions consistent 1.3 Add 15ns as available in Commercial and Industrial Temperatures only.	May 1999	Final
Rev 4	Change (Pg. 1, 3) 1.1 Change Standby Current (Isb) from 60mA to 80mA Maximum	June 1999	Final
Rev 5	Change (Pg. 1, 2, 3, 4, 7, 8) 1.1 Add G1U package	November 1999	Final
Rev 6	Change (Pg. 1, 8) 1.1 Change G1U lead foot length from 0.64mm to 0.84mm Ref	February 2000	Final

Rev 7   Change (Pg. 1, 3, 9)   October 2000   Final
          1.1 Change Operating Supply Current from 540mA to 660mA Maximum
          1.2 Add Low Power Data Retention Current of 16mA to Data Retention Characteristics table
          1.3 Add Low Power Data Retention (L) option to Ordering Information

Rev 8   Change (Pg. 1, 2, 6, 7, 9, 10)   October 2001   Final
          1.1 Change G2T and G4T package status to Not Recommended For New Design

Rev 9   Change (Pg. 1, 2, 3, 8, 9, 10)   November 2001   Final
          1.1 Add G1T package
          1.2 Remove 'Hi-Reliability Product' Title

Rev 10   Change (Pg. 1, 2, 3, 4, 7, 8, 9, 10, 11)   August 2002   Final
          1.1 Remove G2T package
          1.2 Add G2U package
          1.3 Remove 'Package to be Developed' note for G4T

Rev 11   Change (Pg. 1,2,4,8,10,11,13)   February 2002   Final
          1.1 Change G1U package status to Not Recommended For New Designs

Rev 12   Change (Pg. 1,2,3,7,8,10,11,13)   May 2003   Final
          1.1 Add G2L package