

K1602T Series

14 DIP, 5.0 Volt, CMOS/TTL, TCXO



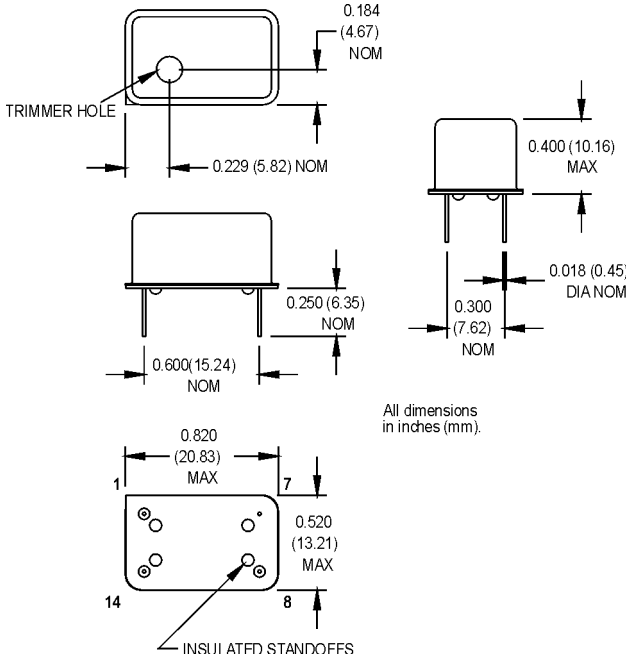
- Former **Champion TECHNOLOGIES, INC.** Product
- Phase-Locked Loops, SONET, Reference Signal, Signal Tracking, ATM

Ordering Information

00.0000
MHz

K1602T -R

Product Series _____
 RoHS Compliance _____
 Blank: non-RoHS compliant part
 -R: RoHS compliant part
 Frequency (customer specified) _____



Pin Connections

PIN	FUNCTION
1	N/C
7	Ground/Case Ground
8	Output
14	+Vdd

	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Electrical Specifications	Frequency Range	F	2		30	MHz		
	Operating Temperature	T _A	-40		+85	°C		
	Storage Temperature	T _S	-40		+85	°C		
	Initial Calibration		-1.5		+1.5	ppm	See Note 1	
	Stability vs. Temperature		-2.0		+2.0	ppm		
	Aging (10 Year)		-2		+2	ppm		
	Manual Adjusted Tuning Range		-5		+5	ppm		
	Input Voltage	V _{dd}	4.75	5.0	5.25	V		
	Input Current	I _{dd}			20	mA		
	Output Type						HCMOS/TTL	
	Load						5 TTL or 15 pF HCMOS	
	Symmetry (Duty Cycle)						See Note 3	
	< 14 MHz			45		55	%	
	≥ 14 MHz			40		60	%	
	Environmental	Logic "1" Level	V _{oh}	4.5			V	
Logic "0" Level		V _{ol}			0.5	V		
Rise Time		T _r		3.5	9.0	ns		
Fall Time		T _f		2.0	8.0	ns		
Start Up Time					20	ms		
Phase Noise (typical)							Offset from carrier	
@ 20 MHz			10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	
			-80	-108	-125	-132	-155	dBc/Hz
Mechanical Shock			Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)					
Vibration			Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)					
Hermeticity		Per MIL-STD-202, Method 112, (1x10 ⁻⁸ atm. cc/s of Helium)						
Thermal Cycle		Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)						
Solderability		Per EIAJ-STD-002						
Soldering Conditions		+240°C max. for 10 secs.						

1. Initial Calibration guaranteed at time of shipment.
2. TTL Load – see load circuit diagram #1. HCMOS load – see load circuit diagram #2.
3. Symmetry is measured at 1.4 V with TTL load, and at 50% V_{dd} with HCMOS load.

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