ZXLD1366

HIGH ACCURACY 1A, 60V LED DRIVER WITH AEC-Q100

Description

The ZXLD1366 is a continuous mode inductive step-down converter, designed for driving single or multiple series connected LEDs efficiently from a voltage source higher than the LED voltage. The device operates from an input supply between 6V and 60V and provides an externally adjustable output current of up to 1A.

The ZXLD1366 has been qualified to AECQ100 Grade 1 enabling operation in ambient temperatures from -40°C to +125°C

The ZXLD1366 uses a high-side output current sensing circuit which uses an external resistor to set the nominal average output current. The output current can be adjusted above, or below the set value, by applying an external control signal to the 'ADJ' pin. Enhanced output current dimming resolution can be achieved by applying a PWM signal to the 'ADJ' pin.

Soft-start can be forced using an external capacitor from the ADJ pin to ground. Applying a voltage of 0.2V or lower to the ADJ pin turns the output off and switches the device into a low current standby state.

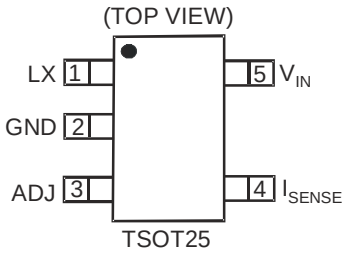
Features

- Typically better than 0.8% output current accuracy
- Simple and with low part count
- Single pin on/off and brightness control using DC voltage or PWM
- PWM resolution up to 1000:1
- High efficiency (up to 97%)
- Switching frequencies up to 1MHz
- Wide input voltage range: 6V to 60V
- Inherent open-circuit LED protection
- Available in thermally enhanced Green molding packages
  - SO-8EP θ_{JA} = +45°C/W
  - V-DFN3030-6 θ_{JA} = +44°C/W
  - TSOT25 θ_{JA} = +82°C/W
  - **Totally Lead-free & Fully RoHS Compliant (Notes 1 & 2)**
  - **Halogen and Antimony Free. "Green" Device (Note 3)**
- Qualified to AEC-Q100 Grade 1
  - SO-8EP ZXLD1366EN8TC
  - TSOT25 ZXLD1366ET5TA

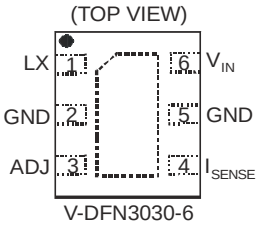
Applications

- Automotive lighting
- Low voltage industrial lighting
- LED back-up lighting
- Illuminated signs
- Emergency lighting
- SELV lighting
- Refrigeration lights

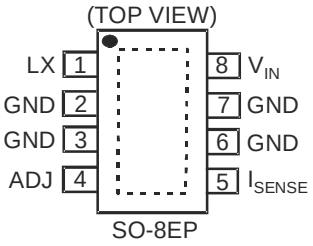
Pin Assignments



TSOT25

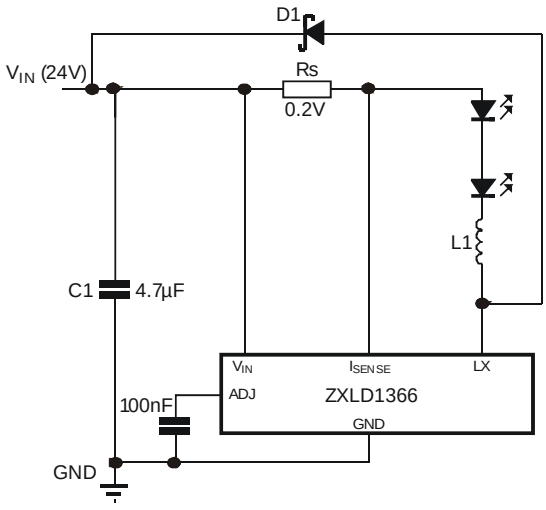


V-DFN3030-6



SO-8EP

Typical Application Circuit



Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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Block Diagram

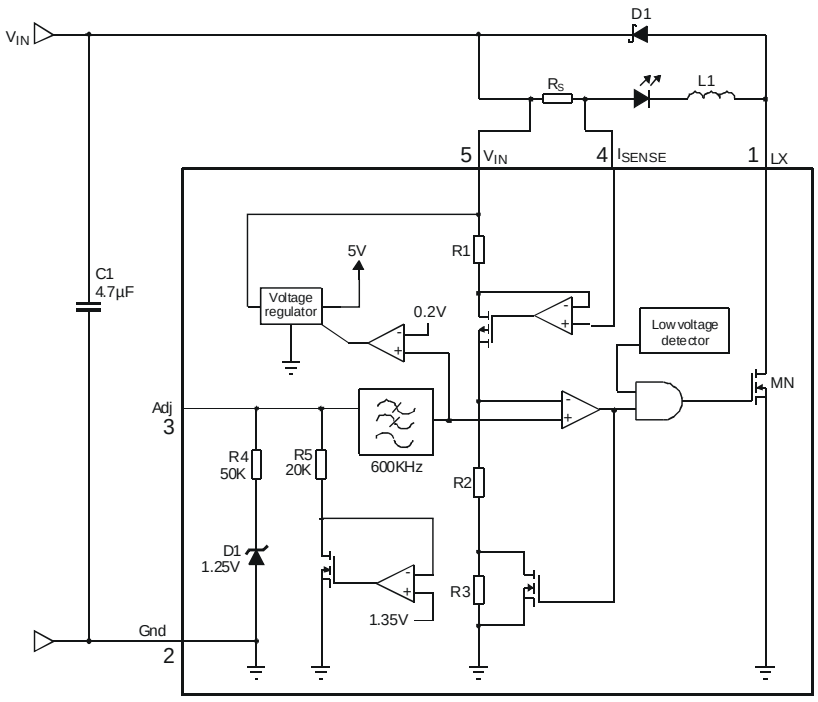

Figure. 1 Pin Connection for TSOT25 Package

Pin Description

Name	TSOT25	V-DFN3030-6	SO-8EP	Function
LX	1	1	1	Drain of NDMOS switch
GND	2	2, 5	2, 3, 6, 7	Ground (0V)
ADJ	3	3	4	Multi-function On/Off and brightness control pin: • Leave floating for normal operation.(V_{ADJ} = V_{REF} = 1.25V giving nominal average output current I_{OUTnom} = 0.2V/R_S) • Drive to voltage below 0.2V to turn off output current • Drive with DC voltage (0.3V < V_{ADJ} < 2.5V) to adjust output current from 25% to 200% of I_{OUTnom} • Connect a capacitor from this pin to ground to set soft-start time. Soft start time increases approximately 0.2ms/nF
I_{SENSE}	4	4	5	Connect resistor RS from this pin to VIN to define nominal average output current I_{OUTnom} = 0.2V/R_S. (Note: R_{SMIN} = 0.2V with ADJ pin open-circuit)
V_{IN}	5	6	8	Input Voltage (6V to 60V). Decouple to ground with 4.7µF of higher X7R ceramic capacitor close to device.
Pad	-	Pad	Pad	Exposed Pad (EP) - connected to device substrate. To improve thermal impedance of package the EP must be connected to power ground but should not be used as the 0V (GND) current path. It can be left floating but must not be connected to any other voltage other than 0V.

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Absolute Maximum Ratings (Note 4)

Symbol	Parameter		Rating	Unit
V_{IN}	Input Voltage		-0.3 to +65	V
V_{SENSE}	I_{SENSE} Voltage (Note 5)		+0.3 to -5	V
V_{LX}	LX Output Voltage		-0.3 to +65	V
V_{ADJ}	Adjust Pin Input Voltage		-0.3 to +6	V
I_{LX}	Switch Output Current		1.25	A
P_{TOT}	Power Dissipation (Refer to Package thermal de-rating curve on page 25)	TSOT25	1	W
		V-DFN3030-6	1.8	
		SO-8EP	2.2	
T_{OP}	Operating Temperature		-40 to +125	°C
T_{ST}	Storage Temperature		-55 to +150	°C
$T_{J\ MAX}$	Junction Temperature		+150	°C

Note: 4 All voltages unless otherwise stated are measured with respect to GND.
5. V_{SENSE} is measured with respect to V_{IN}.

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at conditions between maximum recommended operating conditions and absolute maximum ratings is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

ESD Susceptibility	Rating	Unit
Human Body Model	500	V
Machine Model	75	V

Caution: Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.
The human body model is a 100pF capacitor discharge through a 1.5kΩ resistor pin. The machine model is a 200pF capacitor discharged directly into each pin.

Thermal Resistance

Symbol	Parameter	Rating			Unit
		TSOT25	SO-8EP	V-DFN3030-6	
θ_{JA}	Junction to Ambient	82	45	44	°C/W
Ψ_{JB}	Junction to Board	33	—	—	
θ_{JC}	Junction to Case	—	7	14	

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{IN}	Input voltage (Note 6)	6	60	V
I_{LX}	Maximum recommended continuous/RMS switch current		1	A
V_{ADJ}	External control voltage range on ADJ pin for DC brightness control (Note 7)	0.3	2.5	V
V_{ADJOFF}	DC voltage on ADJ pin to ensure devices is off		0.25	V
t_{OFFMIN}	Minimum switch off-time		800	ns
t_{ONMIN}	Minimum switch on-time		800	ns
$f_{LX\ MAX}$	Recommended maximum operating frequency (Note 8)		625	kHz
D_{LX}	Duty cycle range	0.01	0.99	
$D_{LX(LIMIT)}$	Recommended duty cycle range of output switch at f_{LXMAX}	0.3	0.7	
T_{OP}	Operating Temperature range	-40	+125	°C

Notes: 6. V_{IN} > 16V to fully enhance output transistor. Otherwise out current must be derated - see graphs. Operation at low supply may cause excessive heating due to increased on-resistance. Tested at 7V guaranteed for 6V by design.
7. 100% brightness corresponds to $V_{ADJ} = V_{ADJ(nom)} = V_{REF}$. Driving the ADJ pin above V_{REF} will increase the V_{SENSE} threshold and output current proportionally.
8. ZXLD1366 will operate at higher frequencies but accuracy will be affected due to propagation delays.

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Electrical Characteristics (Test conditions: V_{IN} = 24V, T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SU}	Internal regulator start-up threshold			4.85	5.20	V
V_{SD}	Internal regulator shutdown threshold		4.40	4.75		V
I_{INQoff}	Quiescent supply current with output off	ADJ pin grounded		65	108	µA
I_{INQon}	Quiescent supply current with output switching (Note 9)	ADJ pin floating, L = 68µH, 3 LEDs, f = 260kHz		1.6		mA
V_{SENSE}	Mean current sense threshold voltage (Defines LED current setting accuracy)	Measured on I_{SENSE} pin with respect to V_{IN} V_{ADJ} = 1.25V; V_{IN} = 18V	195	200	205	mV
$V_{SENSEHYS}$	Sense threshold hysteresis			±15		%
I_{SENSE}	I_{SENSE} pin input current	V_{SENSE} = V_{IN} -0.2		4	10	µA
V_{REF}	Internal reference voltage	Measured on ADJ pin with pin floating		1.25		V
$\Delta V_{REF}/\Delta T$	Temperature coefficient of V_{REF}			50		ppm/°C
V_{ADJ}	External control voltage range on ADJ pin for DC brightness control (Note 7)		0.3		2.5	V
V_{ADJoff}	DC voltage on ADJ pin to switch device from active (on) state to quiescent (off) state	V_{ADJ} falling	0.15	0.20	0.27	V
V_{ADJon}	DC voltage on ADJ pin to switch device from quiescent (off) state to active (on) state	V_{ADJ} rising	0.20	0.25	0.30	V
R_{ADJ}	Resistance between ADJ pin and V_{REF}	0 < V_{ADJ} < V_{REF} V_{ADJ} > V_{REF} +100mV	30 10.4	50 14.2	65 18.0	kΩ
I_{LXmean}	Continuous LX switch current				1	A
R_{LX}	LX switch 'On' resistance	@ I_{LX} = 1A		0.50	0.75	Ω
$I_{LX(leak)}$	LX switch leakage current				5	µA
$D_{PWM(LF)}$	Duty cycle range of PWM signal applied to ADJ pin during low frequency PWM dimming mode	PWM frequency < 300Hz PWM amplitude = V_{REF} Measured on ADJ pin	0.001		1.000	V
	Brightness control range			1000:1		
DC_{ADJ}	DC Brightness control range	(Note 8)		5:1		
t_{SS}	Soft start time	Time taken for output current to reach 90% of final value after voltage on ADJ pin has risen above 0.3V. Requires external capacitor 22nF. See graphs for more details		2		ms
f_{LX}	Operating frequency (See graphs for more details)	ADJ pin floating L = 68µH (0.2V) I_{OUT} = 1A @ V_{LED} = 3.6V Driving 3 LEDs		260		kHz
t_{ONmin}	Minimum switch 'ON' time	LX switch 'ON'		130		
t_{OFFmin}	Minimum switch 'OFF' time	LX switch 'OFF'		70		

Notes:
9. Static current of device is approximately 700 µA, see Graph, Page 16
10. 100% brightness corresponds to V_{ADJ} = $V_{ADJ(nom)}$ = V_{REF}. Driving the ADJ pin above V_{REF} will increase the V_{SENSE} threshold and output current proportionally.
11. Ratio of maximum brightness to minimum brightness before shutdown V_{REF} = 1.25/0.3. V_{REF} externally driven to 2.5V, ratio 10:1.

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Device Description

The device, in conjunction with the coil (L1) and current sense resistor (R_S), forms a self-oscillating continuous-mode buck converter.

Device Operation

(refer to Figure 1 - Block diagram and Figure 2 Operating waveforms).

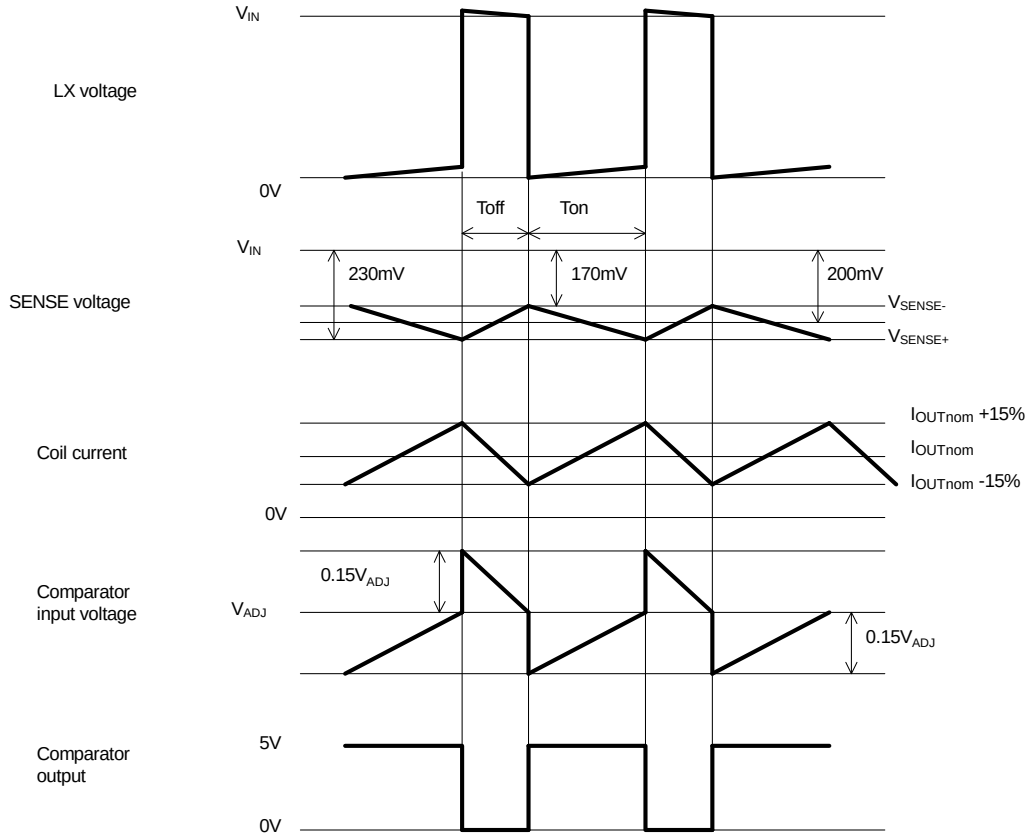

Figure 2. Theoretical Operating Waveforms

Operation can be best understood by assuming that the ADJ pin of the device is unconnected and the voltage on this pin (V_{ADJ}) appears directly at the (+) input of the comparator.

When input voltage V_{IN} is first applied, the initial current in L1 and R_S is zero and there is no output from the current sense circuit. Under this condition, the (-) input to the comparator is at ground and its output is high. This turns MN on and switches the LX pin low, causing current to flow from V_{IN} to ground, via R_S, L1 and the LED(s). The current rises at a rate determined by V_{IN} and L1 to produce a voltage ramp (V_{SENSE}) across R_S. The supply referred voltage V_{SENSE} is forced across internal resistor R1 by the current sense circuit and produces a proportional current in internal resistors R2 and R3. This produces a ground referred rising voltage at the (-) input of the comparator. When this reaches the threshold voltage (V_{ADJ}), the comparator output switches low and MN turns off. The comparator output also drives another NMOS switch, which bypasses internal resistor R3 to provide a controlled amount of hysteresis. The hysteresis is set by R3 to be nominally 15% of V_{ADJ}.

When MN is off, the current in L1 continues to flow via D1 and the LED(s) back to V_{IN}. The current decays at a rate determined by the LED(s) and diode forward voltages to produce a falling voltage at the input of the comparator. When this voltage returns to V_{ADJ}, the comparator output switches high again. This cycle of events repeats, with the comparator input ramping between limits of V_{ADJ} ± 15%.

Switching Thresholds

With $V_{ADJ} = V_{REF}$, the ratios of R1, R2 and R3 define an average V_{SENSE} switching threshold of 200mV (measured on the I_{SENSE} pin with respect to V_{IN}). The average output current I_{OUTnom} is then defined by this voltage and R_S according to:

$I_{OUTnom} = 200mV/R_S$

Nominal ripple current is $\pm 30mV/R_S$

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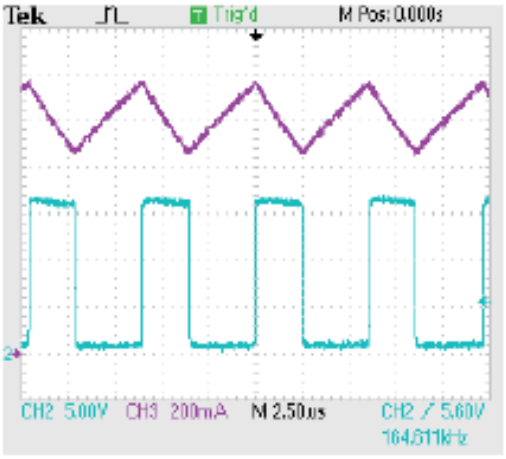
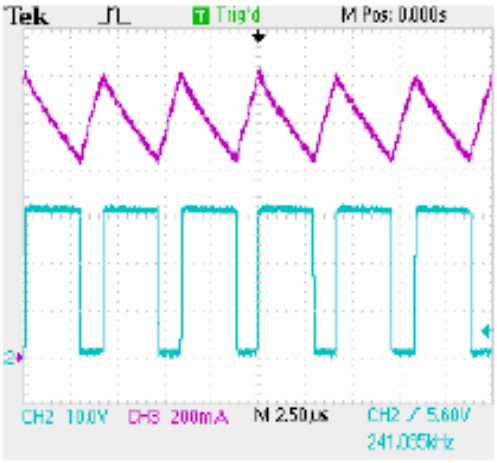
Device Description (cont.)

Actual operating waveforms

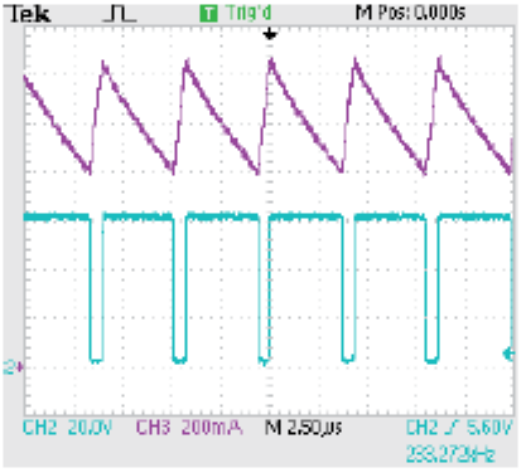
V_{IN} = 15V, R_S = 0.2Ω, L = 68µH Normal operation. Output Current (Ch 3) and LX voltage (Ch 2)



V_{IN} = 30V, R_S = 0.2Ω, L = 68µH Normal operation. Output Current (Ch 3) and LX voltage (Ch 2)



V_{IN} = 60V, R_S = 0.2Ω, L = 68µH Normal operation. Output Current (Ch 3) and LX voltage (Ch 2)



Adjusting Output Current

The device contains a low pass filter between the ADJ pin and the threshold comparator and an internal current limiting resistor (50kΩ nom) between ADJ and the internal reference voltage. This allows the ADJ pin to be overdriven with either DC or pulse signals to change the V_{SENSE} switching threshold and adjust the output current.

Details of the different modes of adjusting output current are given in the applications section.

Output Shutdown

The output of the low pass filter drives the shutdown circuit. When the input voltage to this circuit falls below the threshold (0.2V nom.), the internal regulator and the output switch are turned off. The voltage reference remains powered during shutdown to provide the bias current for the shutdown circuit. Quiescent supply current during shutdown is nominally 60µA and switch leakage is below 5µA.

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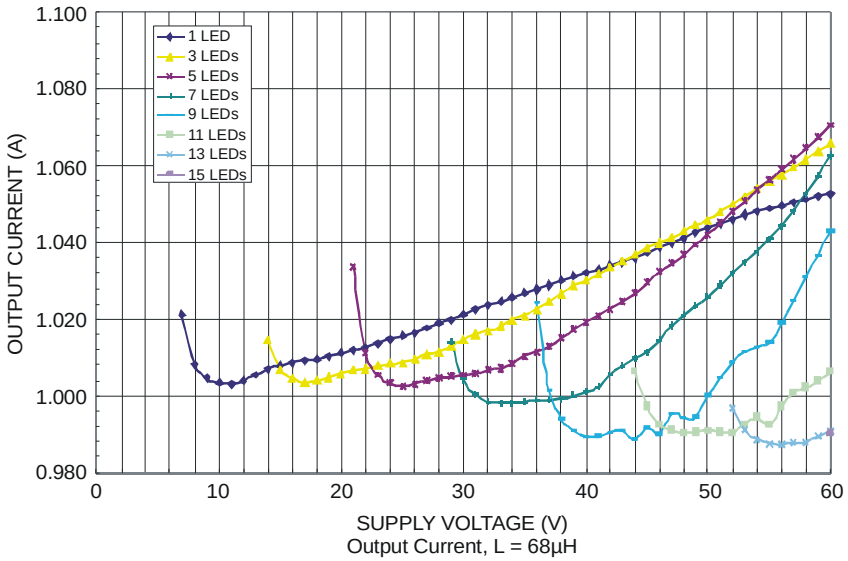
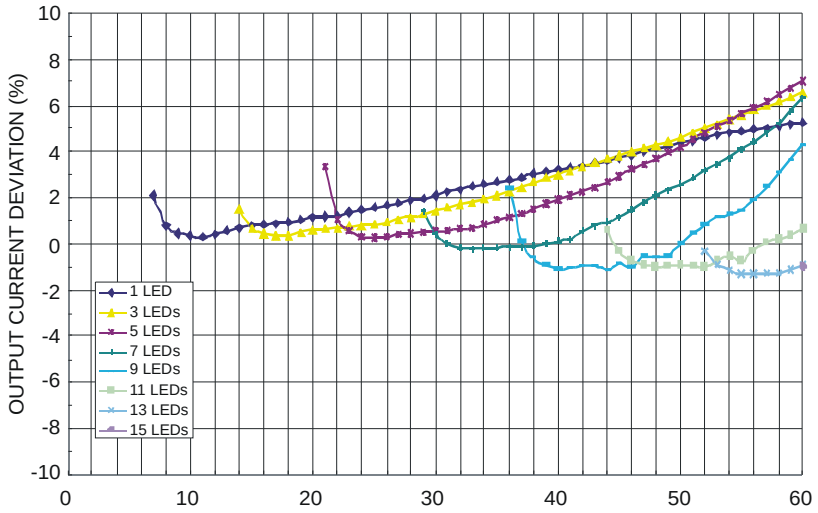
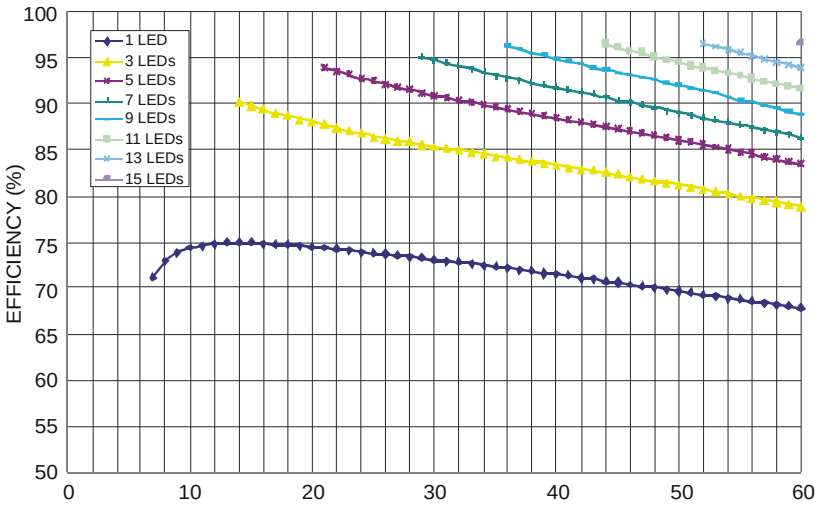
Typical Operating Conditions



Output Current, L = 68µH



Output Current Deviation, L = 68µH



Efficiency, L = 68µH

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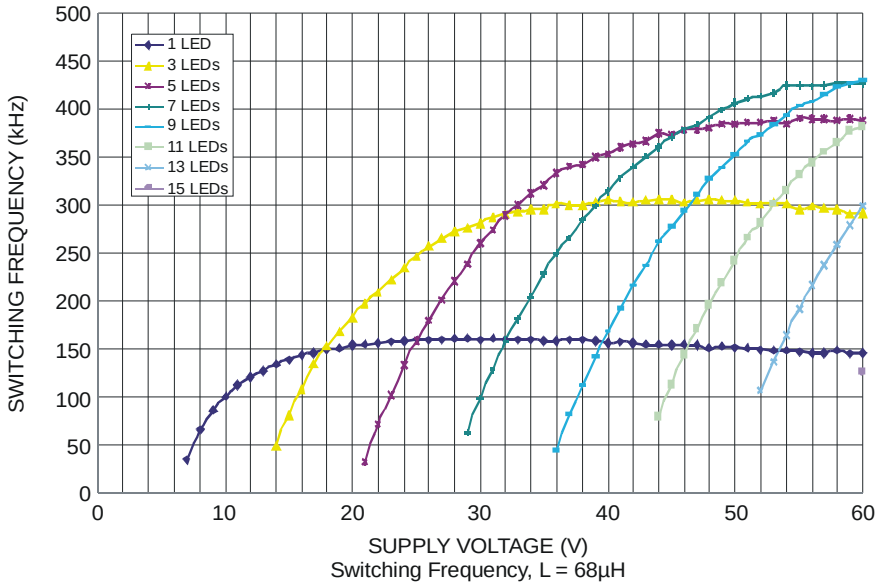
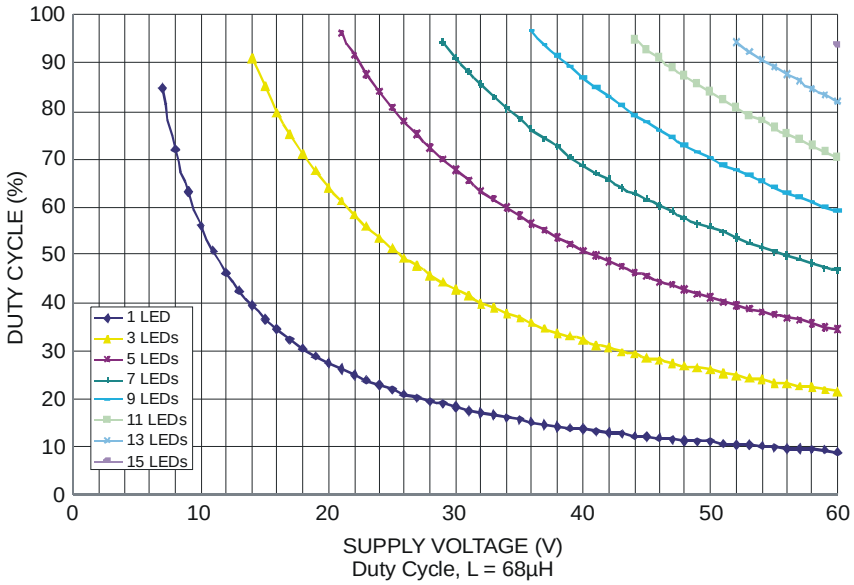
Typical Operating Conditions (cont.)



Switching Frequency, L = 68µH



Duty Cycle, L = 68µH

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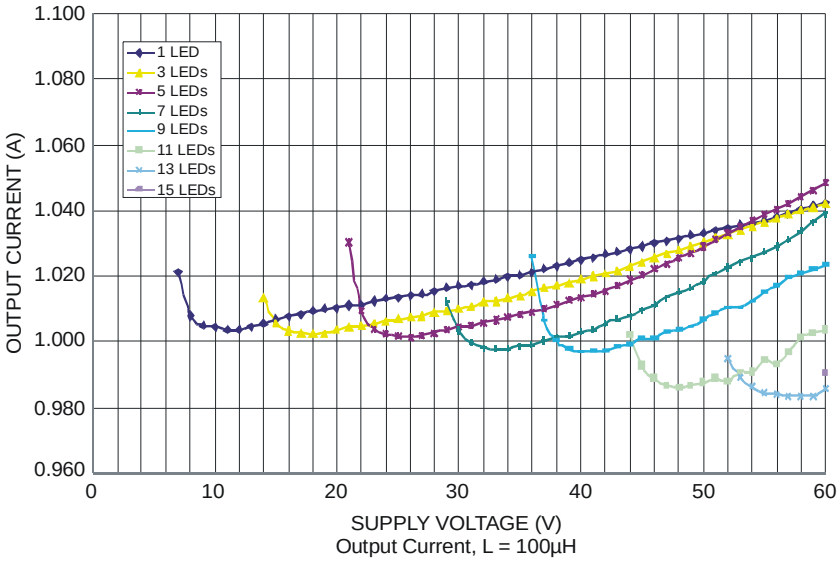
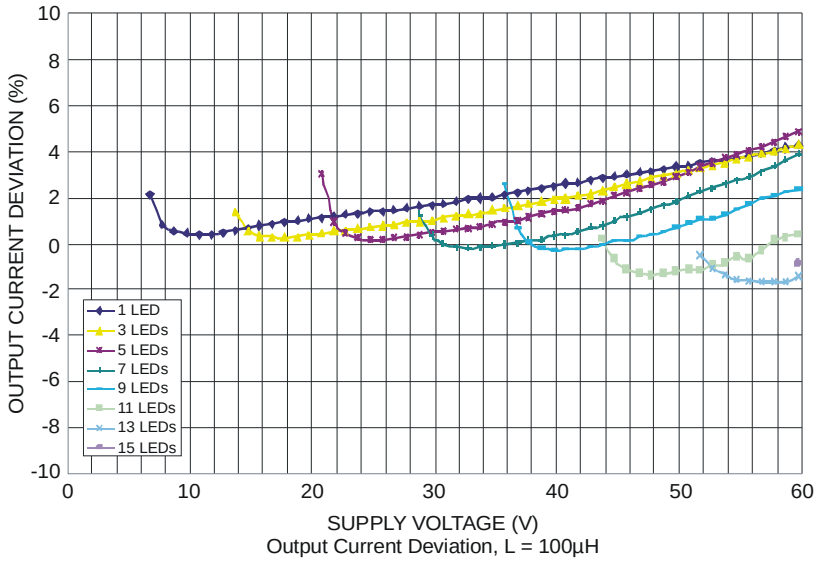
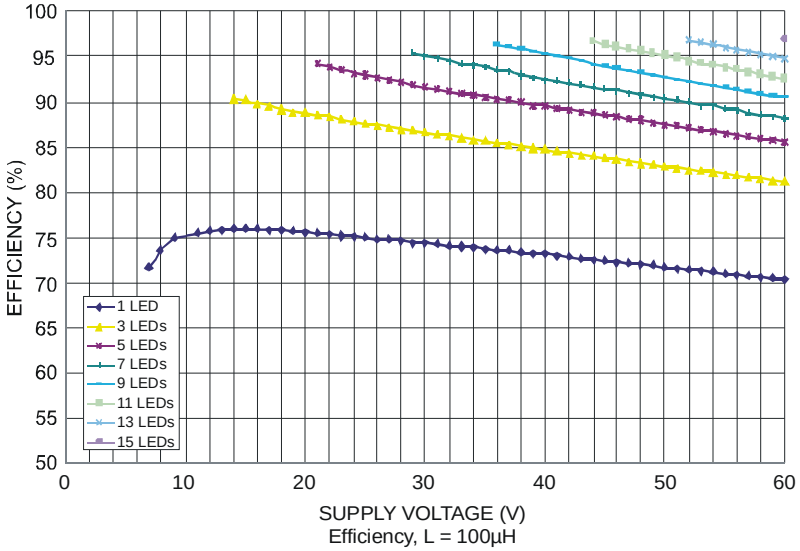
Typical Operating Conditions (cont.)



Output Current, L = 100µH



Output Current Deviation, L = 100µH



Efficiency, L = 100µH

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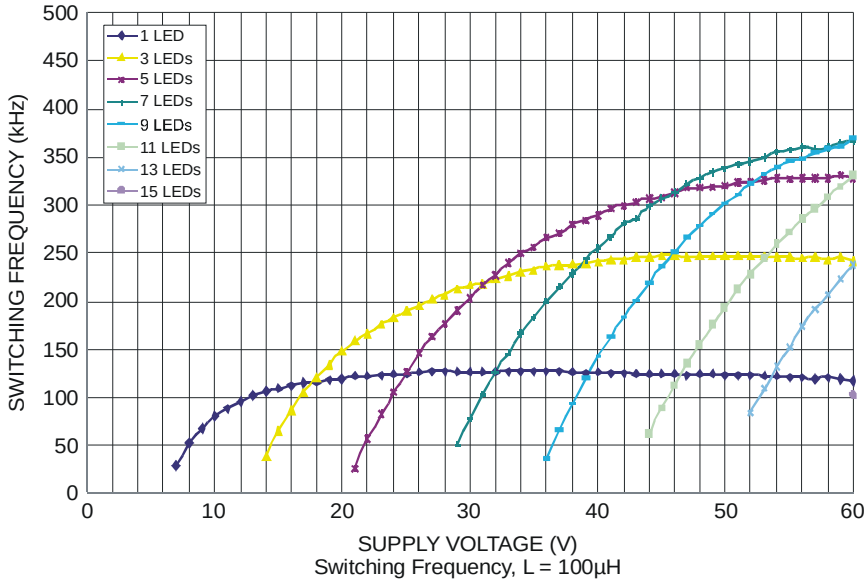
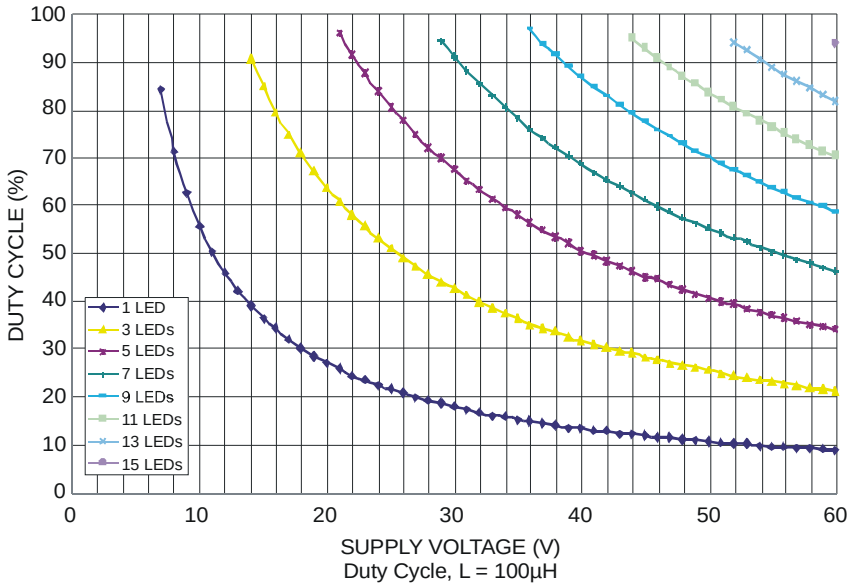
Typical Operating Conditions (cont.)



Switching Frequency, L = 100µH



Duty Cycle, L = 100µH

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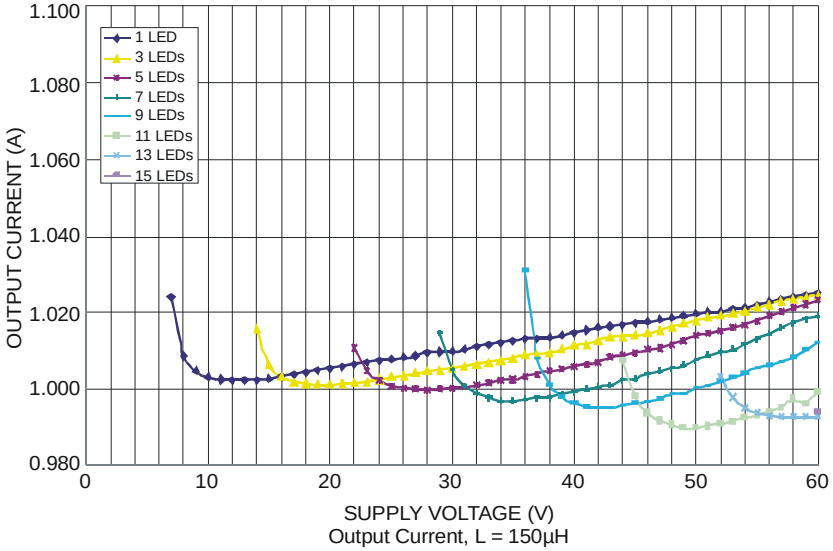
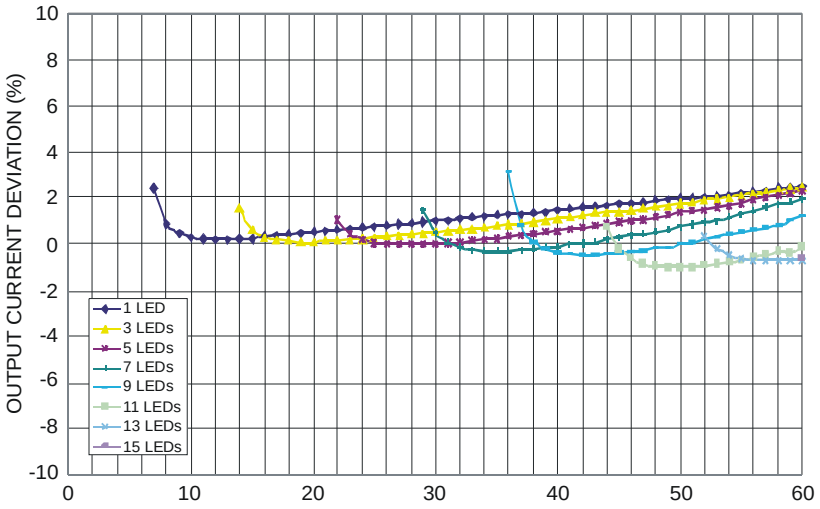
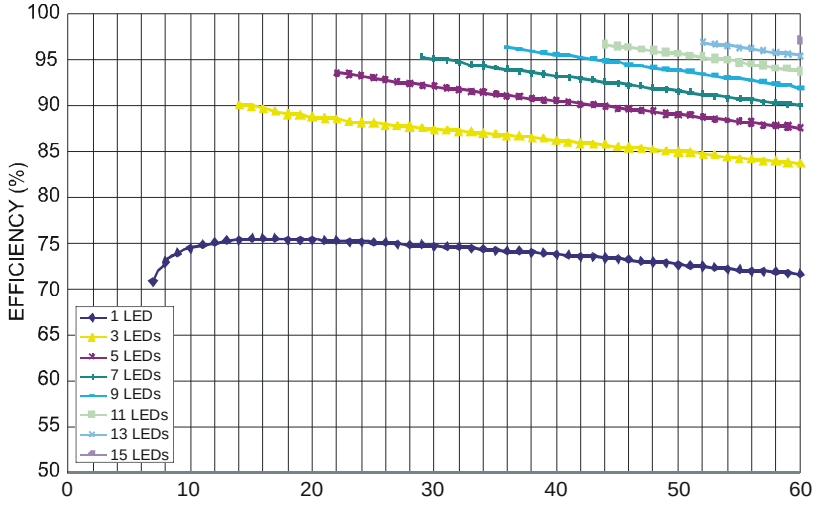
Typical Operating Conditions (cont.)



Output Current, L = 150µH



Output Current Deviation, L = 150µH



Efficiency, L = 150µH

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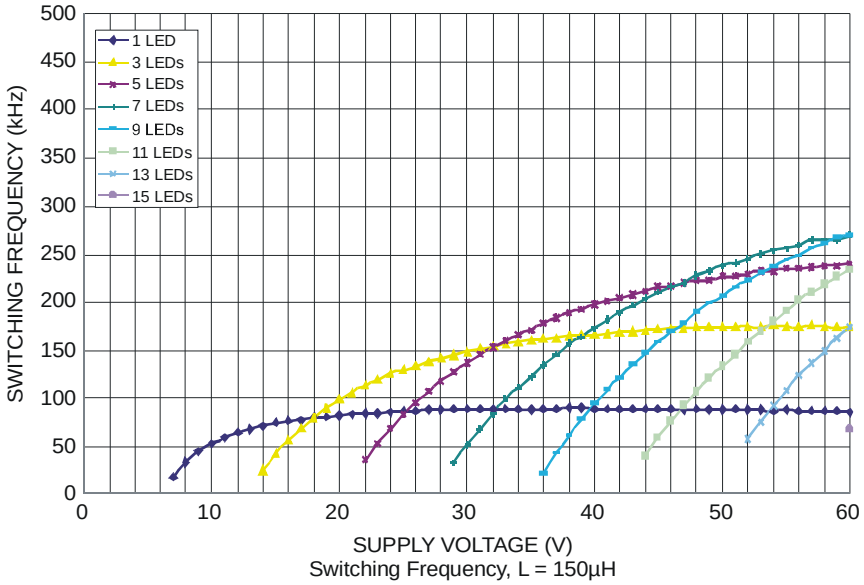
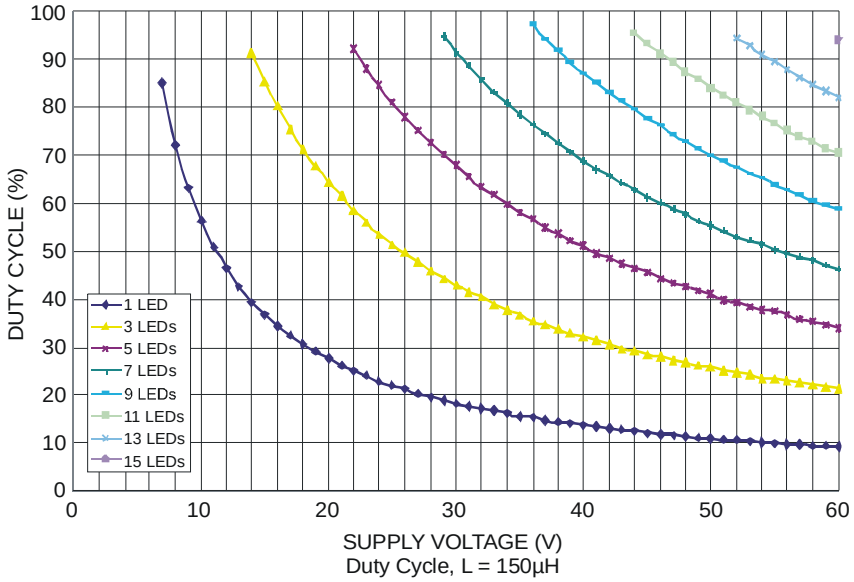
Typical Operating Conditions (cont.)



Switching Frequency, L = 150µH



Duty Cycle, L = 150µH

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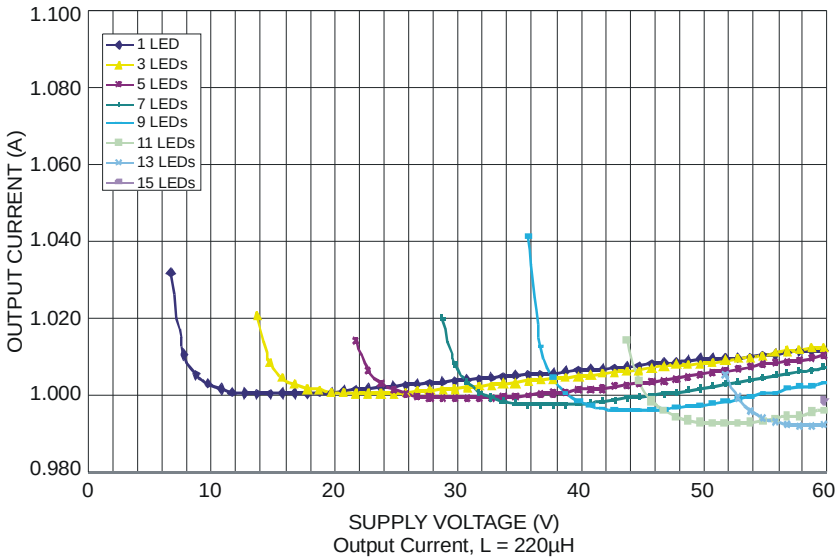
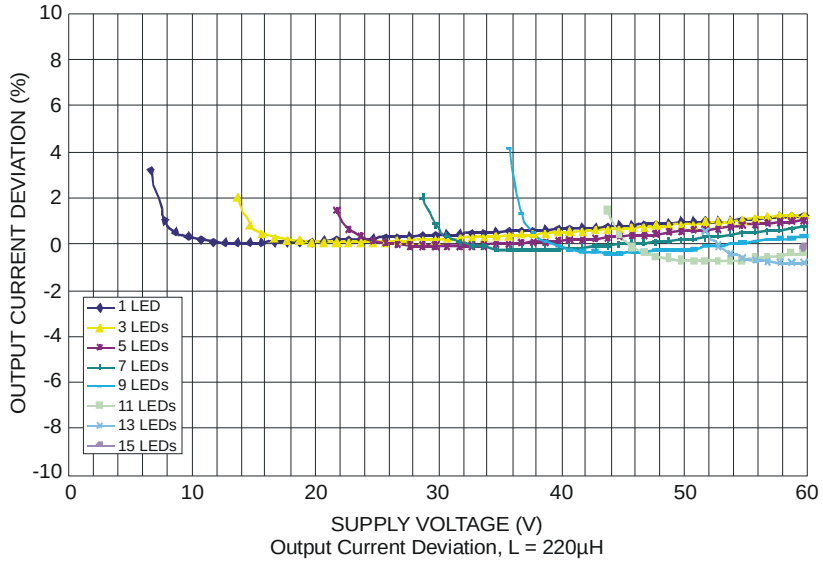
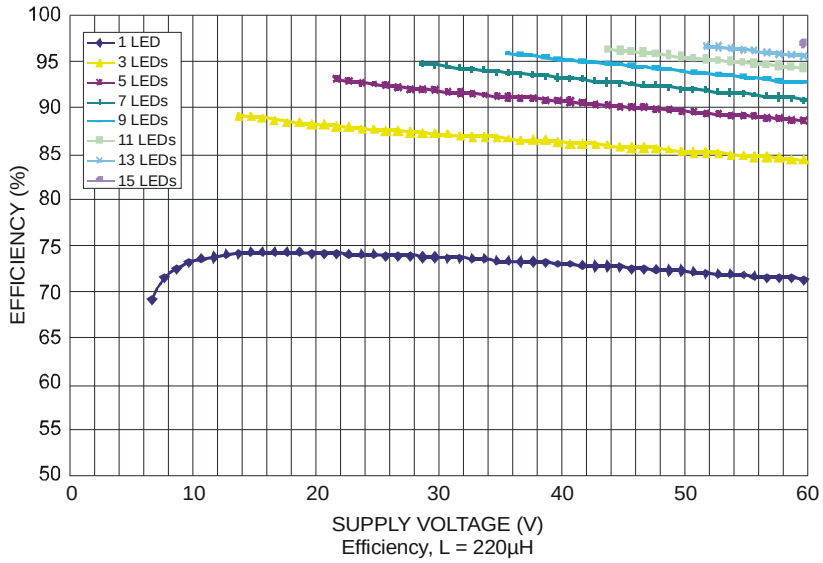
Typical Operating Conditions (cont.)



Output Current, L = 220µH



Output Current Deviation, L = 220µH



Efficiency, L = 220µH

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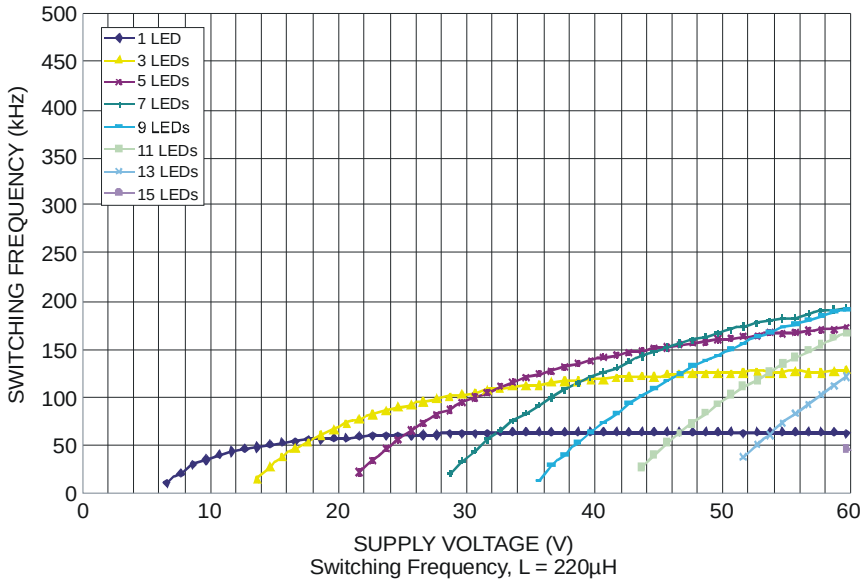
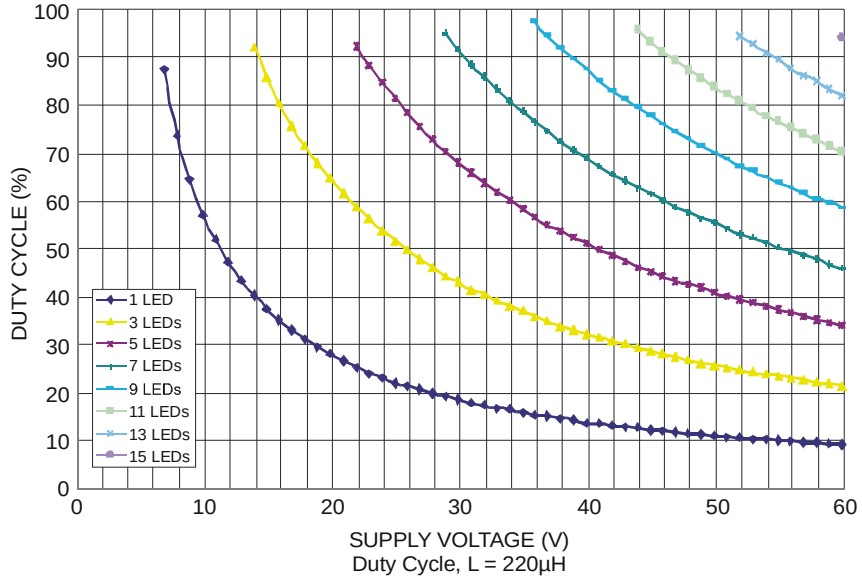
Typical Operating Conditions (cont.)



Switching Frequency, L = 220µH



Duty Cycle, L = 220µH

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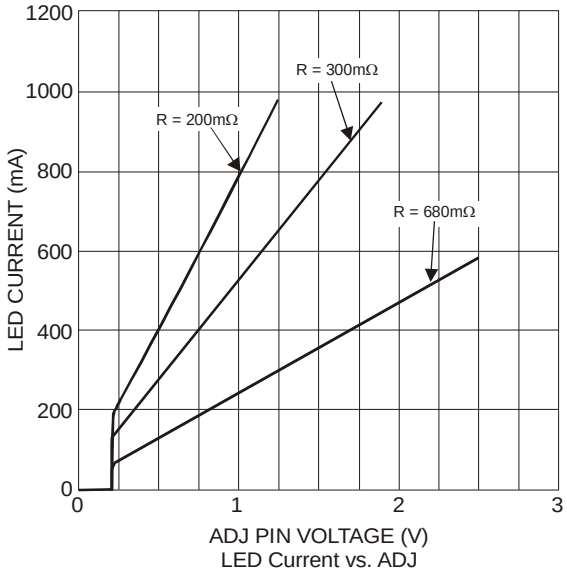
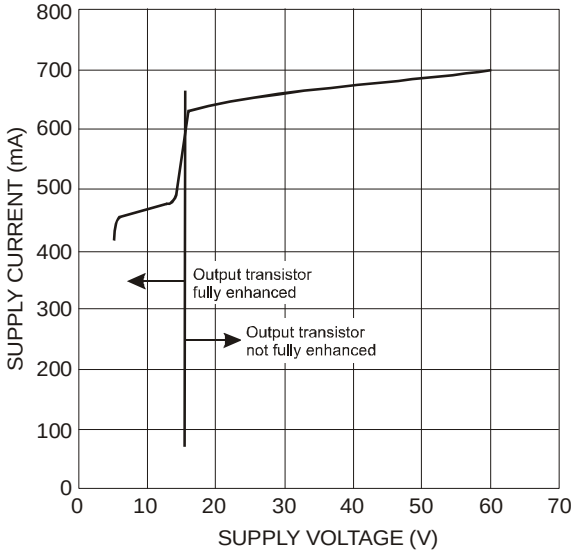
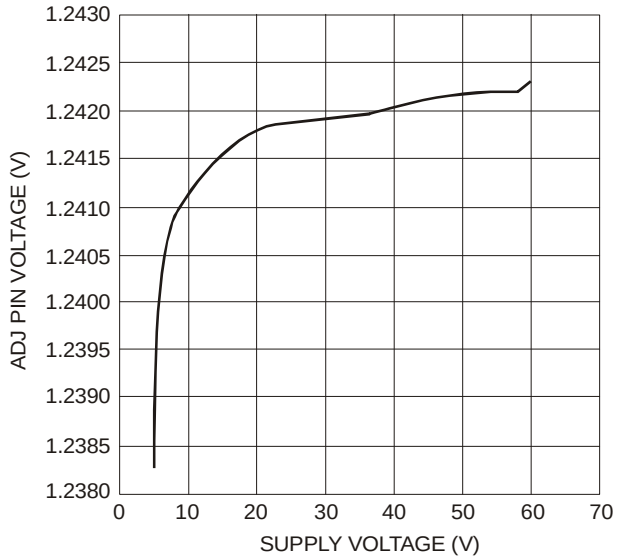
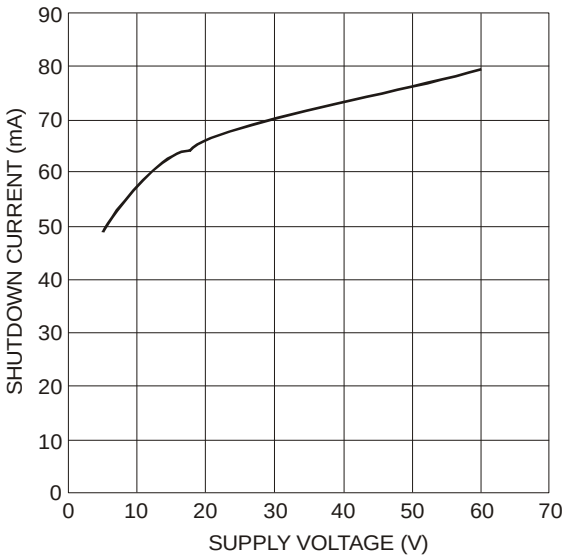
Typical Operating Conditions (cont.)



LED Current vs. ADJ







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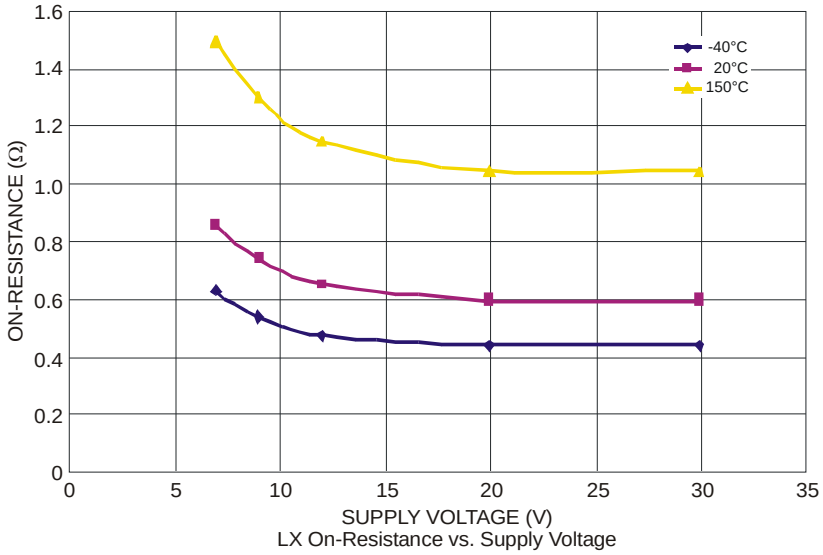
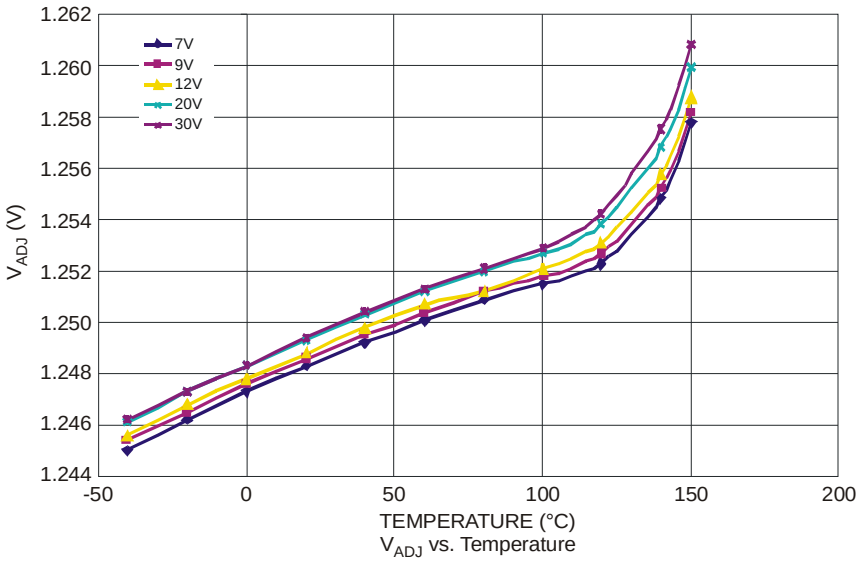
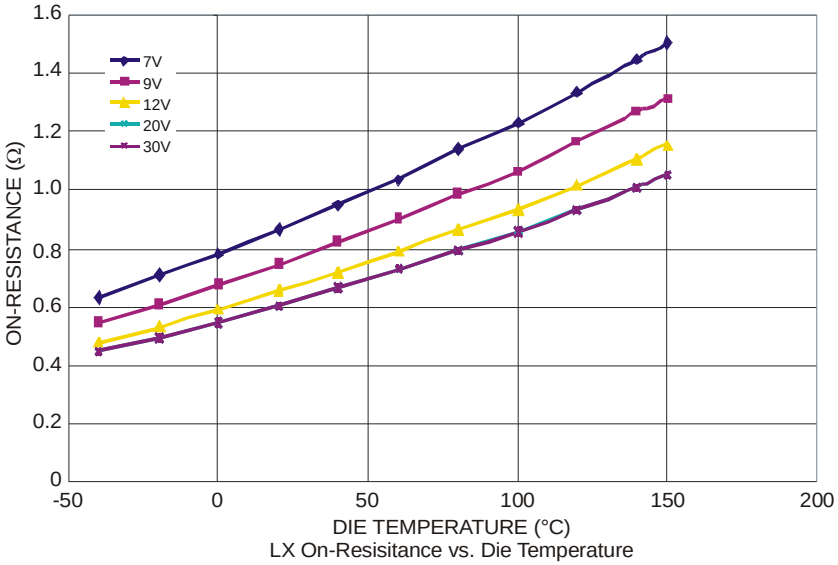
Typical Operating Conditions (cont.)



LX On-Resistance vs. Supply Voltage



V_{ADJ} vs. Temperature



LX On-Resisitance vs. Die Temperature

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Application Information

Setting Nominal Average Output Current with External Resistor R_S

The nominal average output current in the LED(s) is determined by the value of the external current sense resistor (R_S) connected between V_{IN} and I_{SENSE} and is given by:

$I_{OUTnom} = 0.2/R_S$ for $R_S \geq 0.2\Omega$

The table below gives values of nominal average output current for several preferred values of current setting resistor (R_S) in the typical application circuit shown on page 1:

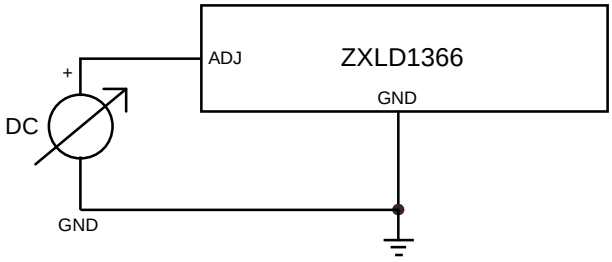
R_S (Ω)	Nominal Average Output Current (mA)
0.20	1000
0.27	740
0.56	357

The above values assume that the ADJ pin is floating and at a nominal voltage of V_{REF} (= 1.25V). Note that R_S = 0.2Ω is the minimum allowed value of sense resistor under these conditions to maintain switch current below the specified maximum value.

It is possible to use different values of R_S if the ADJ pin is driven from an external voltage. (See next section).

Output Current Adjustment by External DC Control Voltage

The ADJ pin can be driven by an external dc voltage (V_{ADJ}), as shown, to adjust the output current to a value above or below the nominal average value defined by R_S.



The nominal average output current in this case is given by:

$I_{OUTdc} = (V_{ADJ} /1.25) \times (0.2/R_S)$ for $0.3 < V_{ADJ} < 2.5V$

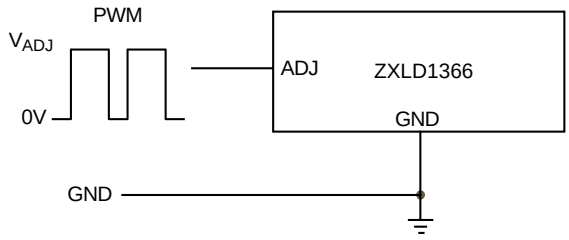
Note that 100% brightness setting corresponds to $V_{ADJ} = V_{REF}$. When driving the ADJ pin above 1.25V, R_S must be increased in proportion to prevent I_{OUTdc} exceeding 1A maximum.

The input impedance of the ADJ pin is 50kΩ ±25% for voltages below V_{REF} and 14.2kΩ ±25% for voltages above V_{REF} +100mV.

Output Current Adjustment by PWM Control

Directly Driving ADJ Input

A Pulse Width Modulated (PWM) signal with duty cycle DPWM can be applied to the ADJ pin, as shown below, to adjust the output current to a value above or below the nominal average value set by resistor R_S:



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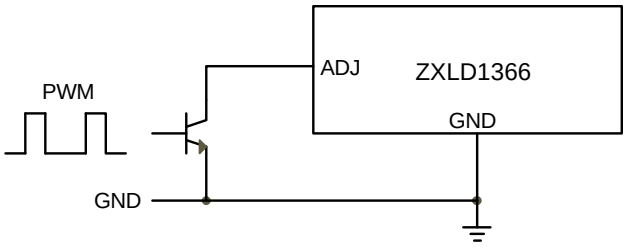
Application Information (cont.)

Driving the ADJ Input via Open Collector Transistor

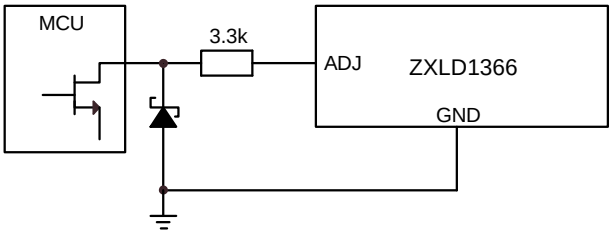
The recommended method of driving the ADJ pin and controlling the amplitude of the PWM waveform is to use a small NPN switching transistor as shown below:



This scheme uses the 50k resistor between the ADJ pin and the internal voltage reference as a pull-up resistor for the external transistor.

Driving the ADJ Input from a Microcontroller

Another possibility is to drive the device from the open drain output of a microcontroller. The diagram below shows one method of doing this:



If the NMOS transistor within the microcontroller has high Gate / Drain capacitance, this arrangement can inject a negative spike into ADJ input of the ZXLD1366 and cause erratic operation but the addition of a Schottky clamp diode (eg Diodes Inc. SD103CWS) to ground and inclusion of a series resistor (3.3k) will prevent this. See the section on PWM dimming for more details of the various modes of control using high frequency and low frequency PWM signals.

Shutdown Mode

Taking the ADJ pin to a voltage below 0.2V for more than approximately 100µs will turn off the output and supply current to a low standby level of 65µA nominal.

Note that the ADJ pin is not a logic input. Taking the ADJ pin to a voltage above V_{REF} will increase output current above the 100% nominal average value. (See page 18 graphs for details).

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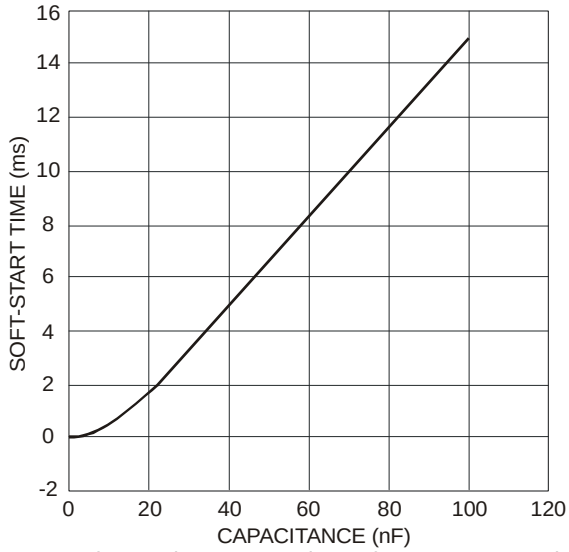
Application Information (cont.)

Soft-Start

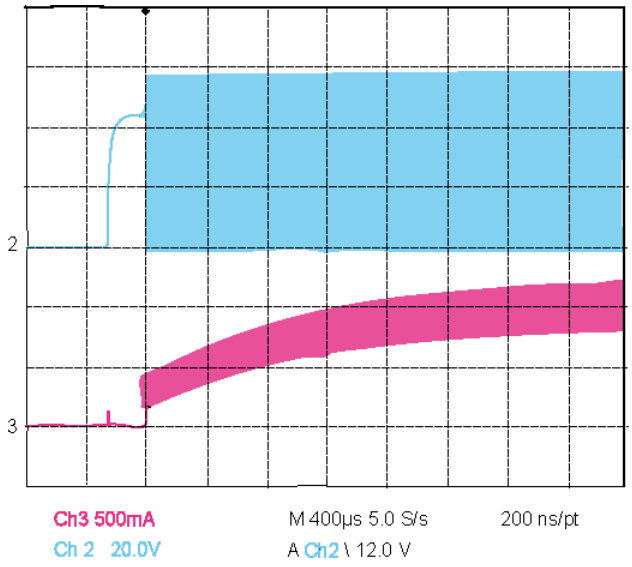
An external capacitor from the ADJ pin to ground will provide a soft-start delay, by increasing the time taken for the voltage on this pin to rise to the turn-on threshold and by slowing down the rate of rise of the control voltage at the input of the comparator. Adding capacitance increases this delay by approximately 0.2ms/nF. The graph below shows the variation of soft-start time for different values of capacitor.



Soft-Start Time vs. Capacitance form ADJ to Ground

Actual Operating Waveforms [V_{IN} = 60V, R_S = 0.2Ω, L = 68µH, 22nF on ADJ]

Soft-start operation. LX voltage (CH2) and Output current (CH3) using a 22nF external capacitor on the ADJ pin.



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Application Information (cont.)

V_{IN} Capacitor Selection

A low ESR capacitor should be used for input decoupling, as the ESR of this capacitor appears in series with the supply source impedance and lowers overall efficiency. This capacitor has to supply the relatively high peak current to the coil and smooth the current ripple on the input supply.

To avoid transients into the IC, the size of the input capacitor will depend on the V_{IN} voltage:

V_{IN} = 6 to 40V C_{IN} = 2.2µF

V_{IN} = 40 to 50V C_{IN} = 4.7µF

V_{IN} = 50 to 60V C_{IN} = 10µF

When the input voltage is close to the output voltage the input current increases which puts more demand on the input capacitor. The minimum value of 2.2µF may need to be increased to 4.7µF; higher values will improve performance at lower input voltages, especially when the source impedance is high. The input capacitor should be placed as close as possible to the IC.

For maximum stability over temperature and voltage, capacitors with X7R, X5R, or better dielectric is recommended. Capacitors with Y5V dielectric are not suitable for decoupling in this application and should **NOT** be used.

When higher voltages are used with the C_{IN} = 10µF, an electrolytic capacitor can be used provided that a suitable 1µF ceramic capacitor is also used and positioned as close to the V_{IN} pin as possible.

A suitable capacitor would be NACEW100M1006.3x8TR13F (NIC Components).

The following web sites are useful when finding alternatives:

www.murata.com
www.niccomp.com
www.kemet.com

Inductor Selection

Recommended inductor values for the ZXLD1366 are in the range 68µH to 220µH.

Higher values of inductance are recommended at higher supply voltages in order to minimize errors due to switching delays, which result in increased ripple and lower efficiency. Higher values of inductance also result in a smaller change in output current over the supply voltage range. (see graphs pages 10-17). The inductor should be mounted as close to the device as possible with low resistance connections to the LX and VIN pins.

The chosen coil should have a saturation current higher than the peak output current and a continuous current rating above the required mean output current.

Suitable coils for use with the ZXLD1366 may be selected from the MSS range manufactured by Coilcraft, or the NPIS range manufactured by NIC components. The following websites may be useful in finding suitable components.

www.coilcraft.com
www.niccomp.com
www.wuerth-elektronik.de

The inductor value should be chosen to maintain operating duty cycle and switch 'on'/'off' times within the specified limits over the supply voltage and load current range.

The graph Figure 3 below can be used to select a recommended inductor based on maintaining the ZXLD1366 case temperature below +60°C. For detailed performance characteristics for the inductor values 68, 100, 150 and 220µH see graphs on pages 10-17.

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Application Information (cont.)

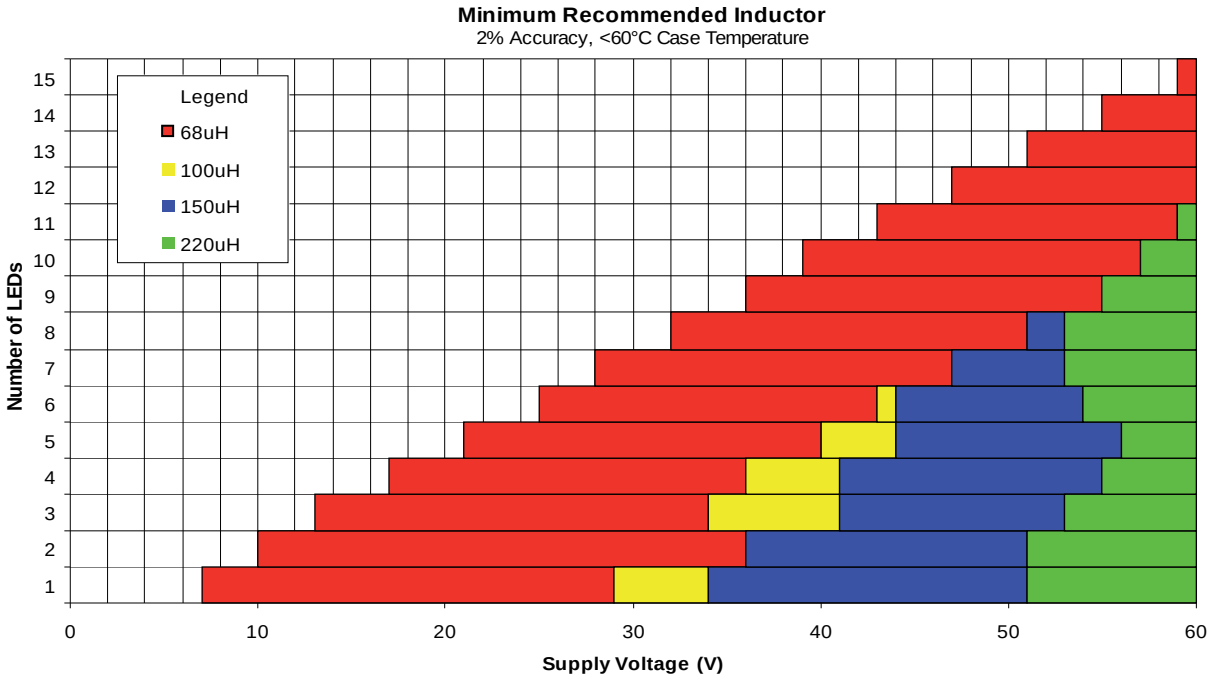

Figure. 3 ZXLD1366 Minimum Recommended Inductor (TSOT25)

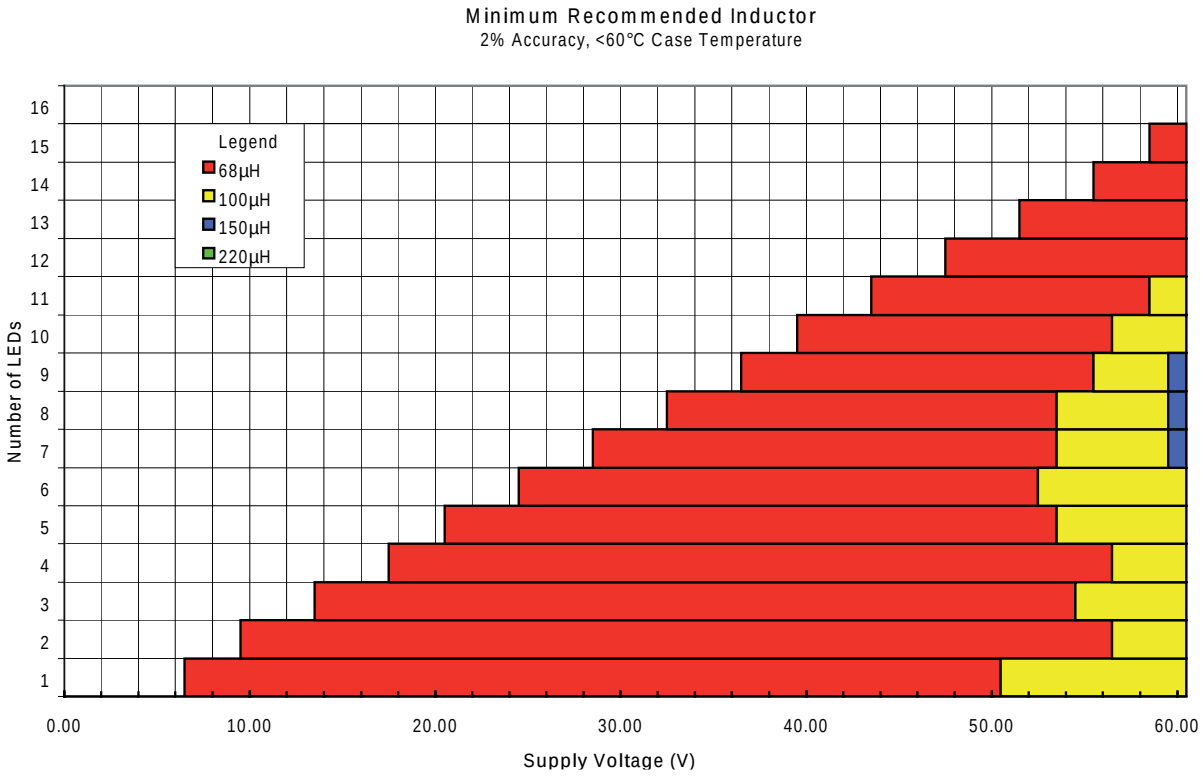

Figure. 4 ZXLD1366 Minimum Recommended Inductor (V-DFN3030-6)

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Application Information (cont.)

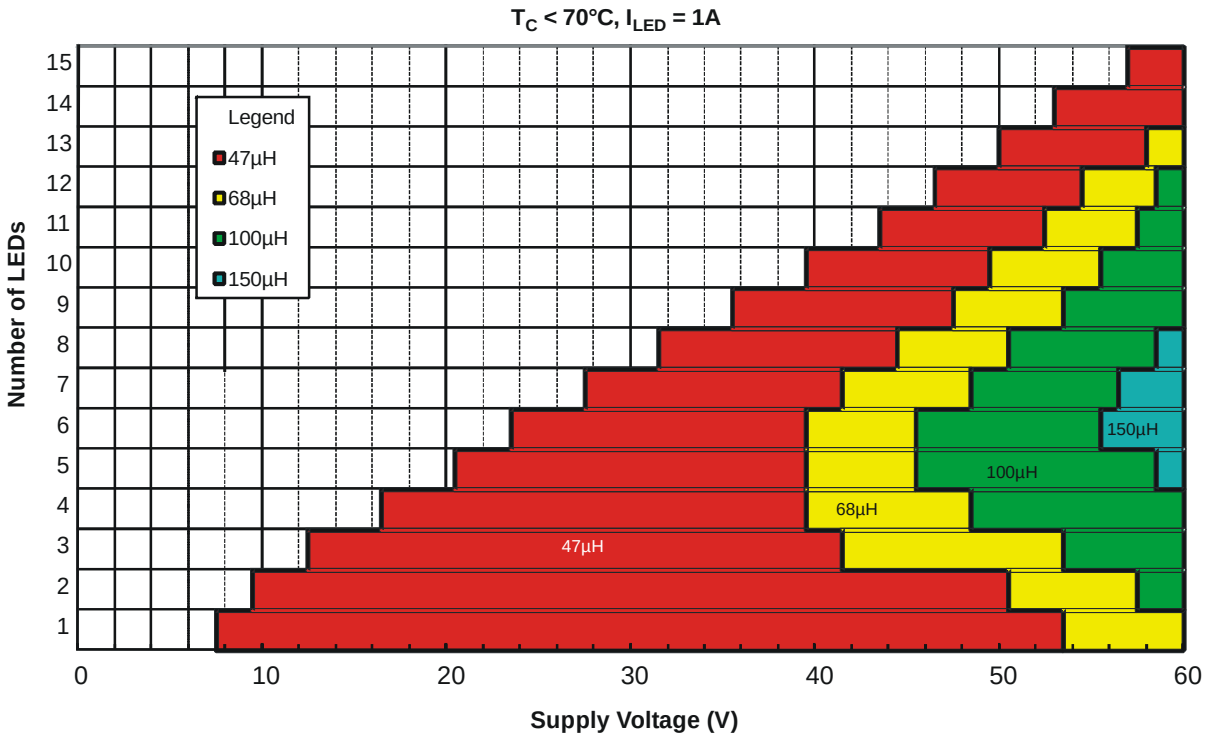

Figure. 5 ZXLD1366 Minimum Recommended Inductor (SO-8EP)

Diode Selection

For maximum efficiency and performance, the rectifier (D1) should be a fast low capacitance Schottky diode* with low reverse leakage at the maximum operating voltage and temperature.

They also provide better efficiency than silicon diodes, due to a combination of lower forward voltage and reduced recovery time.

It is important to select parts with a peak current rating above the peak coil current and a continuous current rating higher than the maximum output load current. It is very important to consider the reverse leakage of the diode when operating above 85°C. Excess leakage will increase the power dissipation in the device and if close to the load may create a thermal runaway condition.

The higher forward voltage and overshoot due to reverse recovery time in silicon diodes will increase the peak voltage on the LX output. If a silicon diode is used, care should be taken to ensure that the total voltage appearing on the LX pin including supply ripple, does not exceed the specified maximum value.

*A suitable Schottky diode would be B3100 (Diodes Inc).

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Application Information (cont.)

Reducing Output Ripple

Peak to peak ripple current in the LED(s) can be reduced, if required, by shunting a capacitor Cled across the LED(s) as shown below:

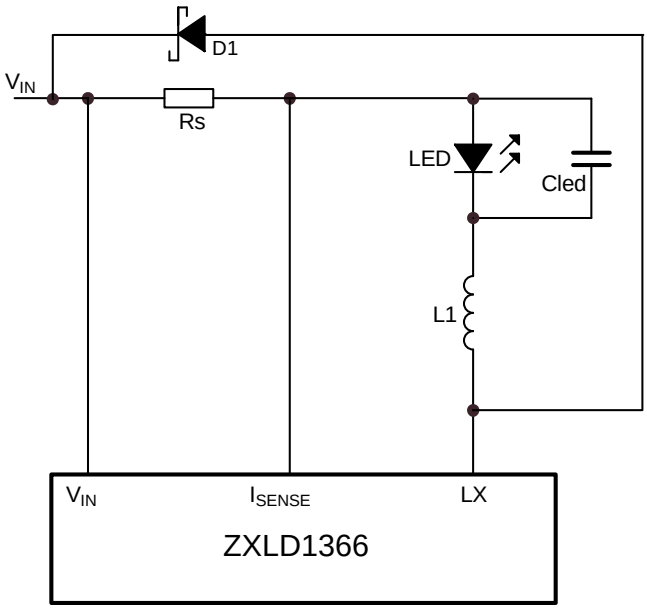

Figure. 6 Reduced Output Ripple

A value of 1µF will reduce the supply ripple current by a factor three (approx.). Proportionally lower ripple can be achieved with higher capacitor values. Note that the capacitor will not affect operating frequency or efficiency, but it will increase start-up delay, by reducing the rate of rise of LED voltage.

By adding this capacitor the current waveform through the LED(s) changes from a triangular ramp to a more sinusoidal version without altering the mean current value.

Operation at Low Supply Voltage

Below the under-voltage lockout threshold (V_{SD}) the drive to the output transistor is turned off to prevent device operation with excessive on-resistance of the output transistor. The output transistor is not full enhanced until the supply voltage exceeds approximately 17V. At supply voltages between V_{SD} and 17V care must be taken to avoid excessive power dissipation due to the on-resistance.

Note that when driving loads of two or more LEDs, the forward drop will normally be sufficient to prevent the device from switching below approximately 6V. This will minimize the risk of damage to the device.

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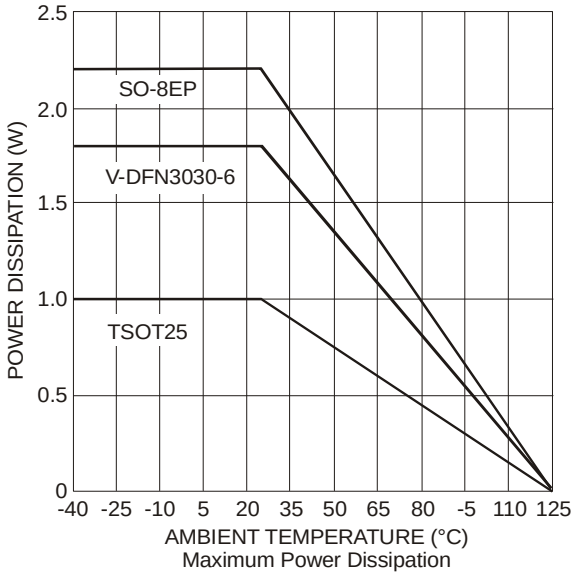
Application Information (cont.)

Thermal Considerations

When operating the device at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The graph below gives details for power derating. This assumes the device to be mounted on a 25mm^2 PCB with 1oz copper standing in still air.



Note that the device power dissipation will most often be a maximum at minimum supply voltage. It will also increase if the efficiency of the circuit is low. This may result from the use of unsuitable coils, or excessive parasitic output capacitance on the switch output.

In order to maximize the thermal capabilities of the DFN3030-6 and the SO-8EP packages thermal vias should be incorporated into the PCB. See figures 7 and 8 for examples used in the ZXLD1366 evaluation boards.

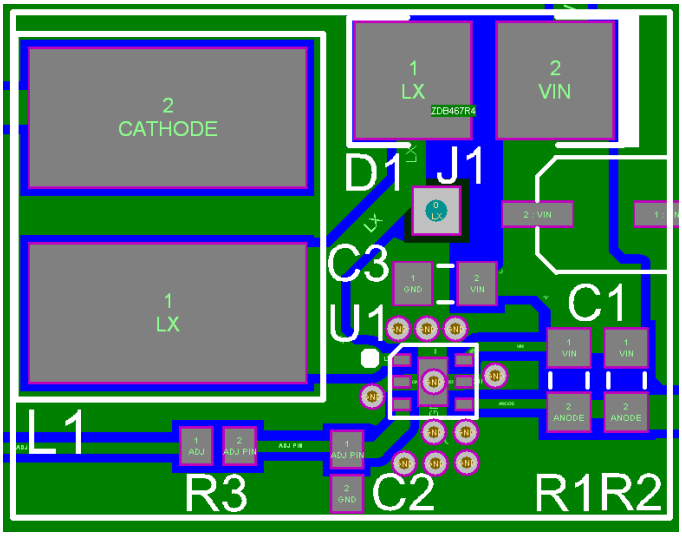


Figure. 7 Suggested Layout for V-DFN3030-6 Package

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Application Information (cont.)

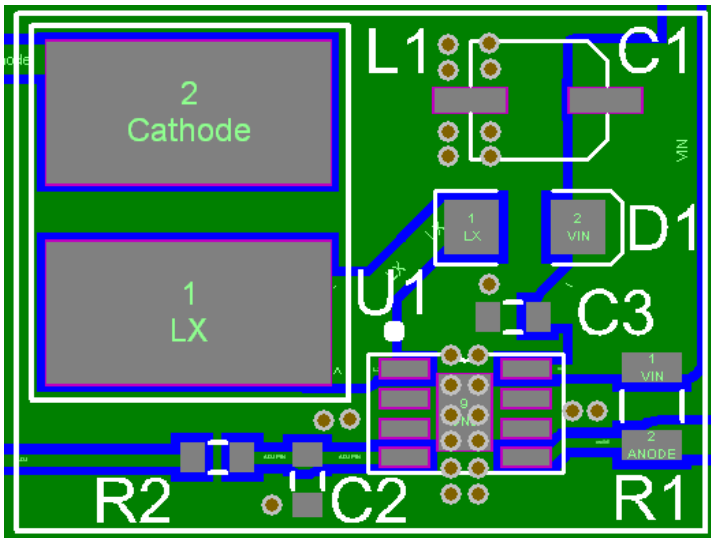

Figure. 8 Suggested Layout for SO-8EP Package

Vias ensure an effective path to the ground plane for the heat flow therefore reducing the thermal impedance between junction and ambient temperature. Diodes came to the conclusion that the compromise is reached by using more than 10 vias with 1mm of diameter and 0.5 hole size.

Finally the same scheme in Figure 7 (without the exposed paddle) can be usde for the TSOT25 package guaranteeing an effective thermal path.

Thermal Compensation of Output Current

High luminance LEDs often need to be supplied with a temperature compensated current in order to maintain stable and reliable operation at all drive levels. The LEDs are usually mounted remotely from the device so, for this reason, the temperature coefficients of the internal circuits for the ZXLD1366 have been optimized to minimize the change in output current when no compensation is employed. If output current compensation is required, it is possible to use an external temperature sensing network normally using Negative Temperature Coefficient (NTC) thermistors and/or diodes, mounted very close to the LED(s). The output of the sensing network can be used to drive the ADJ pin in order to reduce output current with increasing temperature.

Layout Considerations

LX Pin

The LX pin of the device is a fast switching node, so PCB tracks should be kept as short as possible. To minimize ground 'bounce', the ground pin of the device should be soldered directly to the ground plane.

Coil and Decoupling Capacitors and Current Sense Resistor

It is particularly important to mount the coil and the input decoupling capacitor as close to the device pins as possible to minimize parasitic resistance and inductance, which will degrade efficiency. It is also important to minimize any track resistance in series with current sense resistor R_S. Its best to connect V_{IN} directly to one end of R_S and I_{SENSE} directly to the opposite end of R_S with no other currents flowing in these tracks. It is important that the cathode current of the Schottky diode does not flow in a track between R_S and V_{IN} as this may give an apparent higher measure of current than is actual because of track resistance.

ADJ Pin

The ADJ pin is a high impedance input for voltages up to 1.35V so, when left floating, PCB tracks to this pin should be as short as possible to reduce noise pickup. A 100nF capacitor from the ADJ pin to ground will reduce frequency modulation of the output under these conditions. An additional series 3.3kΩ resistor can also be used when driving the ADJ pin from an external circuit (see next page). This resistor will provide filtering for low frequency noise and provide protection against high voltage transients.

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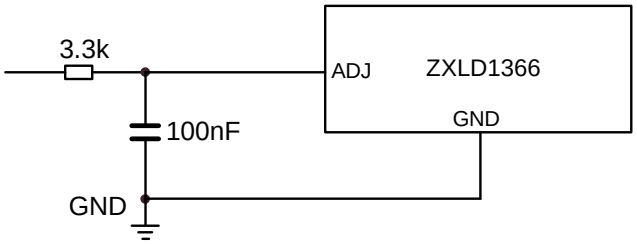
Application Information (cont.)



High Voltage Tracks

Avoid running any high voltage tracks close to the ADJ pin, to reduce the risk of leakage currents due to board contamination. The ADJ pin is soft-clamped for voltages above 1.35V to desensitize it to leakage that might raise the ADJ pin voltage and cause excessive output current. However, a ground ring placed around the ADJ pin is recommended to minimize changes in output current under these conditions.

Evaluation PCB

ZXLD1366 evaluation boards are available on request. Terminals allow users to interface the boards to their preferred LED products.

Dimming Output Current Using PWM

Low Frequency PWM Mode

When the ADJ pin is driven with a low frequency PWM signal (eg 100Hz), with a high level voltage V_{ADJ} and a low level of zero, the output of the internal low pass filter will swing between 0V and V_{ADJ}, causing the input to the shutdown circuit to fall below its turn-off threshold (200mV nom) when the ADJ pin is low. This will cause the output current to be switched on and off at the PWM frequency, resulting in an average output current I_{OUTavg} proportional to the PWM duty cycle.
(See Figure 9 - Low frequency PWM operating waveforms).

The average value of output current in this mode is given by:

$$I_{OUTavg} \approx 0.2 D_{PWM} / R_S \text{ [for } D_{PWM} > 0.001\text{]}$$

This mode is preferable if optimum LED 'whiteness' is required. It will also provide the widest possible dimming range (approx. 1000:1) and higher efficiency at the expense of greater output ripple.

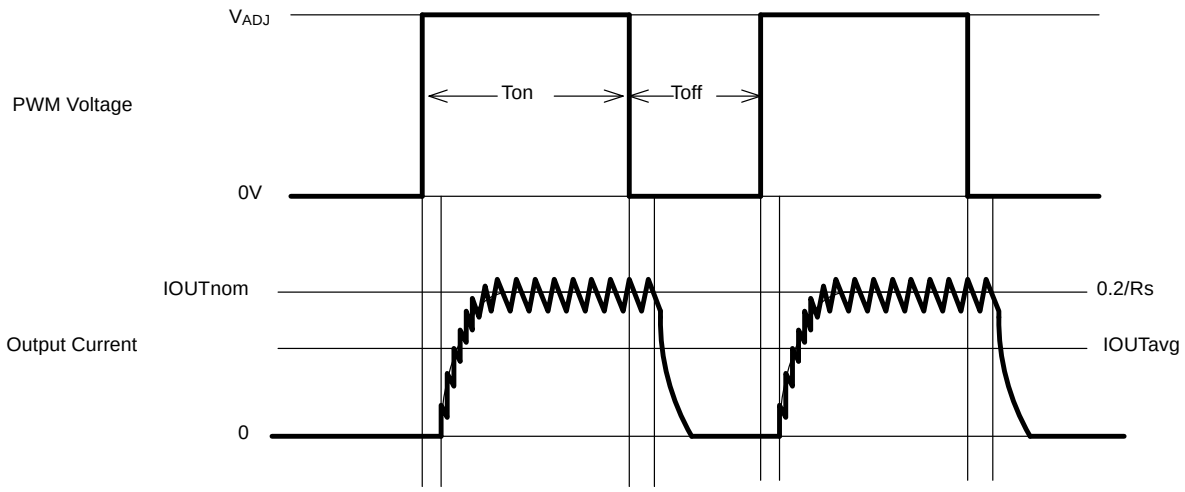


Figure. 9 Low Frequency PWM Operating Waveforms

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Ordering Information

ZXLD1366 XXX XX

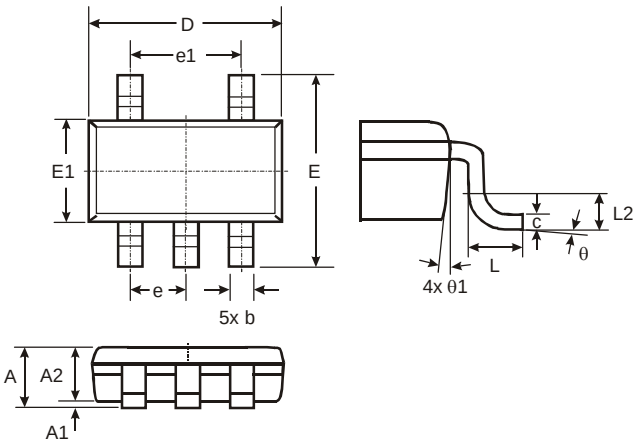
Part Number	Package	Packing
ZXLD1366	DAC : V-DFN3030-6	TC : 13” Tape & Reel
	EN8 : SO-8EP	TC : 13” Tape & Reel
	ET5 : TSOT25	TA : 7” Tape & Reel

Device	Part Mark	Packaging	Reel Size (inches)	Reel Width (mm)	Quantity Per Reel	Part Number Suffix	AEC-Q100
ZXLD1366DACTC	1366	V-DFN3030-6	13	12	3000	TC	
ZXLD1366EN8TC	ZXLD 1366 YYWW	SO-8EP	13	12	2500	TC	Grade 1
ZXLD1366ET5TA	1366	TSOT25	7	8	3000	TA	Grade 1

Where YY stands for last 2 digits of year - 10, 11 and WW stands for week number.

Package Outline Dimensions

1) TSOT25



TSOT25			
Dim	**Min**	**Max**	**Typ**
A	–	1.00	–
A1	0.01	0.10	–
A2	0.84	0.90	–
D	–	–	2.90
E	–	–	2.80
E1	–	–	1.60
b	0.30	0.45	–
c	0.12	0.20	–
e	–	–	0.95
e1	–	–	1.90
L	0.30	0.50	
L2	–	–	0.25
θ	0°	8°	4°
θ1	4°	12°	–
All Dimensions in mm			

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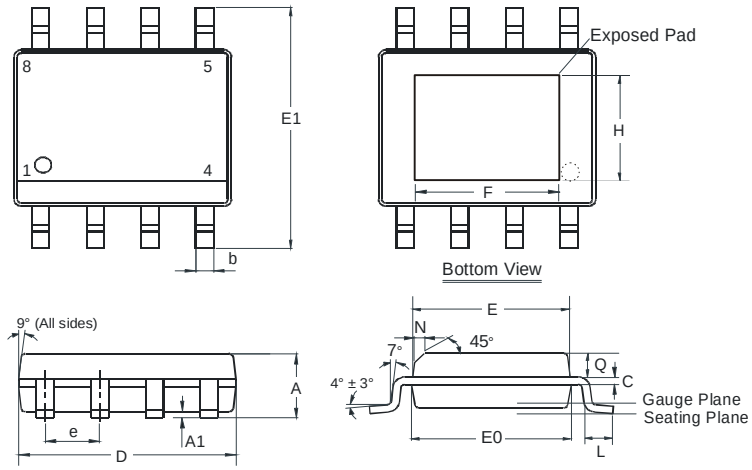
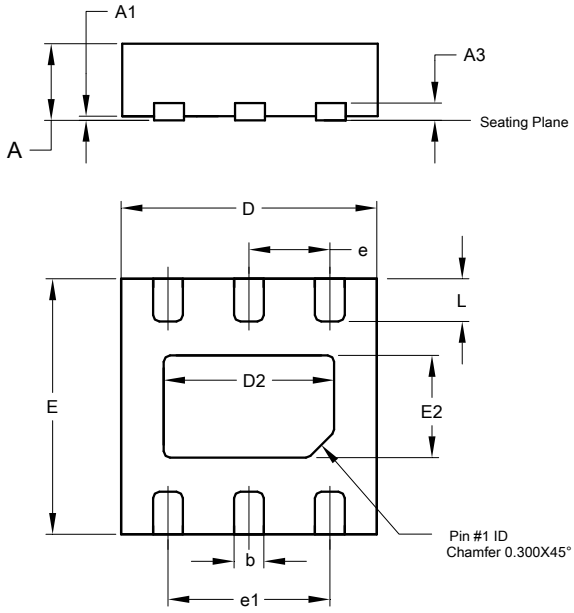
Package Outline Dimensions (cont.)

2) SO-8EP



SO-8EP (SOP-8L-EP)			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

3) V-DFN3030-6



V-DFN3030-6			
Dim	**Min**	**Max**	**Typ**
A	0.80	0.90	0.85
A1	0	0.05	-
A3	-	-	0.203
b	0.30	0.40	0.35
D	2.95	3.05	3.00
D2	1.95	2.05	2.00
E	2.95	3.05	3.00
E2	1.15	1.25	1.20
e	-	-	0.95
e1	-	-	1.90
L	0.45	0.55	0.50
All Dimensions in mm			

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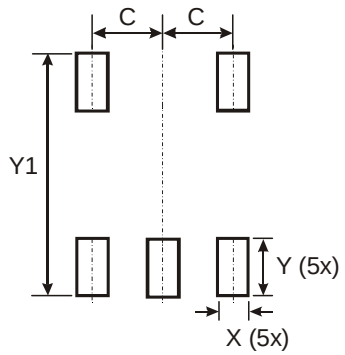
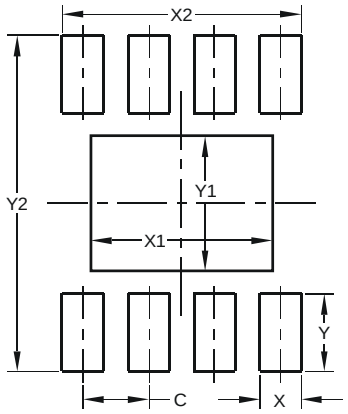
Suggested Pad Layout

1) TSOT25



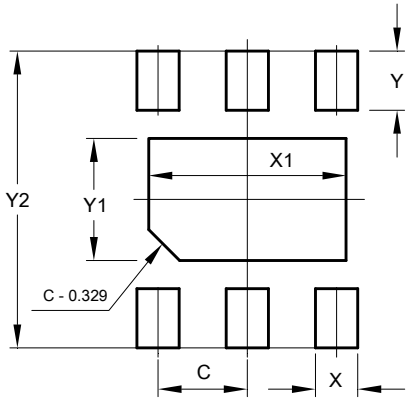
Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

2) SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

3) V-DFN3030-6



Dimensions	Value (in mm)
C	0.950
X	0.450
X1	2.100
Y	0.630
Y1	1.300
Y2	3.160

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