

TIC106A, TIC106B, TIC106C, TIC106D, TIC106E, TIC106M, TIC106N, TIC106S

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

- 5 A Continuous On-State Current
- 30 A Surge-Current
- Glass Passivated Wafer
- 100 V to 800 V Off-State Voltage
- Max I_{GT} of 200 μA
- Compliance to ROHS

ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Value								Unit
		A	B	C	D	E	M	S	N	
V_{DRM}	Repetitive peak off-state voltage (see Note1)	100	200	300	400	500	600	700	800	V
V_{RRM}	Repetitive peak reverse voltage	100	200	300	400	500	600	700	800	V
$I_{T(RMS)}$	Continuous on-state current at (or below) 80°C case temperature (see note2)	5								A
$I_{T(AV)}$	Average on-state current (180° conduction angle) at(or below) 80°C case temperature (see Note3)	3.2								A
I_{TM}	Surge on-state current (see Note4)	30								A
I_{GM}	Peak positive gate current (pulse width $\leq 300 \mu s$)	0.2								A
P_{GM}	Peak power dissipation (pulse width $\leq 300 \mu s$)	1.3								W
$P_{G(AV)}$	Average gate power dissipation (see Note5)	0.3								W
T_C	Operating case temperature range	-40 to +110								°C
T_{stg}	Storage temperature range	-40 to +125								°C
T_L	Lead temperature 1.6 mm from case for 10 seconds	230								°C

TIC106A, TIC106B, TIC106C, TIC106D, TIC106E, TIC106M, TIC106N, TIC106S

THERMAL CHARACTERISTICS

Symbol	Ratings		Value	Unit
t_{gt}	Gate-controlled Turn-on time	$V_{AA} = 30\text{ V}, R_L = 6\ \Omega$ $R_{GK(\text{eff})} = 5\text{ k}\Omega$ $V_{in} = 50\text{ V}$	1.75	μs
t_q	Circuit-communicated Turn-off time	$V_{AA} = 30\text{ V}, R_L = 6\ \Omega$ $I_{RM} \approx 8\text{ A}$	7.7	
$R_{\theta JC}$	Junction to case thermal resistance		≤ 3.5	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Junction to free air thermal resistance		≤ 62.5	

ELECTRICAL CHARACTERISTICS

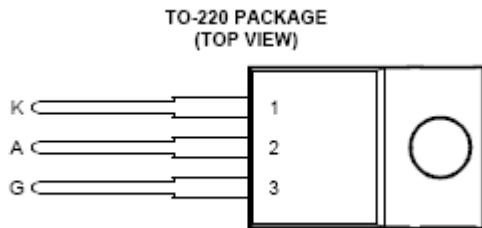
TC=25°C unless otherwise noted

Symbol	Ratings	Test Condition(s)	Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = \text{Rated } V_{DRM}$ $R_{GK} = 1\text{ k}\Omega, T_C = 110^{\circ}\text{C}$	-	-	400	μA
I_{RRM}	Repetitive peak reverse current	$V_R = \text{Rated } V_{RRM}, I_G = 0$ $T_C = 110^{\circ}\text{C}$	-	-	1	mA
I_{GT}	Gate trigger current	$V_{AA} = 6\text{ V}, R_L = 100\ \Omega$ $t_{p(g)} \geq 20\ \mu\text{s}$	-	60	200	μA
V_{GT}	Gate trigger voltage	$V_{AA} = 6\text{ V}, R_L = 100\ \Omega$ $R_{GK} = 1\text{ k}\Omega, t_{p(g)} \geq 20\ \mu\text{s}$ $T_C = -40^{\circ}\text{C}$	-	-	1.2	V
		$V_{AA} = 6\text{ V}, R_L = 100\ \Omega$ $R_{GK} = 1\text{ k}\Omega, t_{p(g)} \geq 20\ \mu\text{s}$	0.4	0.6	1	
		$V_{AA} = 6\text{ V}, R_L = 100\ \Omega$ $R_{GK} = 1\text{ k}\Omega, t_{p(g)} \geq 20\ \mu\text{s}$ $T_C = 110^{\circ}\text{C}$	0.2	-	-	
I_H	Holding current	$V_{AA} = 6\text{ V}, R_{GK} = 1\text{ k}\Omega$ initiating $I_T = 10\text{ mA}$	-	-	5	mA
		$V_{AA} = 6\text{ V}, R_{GK} = 1\text{ k}\Omega$ initiating $I_T = 10\text{ mA}$ $T_C = -40^{\circ}\text{C}$	-	-	8	
V_{TM}	Peak on-state voltage	$I_{TM} = 5\text{ A}$ (see Note6)	-	-	1.7	V
dv/dt	Critical rate of rise of off-state voltage	$V_D = \text{Rated } V_D$ $R_{GK} = 1\text{ k}\Omega, T_C = 110^{\circ}\text{C}$	-	10	-	V/ μs



TIC106A, TIC106B, TIC106C, TIC106D, TIC106E, TIC106M, TIC106N, TIC106S

PINNING



Pin 1 :	kathode
Pin 2 :	Anode
Pin 3 :	Gate

Pin 2 is in electrical contact with the mounting base.

Revised September 2012

Information furnished is believed to be accurate and reliable. However, Comset Semiconductors assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. Data are subject to change without notice. Comset Semiconductors makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Comset Semiconductors assume any liability arising out of the application or use of any product and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Comset Semiconductors' products are not authorized for use as critical components in life support devices or systems.

www.comsetsemi.com

info@comsetsemi.com