

J/SST108 Series

Siliconix

N-Channel JFETs

J108	SST108
J109	SST109
J110	SST110

Product Summary

Part Number	V _{GS(off)} (V)	r _{DS(on)} Max (Ω)	I _{D(off)} Typ (pA)	t _{ON} Typ (ns)
J/SST108	-3 to -10	8	20	4
J/SST109	-2 to -6	12	20	4
J/SST110	-0.5 to -4	18	20	4

Features

- Low On-Resistance: J108 <8 Ω
- Fast Switching—t_{ON}: 4 ns
- Low Leakage: 20 pA
- Low Capacitance: 11 pF
- Low Insertion Loss

Benefits

- Low Error Voltage
- High-Speed Analog Circuit Performance
- Negligible "Off-Error," Excellent Accuracy
- Good Frequency Response
- Eliminates Additional Buffering

Applications

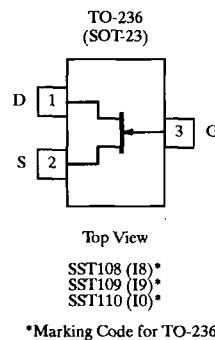
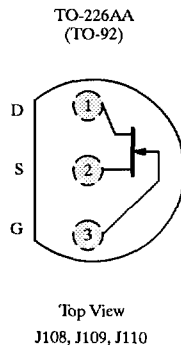
- Analog Switches
- Choppers
- Sample-and-Hold
- Normally "On" Switches
- Current Limiters

Description

The J/SST108 series is designed with high-performance analog switching applications in mind. It features low on-resistance, good off-isolation, and fast switching.

The SST108 series is comprised of surface-mount devices featuring the lowest r_{DS(on)} of any TO-236 (SOT-23) JFET device.

The TO-226AA (TO-92) plastic package provides a low-cost option. Both the J and SST series are available in tape-and-reel for automated assembly (see Packaging Information). For similar products packaged in TO-206AC (TO-52), see the 2N5432/5433/5434 data sheet.



Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage	-25 V
Gate Current	50 mA
Lead Temperature (1/16" from case for 10 sec.)	300°C
Storage Temperature	-55 to 150°C

Operating Junction Temperature	-55 to 150°C
Power Dissipation ^a	350 mW

Notes
a. Derate 2.8 mW/°C above 25°C

Switching Time Test Circuit

	J105	J106	J107
$V_{GS(L)}$	-12V	-7V	-5V
R_L	50 Ω	50 Ω	50 Ω
$I_{D(on)}$	28 mA	27 mA	26 mA

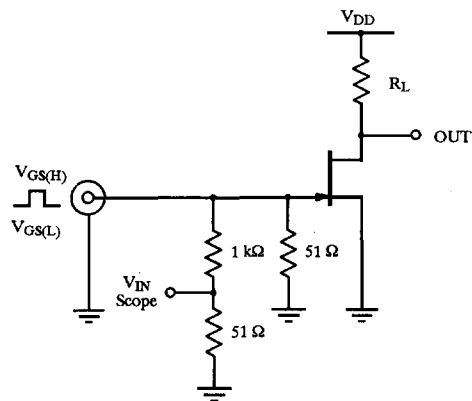
*Non-inductive

Input Pulse

Rise Time < 1 ns
 Fall Time < 1 ns
 Pulse Width 100 ns
 PRF 1 MHz

Sampling Scope

Rise Time 0.4 ns
 Input Resistance 10 M Ω
 Input Capacitance 1.5 pF



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Specifications^a

Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit
				J/SST108		J/SST109		J/SST110		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 5 V, I_D = 1 \mu A$		-3	-10	-2	-6	-0.5	-4	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 15 V, V_{GS} = 0 V$		80		40		10		mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -15 V, V_{DS} = 0 V$ $T_A = 125^\circ C$	-0.01		-3		-3		-3	nA
			-5							
Gate Operating Current	I_G	$V_{DG} = 10 V, I_D = 10 mA$	-0.01							
Drain Cutoff Current	$I_{D(off)}$	$V_{DS} = 5 V, V_{GS} = -10 V$ $T_A = 125^\circ C$	0.02		3		3		3	nA
			1.0							
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0 V, V_{DS} \leq 0.1 V$			8		12		18	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1 mA, V_{DS} = 0 V$	0.7							V
Dynamic										
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 5 V, I_D = 10 mA, f = 1 kHz$	17							mS
Common-Source Output Conductance	g_{os}		0.6							
Drain-Source On-Resistance	$r_{ds(on)}$	$V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz$			8		12		18	Ω
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 0 V$ $V_{GS} = 0 V$ $f = 1 MHz$	SST	60						pF
			J Series	60		85		85		
Common-Source Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 0 V$ $V_{GS} = -10 V$ $f = 1 MHz$	SST	11						pF
			J Series	11		15		15		
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DG} = 5 V, I_D = 10 mA$ $f = 1 kHz$	3.5							nV/ \sqrt{Hz}
Switching										
Turn-On Time	$t_{d(on)}$	$V_{DD} = 1.5 V, V_{GS(H)} = 0 V$ Sec Switching Diagram	3							ns
	t_r		1							
Turn-Off Time	$t_{d(off)}$		4							
	t_f		18							

Notes

- a. $T_A = 25^\circ C$ unless otherwise noted.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- c. Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.

NIP

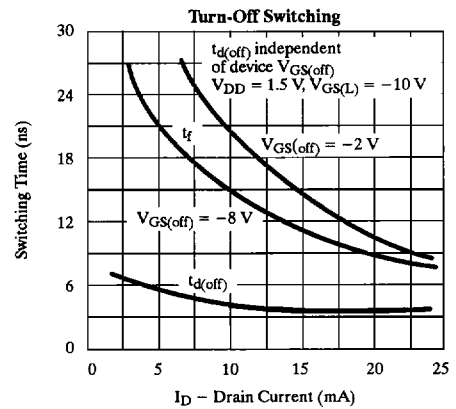
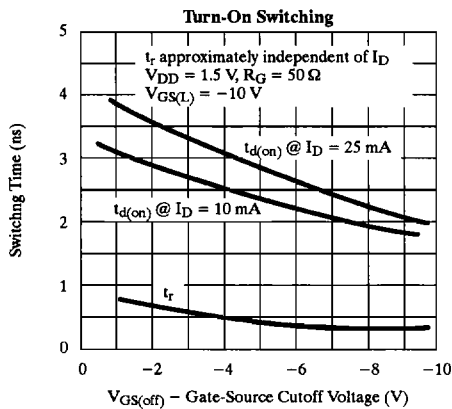
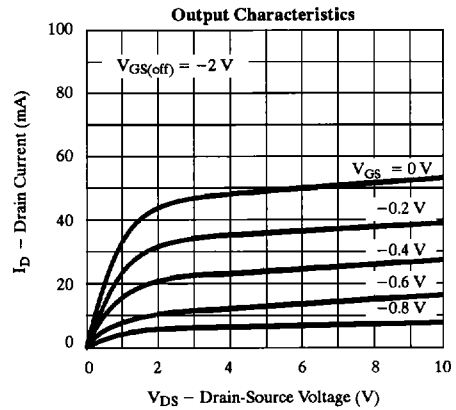
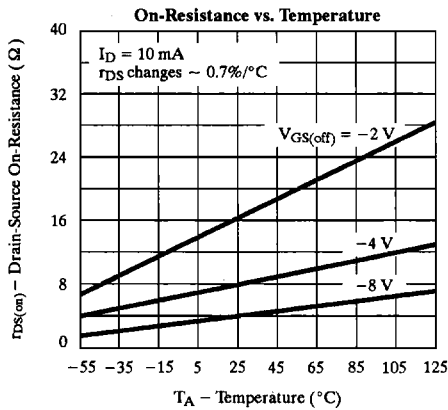
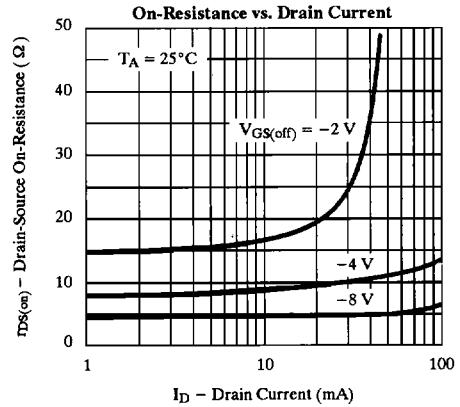
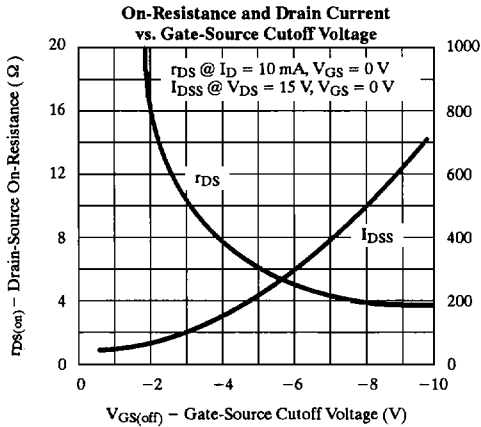
7

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Typical Characteristics



Typical Characteristics (Cont'd)

