9 Electrical specifications

9.1 DC electrical characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VDD	DC supply voltage	0	7.0	V	1,2,3
V_I, V_O	Voltage on input and output pins	–0.5	VDD+0.5	V	1,2,3
I_I	Input current		±25	mA	4
t_{OSC}	Output short circuit time (one pin)		1	s	2
T_S	Storage temperature	–65	150	°C	2
T_A	Ambient temperature under bias	–55	125	°C	2
P_{Dmax}	Maximum allowable dissipation		2	W	2

Notes

1 All voltages are with respect to **GND**.

2 This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operating sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3 This device contains circuitry to protect the inputs against damage caused by high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this high impedance circuit. Unused inputs should be tied to an appropriate logic level such as **VDD** or **GND**.

4 The input current applies to any input or output pin and applies when the voltage on the pin is between **GND** and **VDD**.

Table 9.1 Absolute maximum ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VDD	DC supply voltage	4.75	5.25	V	1
V_I, V_O	Input or output voltage	0	VDD	V	1,2
C_L	Load capacitance on any pin		60	pF	3
T_A	Operating temperature range	–55	125	°C	

Notes

1 All voltages are with respect to **GND**.

2 Excursions beyond the supplies are permitted but not recommended; see DC characteristics.

3 Excluding **LinkOut** load capacitance.

Table 9.2 Operating conditions

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
V_{IH}	High level input voltage		2.0	VDD+0.5	V	1, 2
V_{IL}	Low level input voltage		–0.5	0.8	V	1, 2
I_I	Input current	@ GND<VI<VDD		±10	µA	1, 2
V_{OH}	Output high voltage	@ IOH=2mA	VDD–1		V	1, 2
V_{OL}	Output low voltage	@ IOL=4mA		0.4	V	1, 2
I_{OZ}	Tristate output current	@ GND<V0<VDD		±10	µA	1, 2
P_D	Power dissipation			1.2	W	2, 3
C_{IN}	Input capacitance	@ f=1MHz		7	pF	
C_{OZ}	Output capacitance	@ f=1MHz		10	pF	

Notes

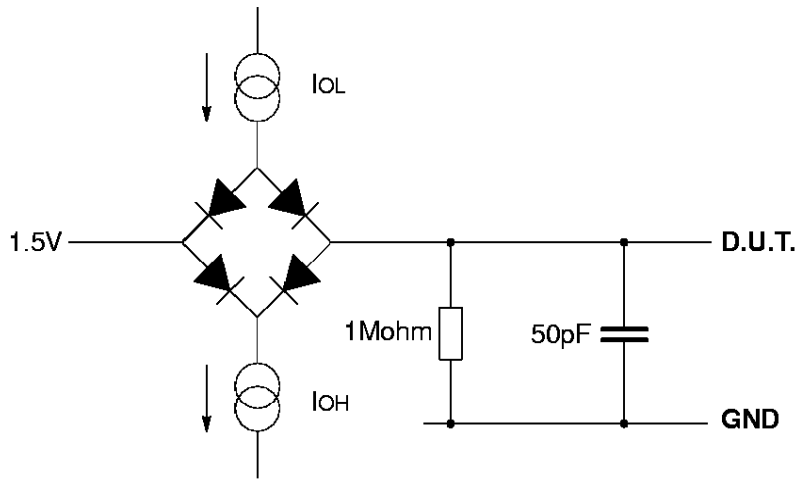
1 All voltages are with respect to **GND**.

2 Parameters for IMS T805E measured at 4.75V<**VDD**<5.25V and –55ºC<**TA**<125ºC. Input clock frequency = 5 MHz.

3 Power dissipation varies with output loading and program execution. Power dissipation for processor operating at 20 MHz.

Table 9.3 DC characteristics

9.2 Equivalent circuits



Note: This circuit represents the device sinking IOL and sourcing IOH with a 50pF capacitive load.

Figure 9.1 Load circuit for AC measurements

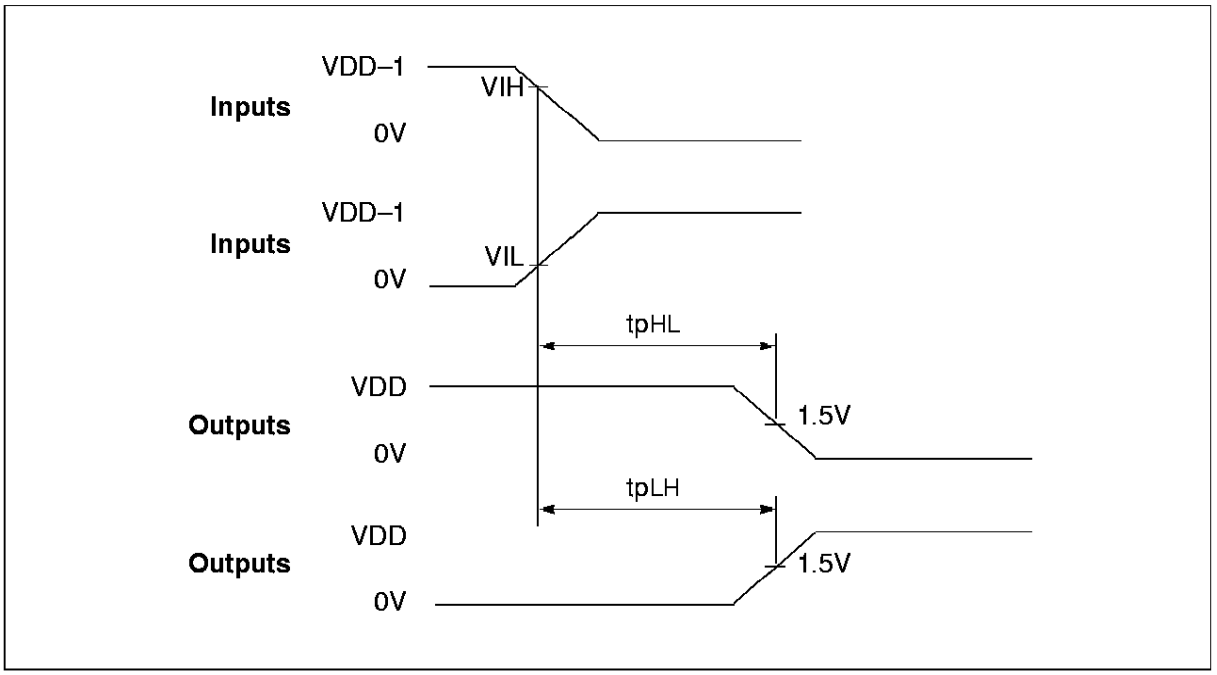


Figure 9.2 AC measurements timing waveforms

9.3 AC timing characteristics

Symbol	Parameter	Min	Max	Units	Notes
TDr	Input rising edges	2	20	ns	1, 2
TDf	Input falling edges	2	20	ns	1, 2
TQr	Output rising edges		25	ns	1
TQf	Output falling edges		15	ns	1
TS0LaX	Address hold after **notMemS0**	**a**–8	**a**+8	ns	3

Notes

1 Non-link pins; see section on links.

2 All inputs except **ClockIn**; see section on **ClockIn**.

3 **a** is **T2** where **T2** can be from one to four periods **Tm** in length. Address lines include **MemnotWrD0**, **MemnotRfD1**, **MemAD2-31**.

Table 9.4 Input and output edges

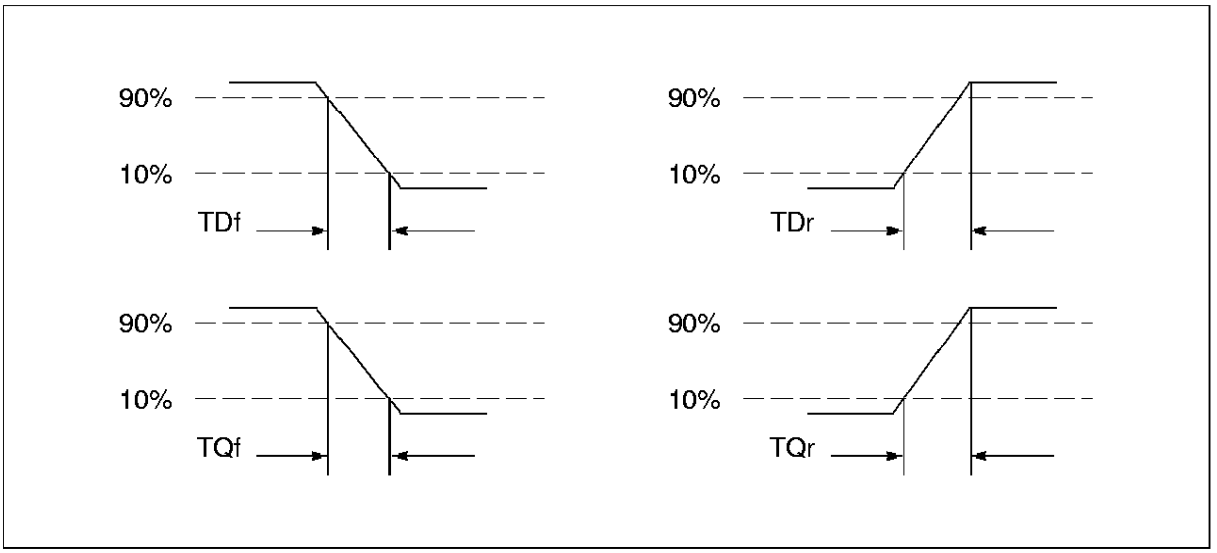


Figure 9.3 IMS T805E input and output edge timing

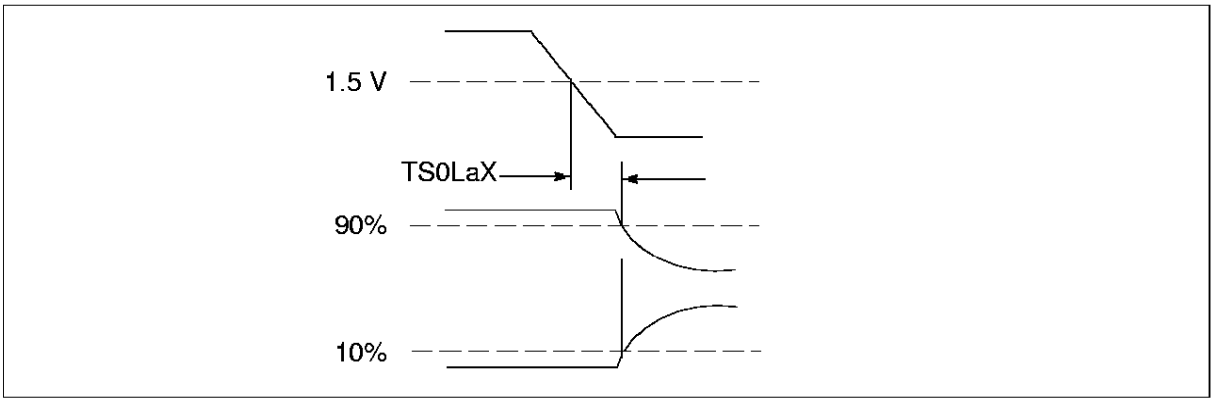
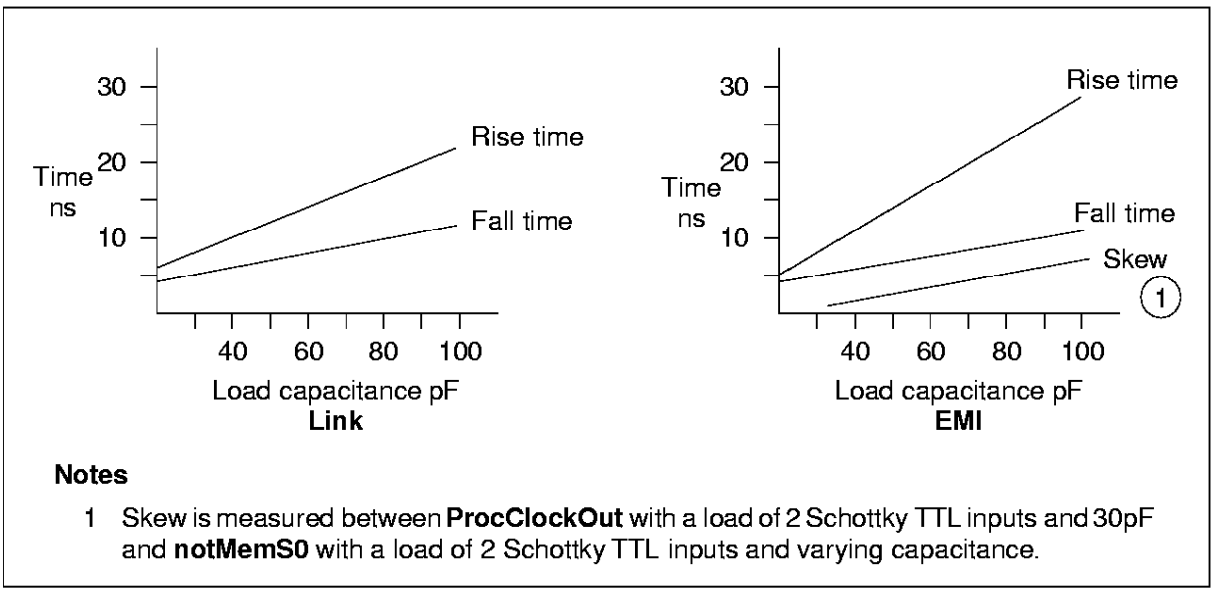


Figure 9.4 IMS T805E tristate timing relative to **notMemS0**



Notes

1 Skew is measured between **ProcClockOut** with a load of 2 Schottky TTL inputs and 30pF and **notMemS0** with a load of 2 Schottky TTL inputs and varying capacitance.

Figure 9.5 Typical rise/fall times

9.4 Power rating

Internal power dissipation (P_{INT}) of transputer and peripheral chips depends on **VDD**, as shown in figure 9.6. P_{INT} is substantially independent of temperature.

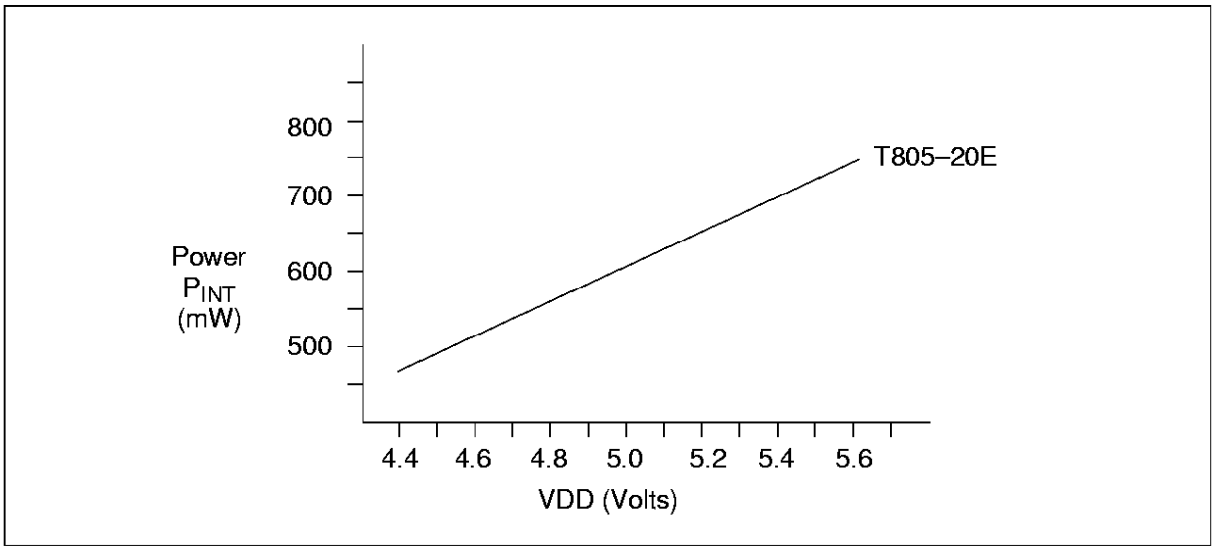


Figure 9.6 IMS T805E internal power dissipation vs VDD

Total power dissipation (P_D) of the chip is

$$P_D = P_{INT} + P_{IO}$$

where P_{IO} is the power dissipation in the input and output pins; this is application dependent.

Internal working temperature T_J of the chip is

$$T_J = T_A + \theta_{JA} \times P_D$$

where T_A is the external ambient temperature in °C and θ_{JA} is the junction-to-ambient thermal resistance in °C/W.

Further information about device thermal characteristics can be found in section 10.3.