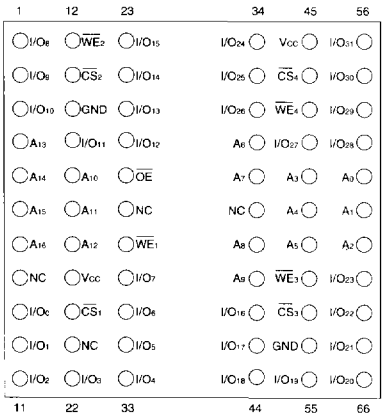
128Kx32 SRAM MODULE

FEATURES

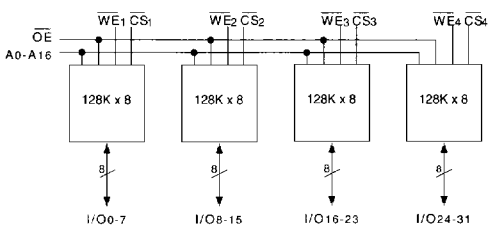
- Access Times of 55 to 120nS
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic Package, Industry Standard Pinout, SMD Number 5962-93187
  - 68 lead, 40mm, Hermetic CQFP
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS128K32-XHX - 13 grams typical
  WS128K32-XG4X - 20 grams typical

FIG. 1 PIN CONFIGURATION FOR WS-128K32N-XHX, SMD5962-93137

TOP VIEW



BLOCK DIAGRAM



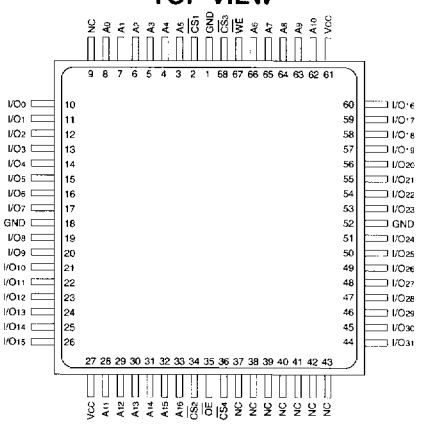
PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

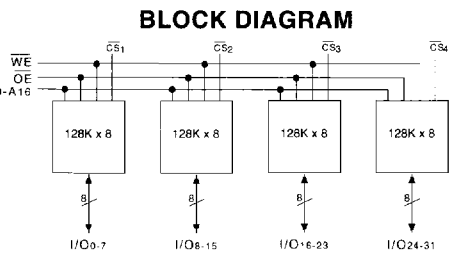
SID2001/SID3001

FIG. 2 PIN CONFIGURATION FOR WS-128K32-XG4X

TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz		50	pF
$\overline{WE}$ 1-4 capicitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		30	pF
$\overline{CS}$ 1-4 capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz		30	pF
D0 - D31 capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz		30	pF
A0 - A16 capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz		50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-55		-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10		10		10	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		350		300		300		220		220	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, f = 5MHz		35		7		7		5		5	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		2.4		2.4		2.4		2.4		V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-55			-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} - .2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		30	3200		30	3000		10	1600		10	1100		10	1100	µA
	I_{CCDR2}	V_{CC} = 2V		20	2100		20	2000		8	1200		8	800		8	800	µA

AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C To +125°C)

Parameter	Symbol	-55		-70		-85		-100		-120		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	55		70		85		100		120		nS
Address Access Time	t_{AA}		55		70		85		100		120	nS
Output Hold from Address Change	t_{OH}	5		5		15		15		15		nS
Chip Select Access	t_{ACS}		55		70		85		100		120	nS
Output Enable to Output Valid	t_{OE}		30		35		40		45		50	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		5		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		25		30		35		40		50	nS
Output Disable to Output in High Z	t_{OHZ}[1]		25		30		35		40		50	nS

1. This parameter is guaranteed by design but not tested.

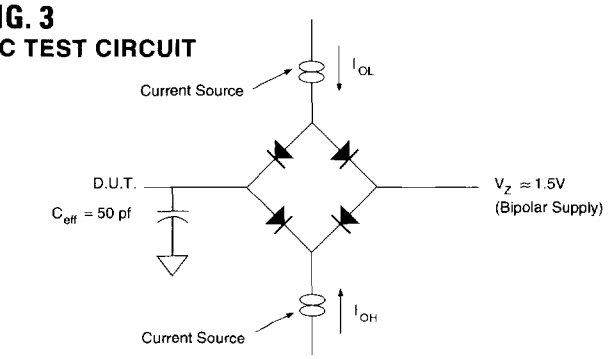
AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C To +125°C)

Parameter	Symbol	-55		-70		-85		-100		-120		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	55		70		85		100		120		nS
Chip Select to End of Write	t_{CW}	45		65		80		90		110		nS
Address Valid to End of Write	t_{AW}	45		65		80		90		110		nS
Data Valid to End of Write	t_{DW}	25		30		35		40		55		nS
Write Pulse Width	t_{WP}	40		45		50		55		65		nS
Address Setup Time	t_{AS}	0		5		5		5		5		nS
Address Hold Time	t_{AH}	0		0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		10		10		10		10		nS
Write Enable to Output in High Z	t_{WHZ}[1]		20		30		35		40		50	nS
Data Hold from Write Time	t_{DH}	0		0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT

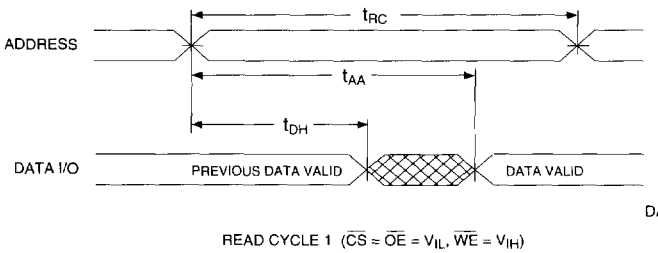


AC TEST CONDITIONS

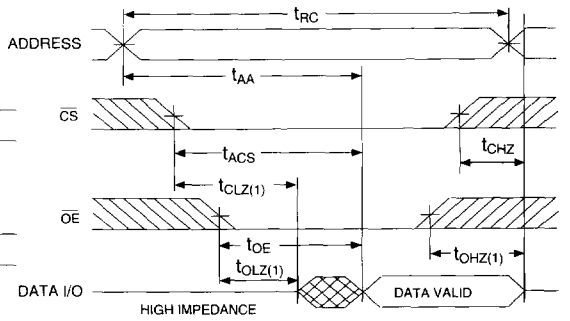
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 4
TIMING WAVEFORM - READ CYCLE



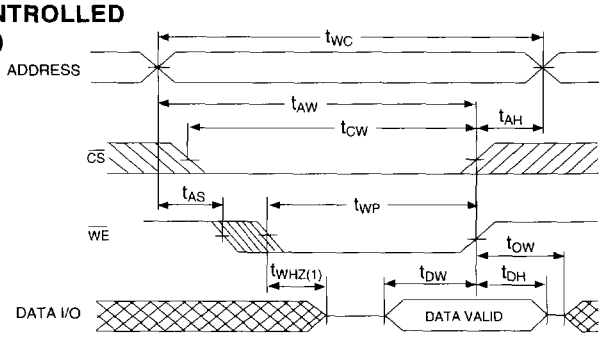
READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



READ CYCLE 2 ($\overline{WE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

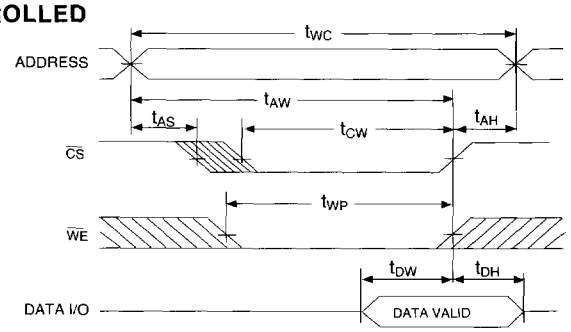
FIG. 5
WRITE CYCLE - $\overline{WE}$ CONTROLLED ($\overline{OE}$ IS INACTIVE - HIGH)



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED ($\overline{OE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

FIG. 6
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED ($\overline{OE}$ = V_{IH})

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

FIG. 7
PACKAGE DIMENSIONS (16A06)

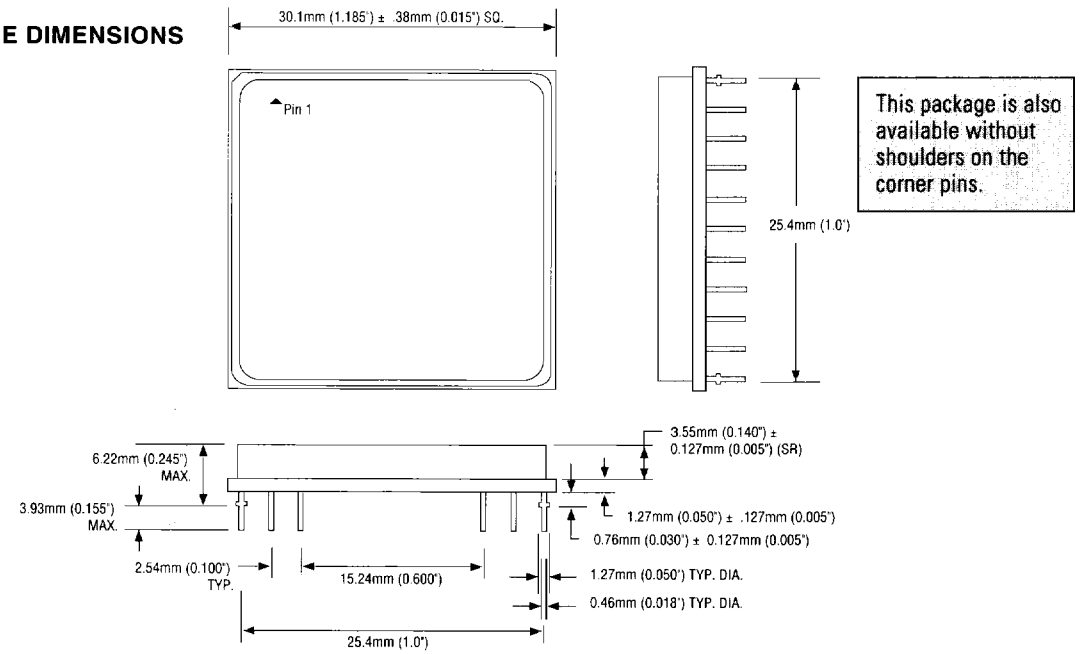
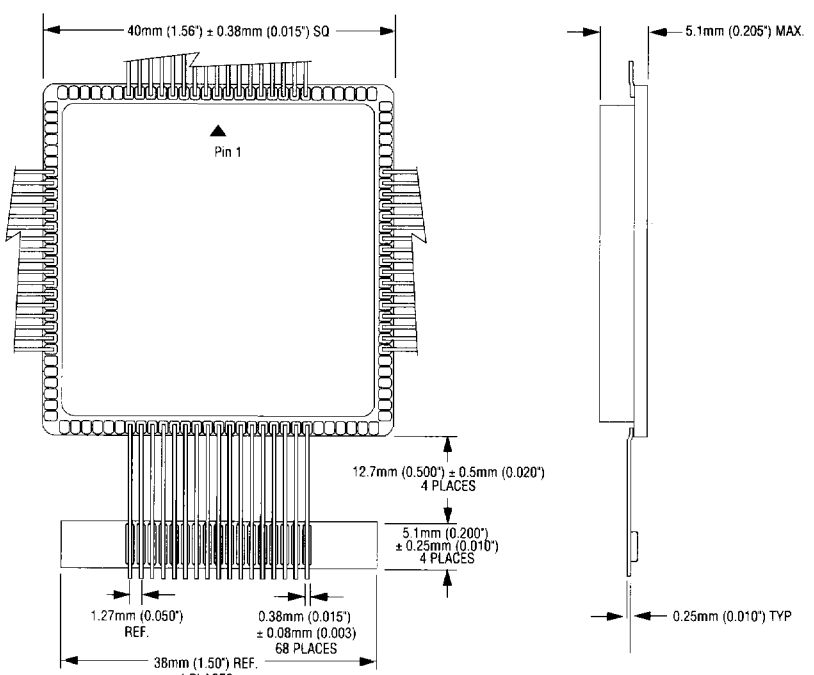
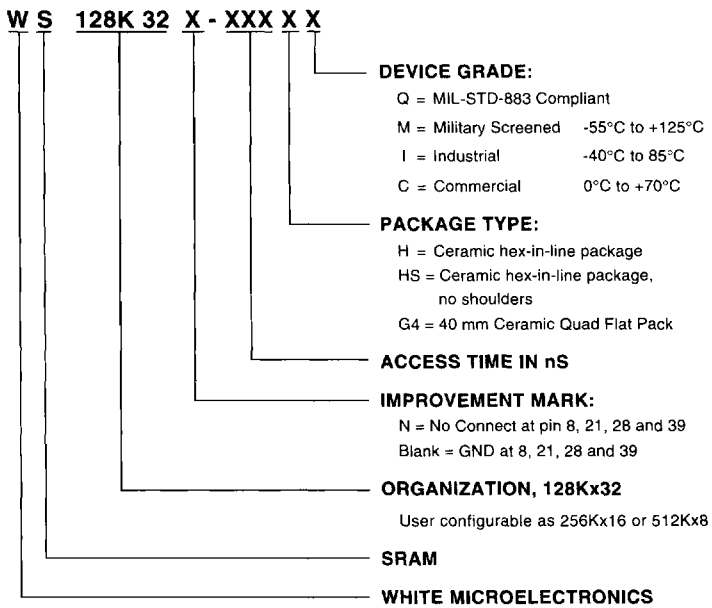


FIG. 8
PACKAGE DIMENSIONS (14A15)



ORDERING INFORMATION



Device Type	Speed	Package	SMD Number
128K x 32 SRAM	120nS	66 pin HIP	5962 93187-01HXX
128K x 32 SRAM	100nS	66 pin HIP	5962 93187-02HXX
128K x 32 SRAM	85nS	66 pin HIP	5962 93187-03HXX
128K x 32 SRAM	70nS	66 pin HIP	5962 93187-04HXX
128K x 32 SRAM	55nS	66 pin HIP	5962 93187-05HXX

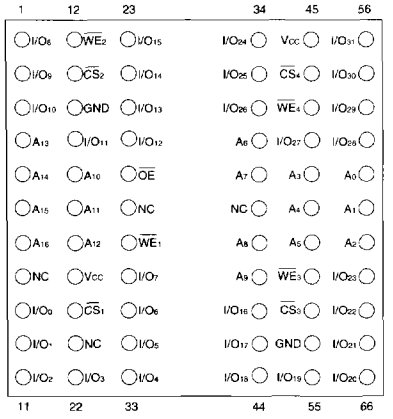
128Kx32 SRAM MODULE

FEATURES

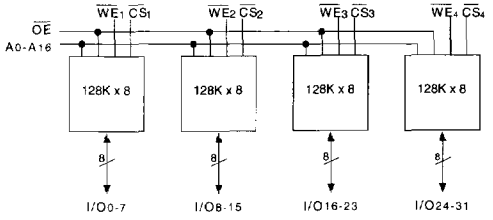
- Access Times of 25 to 45nS
- MIL-STD-883 Compliant Devices Available
- Rad Tolerant Devices Available
- Packaging
  - 66-pin, PGA Type, 1.185 inch square HIP, Hermetic Ceramic Package. Industry Standard Pinout, SMD Number 5962-93187
  - 68 lead, 40mm, Hermetic CQFP
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS128K32-XHX - 13 grams typical
  WS128K32-XG4X - 20 grams typical

FIG. 1 PIN CONFIGURATION FOR WS128K32N-XHX, SMD5962-93187

TOP VIEW



BLOCK DIAGRAM



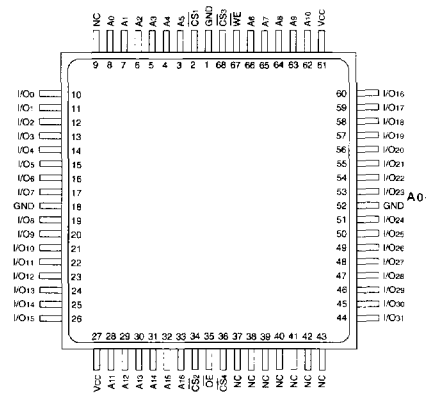
PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

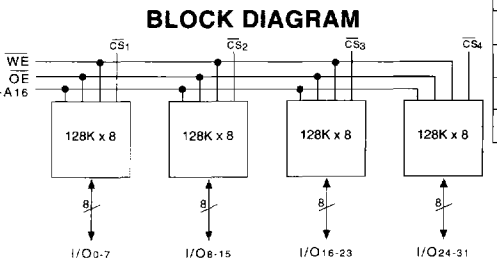
SID3001/SID3301

FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4X

TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(@ T_A = +25°C)

Test	Symbol	Conditions	Limits		Unit
			Min	Max	
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz		50	pF
$\overline{WE}$ 1-4 capicitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		30	pF
$\overline{CS}$ 1-4 capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz		30	pF
D0 - D31 capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz		30	pF
A0 - A16 capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz		50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	-25		-35		-45		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		500		500		400	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		60		60		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-25			-35			-45			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -.2V	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		0.5	8.0		0.5	8.0		0.5	8.0	mA
	I_{CCDR2}	V_{CC} = 2V		0.25	4.0		0.25	4.0		0.25	4.0	mA

AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		-35		-45		Units
Read Cycle		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		nS
Address Access Time	t_{AA}		25		35		45	nS
Output Hold from Address Change	t_{OH}	5		5		5		nS
Chip Select Access Time	t_{ACS}		25		35		45	nS
Output Enable to Output Valid	t_{OE}		15		20		25	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}[1]		12		15		20	nS
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20	nS

1. This parameter is guaranteed by design but not tested.

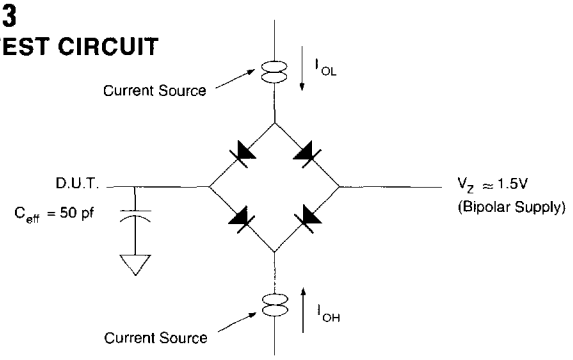
AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		-35		-45		Units
Write Cycle		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		45		nS
Chip Select to End of Write	t_{CW}	20		30		40		nS
Address Valid to End of Write	t_{AW}	20		30		40		nS
Data Valid to End of Write	t_{DW}	15		18		20		nS
Write Pulse Width	t_{WP}	20		25		35		nS
Address Setup Time	t_{AS}	0		0		0		nS
Address Hold Time	t_{AH}	0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}[1]		10		15		15	nS
Data Hold from Write Time	t_{DH}	0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT

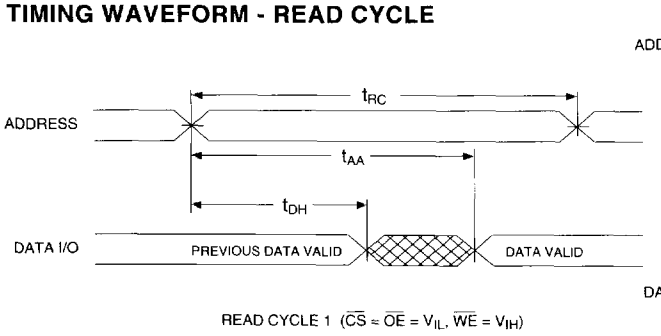


AC TEST CONDITIONS

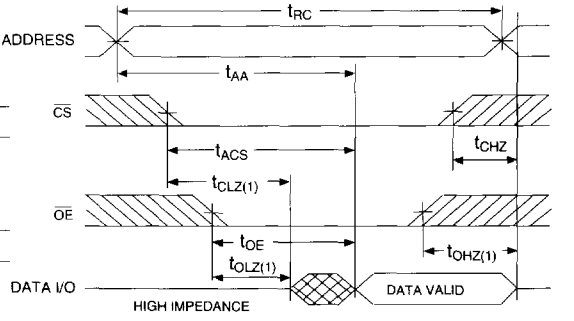
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 4
TIMING WAVEFORM - READ CYCLE



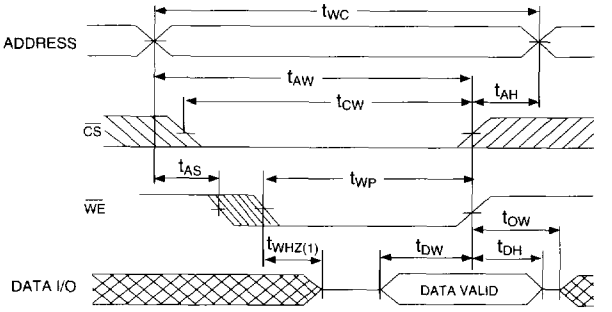
READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



READ CYCLE 2 ($\overline{WE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

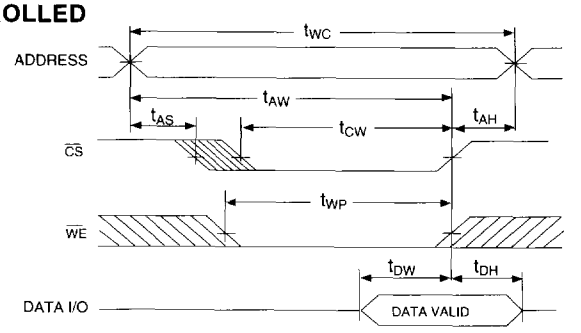
FIG. 5
WRITE CYCLE - $\overline{WE}$ CONTROLLED (OE IS INACTIVE - HIGH)



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED ($\overline{OE}$ = V_{IH})

(1) GUARANTEED BY DESIGN BUT NOT TESTED

FIG. 6
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED ($\overline{OE}$ = V_{IH})

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

FIG. 7
PACKAGE DIMENSIONS (16A06)

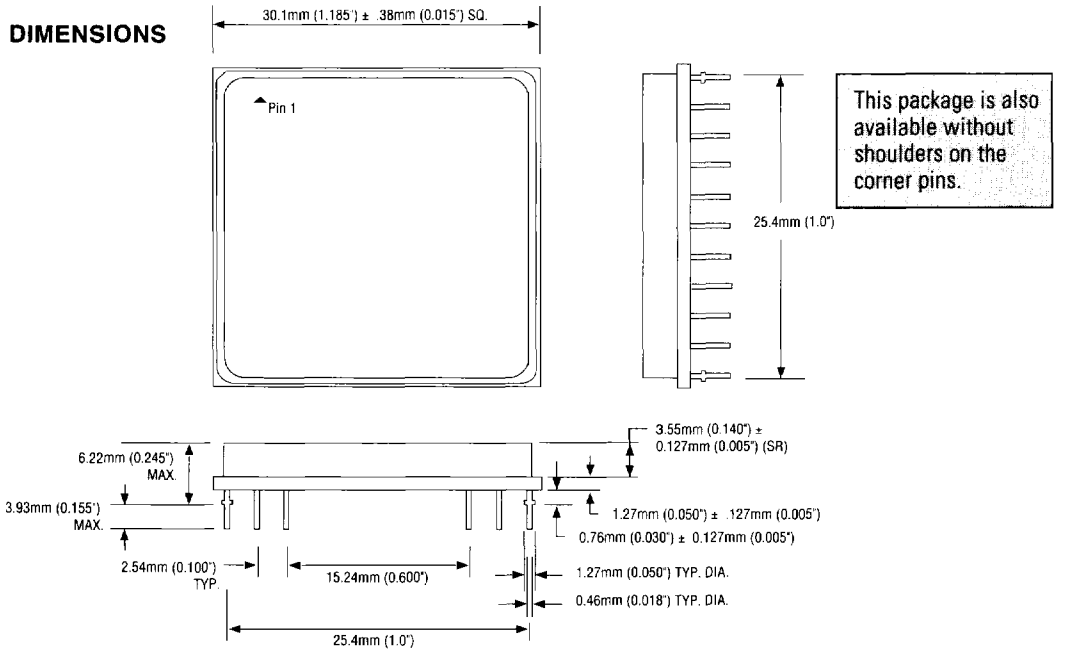
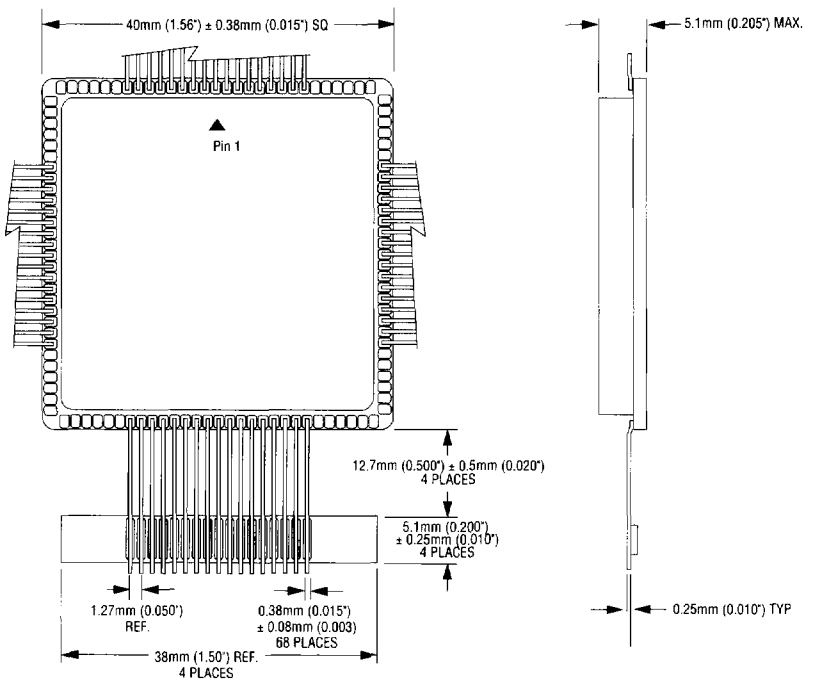
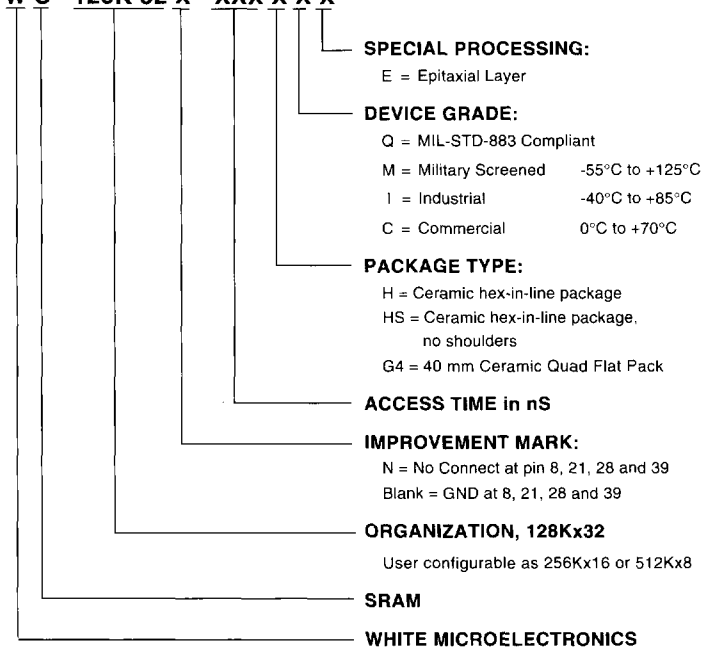


FIG.8
PACKAGE DIMENSIONS (14A15)



ORDERING INFORMATION



Device Type	Speed	Package	SMD Number
128K x 32 SRAM	45nS	66 pin HIP	5962 93187-06HXX
128K x 32 SRAM	35nS	66 pin HIP	5962 93187-07HXX
128K x 32 SRAM	25nS	66 pin HIP	5962 93187-08HXX