

CD40102BMS CD40103BMS

CMOS 8-Stage Presettable Synchronous Down Counters

December 1992

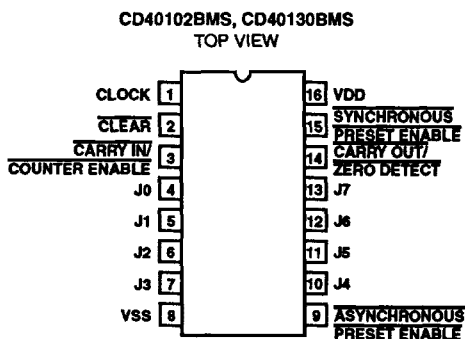
Features

- High Voltage Type (20V Rating)
- CD40102BMS: 2-Decade BCD Type
- CD40103BMS: 8-Bit Binary Type
- Synchronous or Asynchronous Preset
- Medium Speed Operation
 - $f_{CL} = 3.6\text{MHz}$ (Typ) at 10V
- Cascadable
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of $1\mu\text{A}$ at 18V Over Full Package Temperature Range; 100nA at 18V and $+25^\circ\text{C}$
- Noise Margin (Over Full Package/Temperature Range)
 - 1V at $V_{DD} = 5\text{V}$
 - 2V at $V_{DD} = 10\text{V}$
 - 2.5V at $V_{DD} = 15\text{V}$
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Divide-By- "N" Counters
- Programmable Times
- Interrupt Timers
- Cycle/Program Counter

Pinout



Description

CD40102BMS and CD40103BMS consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102BMS is configured as two cascaded 4-bit BCD counters, and the CD40103BMS contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) inputs is high. The CARRY-OUT/ZERO-DETECT ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE (\overline{SPE}) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the ASYNCHRONOUS PRESET-ENABLE (\overline{APE}) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the \overline{SPE} , $\overline{CI/CE}$, or CLOCK inputs. JAM inputs J0-J7 represent two 4-bit BCD words for the CD40102BMS and a single 8-bit binary word for the CD40103BMS.

When the CLEAR (\overline{CLR}) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the CD40102BMS and 255_{10} for the CD40103BMS) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except $\overline{CI/CE}$ are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

This causes the $\overline{CO/ZD}$ output to go low to enable the clock on each succeeding clock pulse.

The CD40102BMS and CD40103BMS may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode as shown in Figures 16 and 17.

The CD40102MS and CD40103BMS are supplied in these 16-lead outline packages:

| | | |
|------------------|----------------|------|
| Braze Seal DIP | *H4W | †H4X |
| Frit Seal DIP | *H1L | †H1F |
| Ceramic Flatpack | H6W | |
| *CD40102B Only | †CD40130B Only | |

Specifications CD40102BMS, CD40103BMS

Absolute Maximum Ratings

| | |
|---|--|
| DC Supply Voltage Range, (VDD) | -0.5V to +20V (Voltage Referenced to VSS Terminals) |
| Input Voltage Range, All Inputs | -0.5V to VDD +0.5V |
| DC Input Current, Any One Input | ±10mA |
| Operating Temperature Range | -55°C to +125°C Package Types D, F, K, H |
| Storage Temperature Range (TSTG) | -65°C to +150°C |
| Lead Temperature (During Soldering) | +265°C |
| At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum | |

Reliability Information

| | | |
|---|---|---------------|
| Thermal Resistance | θ_{JA} | θ_{JC} |
| Ceramic DIP Package | 80°C/W | 20°C/W |
| Flatpack Package | 70°C/W | 20°C/W |
| Maximum Package Power Dissipation (PD) at +125°C | | |
| For T _A = -55°C to +100°C (Package Type D, F, K) | 500mW | |
| For T _A = +100°C to +125°C (Package Type D, F, K) | Derate Linearity at 12mW/°C to 200mW | |
| Device Dissipation per Output Transistor | 100mW | |
| For T _A = Full Package Temperature Range (All Package Types) | | |
| Junction Temperature | +175°C | |

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1) | | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|-----------------------------|--------|------------------------------------|-----------|----------------------|----------------------|----------------|----------------|-------|
| | | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | | 1 | +25°C | - | 10 | μA |
| | | | | 2 | +125°C | - | 1000 | μA |
| | | VDD = 18V, VIN = VDD or GND | | 3 | -55°C | - | 10 | μA |
| Input Leakage Current | IIL | VIN = VDD or GND | VDD = 20V | 1 | +25°C | -100 | - | nA |
| | | | VDD = 18V | 2 | +125°C | -1000 | - | nA |
| | | | | 3 | -55°C | -100 | - | nA |
| Input Leakage Current | IIH | VIN = VDD or GND | VDD = 20V | 1 | +25°C | - | 100 | nA |
| | | | VDD = 18V | 2 | +125°C | - | 1000 | nA |
| | | | | 3 | -55°C | - | 100 | nA |
| Output Voltage | VOL15 | VDD = 15V, No Load | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH15 | VDD = 15V, No Load (Note 3) | | 1, 2, 3 | +25°C, +125°C, -55°C | 14.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | | 1 | +25°C | 0.53 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | | 1 | +25°C | 1.4 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | | 1 | +25°C | 3.5 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | | 1 | +25°C | - | -0.53 | mA |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | | 1 | +25°C | - | -1.8 | mA |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | | 1 | +25°C | - | -1.4 | mA |
| Output Current (Source) | IOH15 | VDD = 15V, VOUT = 13.5V | | 1 | +25°C | - | -3.5 | mA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10μA | | 1 | +25°C | -2.8 | -0.7 | V |
| P Threshold Voltage | VPTH | VSS = 0V, IDD = 10μA | | 1 | +25°C | 0.7 | 2.8 | V |
| Functional | F | VDD = 2.8V, VIN = VDD or GND | | 7 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| | | VDD = 20V, VIN = VDD or GND | | 7 | +25°C | | | |
| | | VDD = 18V, VIN = VDD or GND | | 8A | +125°C | | | |
| | | VDD = 3V, VIN = VDD or GND | | 8B | -55°C | | | |
| Input Voltage Low (Note 2) | VIL | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 1.5 | V |
| Input Voltage High (Note 2) | VIH | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 3.5 | - | V |
| Input Voltage Low (Note 2) | VIL | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 4 | V |
| Input Voltage High (Note 2) | VIH | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 11 | - | V |

- NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
2. Go/No Go test with limits applied to inputs.

7

LOGIC

Specifications CD40102BMS, CD40103BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1, 2) | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|--|----------------|----------------------------|-------------------|---------------|--------|------|-------|
| | | | | | MIN | MAX | |
| Propagation Delay Clock to Output | TPHL1 TPLH1 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 600 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 810 | ns |
| Propagation Delay Carry In/Counter Enable to Output | TPHL2 TPLH2 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 400 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 540 | ns |
| Propagation Delay Asynchronous Preset Enable to Output | TPHL3 TPLH3 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 1300 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 1755 | ns |
| Propagation Delay Clear to Output | TPLH4 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 750 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 1012 | ns |
| Transition Time | TTHL TTLH | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 200 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 270 | ns |
| Maximum Clock Input Frequency | FCL | VDD = 5V, VIN = VDD or GND | 9 | +25°C | .7 | - | MHz |
| | | | 10, 11 | +125°C, -55°C | .52 | - | MHz |

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|-------------------------|--------|-----------------------------|-------|----------------------|--------|-------|-------|
| | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 5V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 5 | µA |
| | | | | +125°C | - | 150 | µA |
| | | VDD = 10V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 10 | µA |
| | | | | +125°C | - | 300 | µA |
| | | VDD = 15V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 10 | µA |
| | | | | +125°C | - | 600 | µA |
| Output Voltage | VOL | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOL | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | 4.95 | - | V |
| Output Voltage | VOH | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | 9.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | 1, 2 | +125°C | 0.36 | - | mA |
| | | | | -55°C | 0.64 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | 1, 2 | +125°C | 0.9 | - | mA |
| | | | | -55°C | 1.6 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | 1, 2 | +125°C | 2.4 | - | mA |
| | | | | -55°C | 4.2 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | 1, 2 | +125°C | - | -0.36 | mA |
| | | | | -55°C | - | -0.64 | mA |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | 1, 2 | +125°C | - | -1.15 | mA |
| | | | | -55°C | - | -2.0 | mA |

Specifications CD40102BMS, CD40103BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|--|----------------|-------------------------------|---------|----------------------|--------|------|-------|
| | | | | | MIN | MAX | |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | 1, 2 | +125°C | - | -0.9 | mA |
| | | | | -55°C | - | -1.6 | mA |
| Output Current (Source) | IOH15 | VDD = 15V, VOUT = 13.5V | 1, 2 | +125°C | - | -2.4 | mA |
| | | | | -55°C | - | -4.2 | mA |
| Input Voltage Low | VIL | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | - | 3 | V |
| Input Voltage High | VIH | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | 7 | - | V |
| Propagation Delay Clock to Output | TPHL1 TPLH1 | VDD = 10V | 1, 2, 3 | +25°C | - | 260 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 190 | ns |
| Propagation Delay Carry In/Counter Enable to Output | TPHL2 TPLH2 | VDD = 10V | 1, 2, 3 | +25°C | - | 180 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 130 | ns |
| Propagation Delay Asynchronous Preset En- able to Output | TPHL3 TPLH3 | VDD = 10V | 1, 2, 3 | +25°C | - | 600 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 400 | ns |
| Propagation Delay Clear to Output | TPLH4 | VDD = 10V | 1, 2, 3 | +25°C | - | 360 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 200 | ns |
| Transition Time | TTHL1 TTLH1 | VDD = 10V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 80 | ns |
| Maximum Clock Input Frequency | FCL | VDD = 10V | 1, 2 | +25°C | 1.8 | - | MHz |
| | | VDD = 15V | 1, 2 | +25°C | 2.4 | - | MHz |
| Minimum \overline{SPE} Setup Time | TSU | VDD = 5V | 1, 2, 3 | +25°C | - | 280 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 140 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 100 | ns |
| Minimum $\overline{C/CE}$ Setup Time | TSU | VDD = 5V | 1, 2, 3 | +25°C | - | 500 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 250 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 150 | ns |
| Minimum Clock Pulse Width | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 300 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 180 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 80 | ns |
| Minimum \overline{APE} Pulse Width | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 360 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 160 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 120 | ns |
| Minimum JAM Setup Time (Synchronous Pre- setting) | TSU | VDD = 5V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 80 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 60 | ns |
| Minimum \overline{APE} Removal Time | TREM | VDD = 5V | 1, 2, 3 | +25°C | - | 220 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 70 | ns |
| Minimum \overline{CLR} Pulse Width | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 320 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 160 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 100 | ns |

Specifications CD40102BMS, CD40103BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|-------------------|--------|------------|-------|-------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Input Capacitance | CIN | Any Input | 1, 2 | +25°C | - | 7.5 | pF |

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---------------------------|--------------|---|------------|-------------|-------------|--------------------|-------|
| | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | 1, 4 | +25°C | - | 25 | μA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10μA | 1, 4 | +25°C | -2.8 | -0.2 | V |
| N Threshold Voltage Delta | ΔVTN | VDD = 10V, ISS = -10μA | 1, 4 | +25°C | - | ±1 | V |
| P Threshold Voltage | VTP | VSS = 0V, IDD = 10μA | 1, 4 | +25°C | 0.2 | 2.8 | V |
| P Threshold Voltage Delta | ΔVTP | VSS = 0V, IDD = 10μA | 1, 4 | +25°C | - | ±1 | V |
| Functional | F | VDD = 18V, VIN = VDD or GND VDD = 3V, VIN = VDD or GND | 1 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| Propagation Delay Time | TPHL TPLH | VDD = 5V | 1, 2, 3, 4 | +25°C | - | 1.35 x +25°C Limit | ns |

- NOTES:**
1. All voltages referenced to device GND.
 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
 3. See Table 2 for +25°C limit.
 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

| PARAMETER | SYMBOL | DELTA LIMIT |
|-------------------------|--------|--------------------------|
| Supply Current - MSI-2 | IDD | ± 1.0μA |
| Output Current (Sink) | IOL5 | ± 20% x Pre-Test Reading |
| Output Current (Source) | IOH5A | ± 20% x Pre-Test Reading |

TABLE 6. APPLICABLE SUBGROUPS

| CONFORMANCE GROUP | MIL-STD-883 METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|-------------------------------|--------------------|-------------------------------|------------------|
| Initial Test (Pre Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 1 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 2 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | 100% 5004 | 1, 7, 9, Deltas | |
| Interim Test 3 (Post Burn-In) | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | 100% 5004 | 1, 7, 9, Deltas | |
| Final Test | 100% 5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |

Specifications CD40102BMS, CD40103BMS

TABLE 6. APPLICABLE SUBGROUPS (Continued)

| CONFORMANCE GROUP | | MIL-STD-883 METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|-------------------|--------------|--------------------|---------------------------------------|------------------------------|
| Group B | Subgroup B-5 | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11 |
| | Subgroup B-6 | Sample 5005 | 1, 7, 9 | |
| Group D | | Sample 5005 | 1, 2, 3, 8A, 8B, 9 | Subgroups 1, 2, 3 |

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

| CONFORMANCE GROUPS | MIL-STD-883 METHOD | TEST | | READ AND RECORD | |
|--------------------|--------------------|-----------|------------|-----------------|------------|
| | | PRE-IRRAD | POST-IRRAD | PRE-IRRAD | POST-IRRAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 |

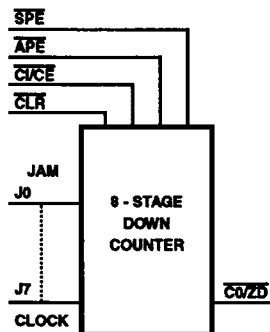
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

| FUNCTION | OPEN | GROUND | VDD | 9V ± 0.5V | OSCILLATOR | |
|------------------------------------|------|------------|-----------------------|-----------|-----------------|-----------------|
| | | | | | 50kHz | 25kHz |
| PART NUMBER CD40102BMS, CD40103BMS | | | | | | |
| Static Burn-In 1 Note 1 | 14 | 1 - 13, 15 | 16 | | | |
| Static Burn-In 2 Note 1 | 14 | 8 | 1 - 7, 9 - 13, 15, 16 | | | |
| Dynamic Burn-In Note 1 | - | 3, 8, 15 | 2, 16 | 14 | 1, 4, 6, 11, 13 | 5, 7, 9, 10, 12 |
| Irradiation Note 2 | - | | | | | |

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Functional Diagram



CD40102BMS, CD40103BMS

Logic Diagrams

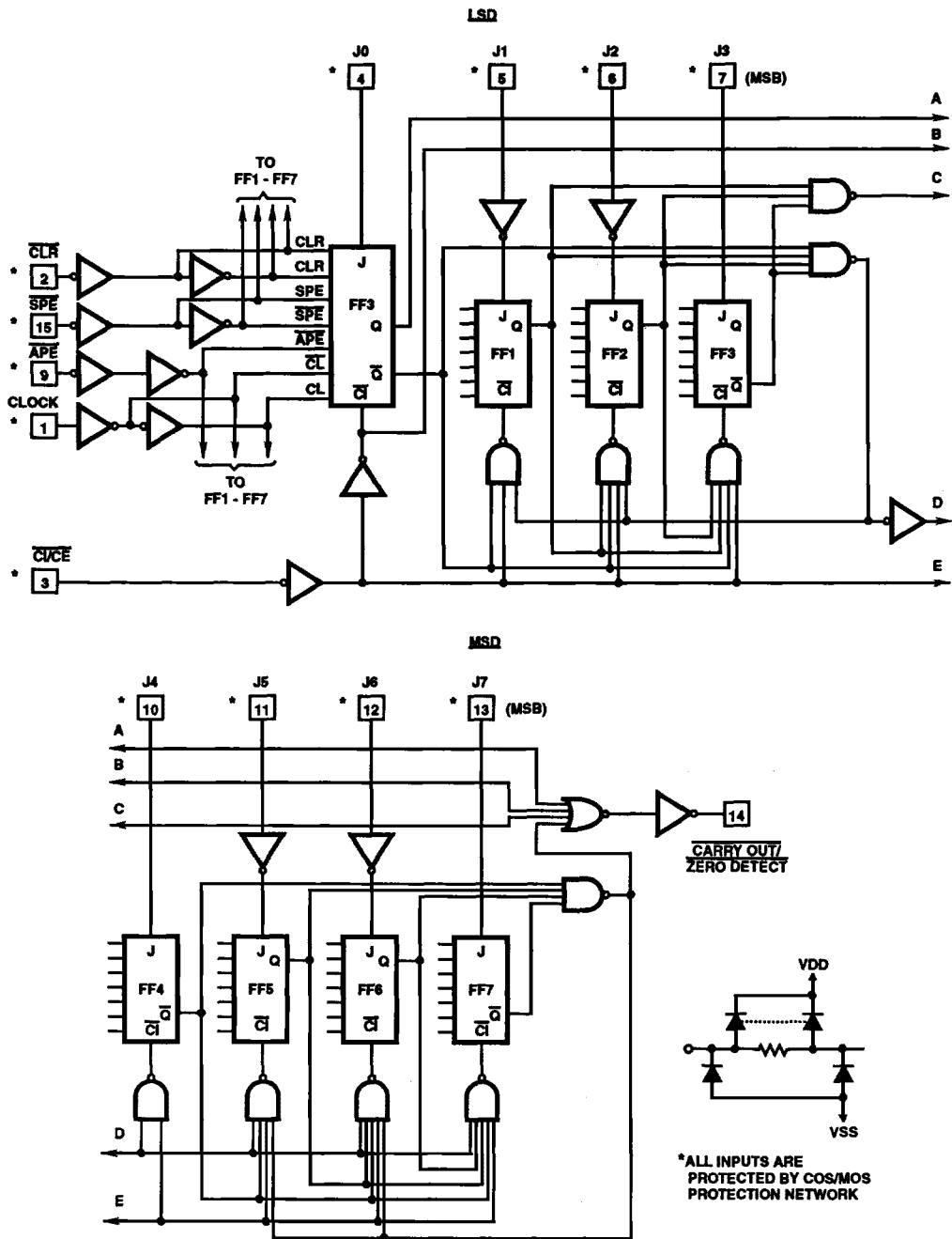


FIGURE 1. LOGIC DIAGRAM FOR CD40102BMS

CD40102BMS, CD40103BMS

TRUTH TABLE

| CONTROL INPUTS | | | | PRESET MODE | ACTION |
|----------------|--------------|--------------|--------------------|--------------|--|
| CLR | AP \bar{E} | SP \bar{E} | \bar{C}/\bar{CE} | | |
| 1 | 1 | 1 | 1 | Synchronous | Inhibit Counter |
| 1 | 1 | 1 | 0 | | Count Down* |
| 1 | 1 | 0 | X | | Preset on next positive clock transition |
| 1 | 0 | X | X | Asynchronous | Preset Asynchronously |
| 0 | X | X | X | | Clear to maximum count |

NOTES:

1. 0 = Low Level
1 = High Level
X = Don't Care
2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40102BMS;
MSD = J7, J6, J5, J4, (J7 is MSB)
LSD = J3, J2, J1, J0 (J3 is MSB)
CD40103BMS Binary;
MBS = J7, LSB = J0

*At zero count, the counters will jump to the maximum count on the next clock transition to "High"

Typical Performance Characteristics

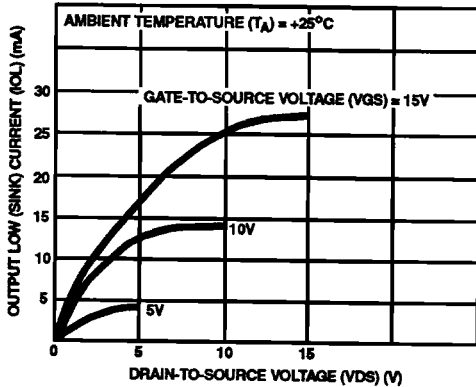


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

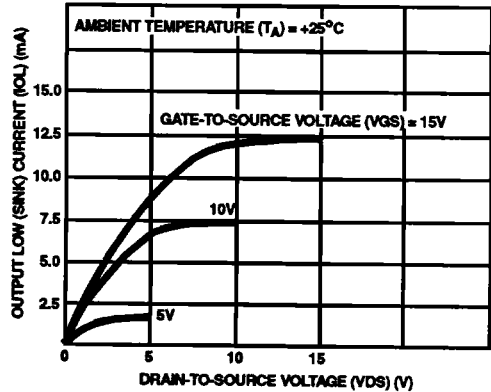


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

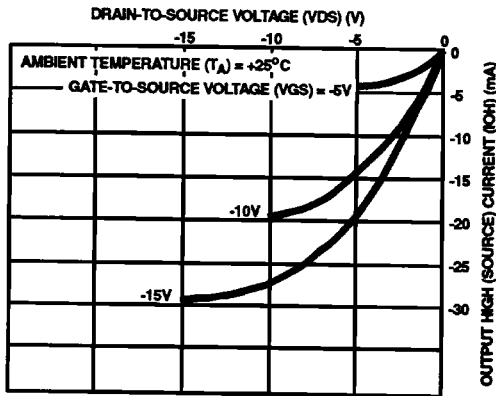


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

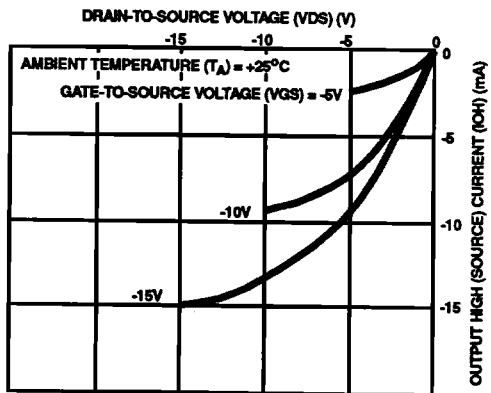


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

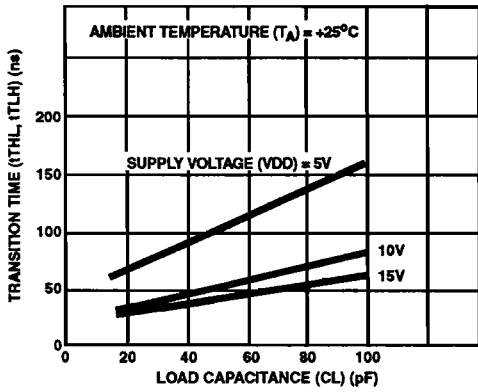


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

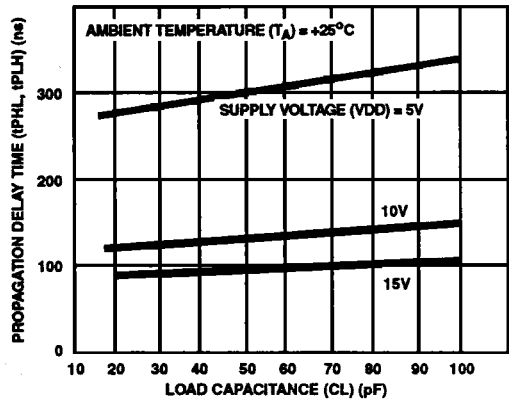


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO CO/ZD)

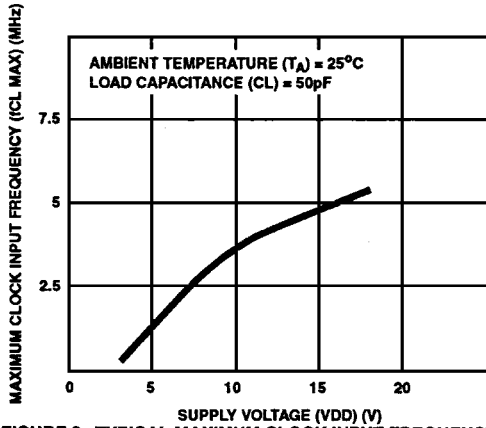


FIGURE 9. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

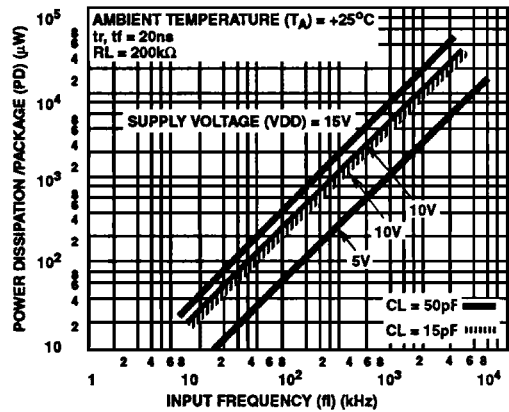


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF FREQUENCY

CD40102BMS, CD40103BMS

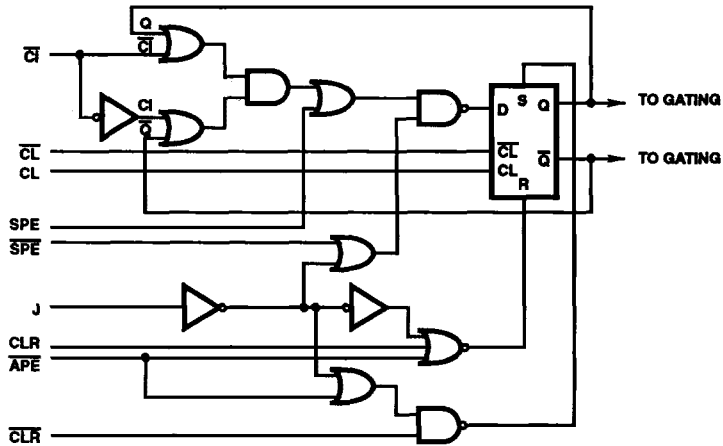


FIGURE 11. DETAIL LOGIC DIAGRAM FOR FLIP-FLOPS, FF0 - FF7, USED IN LOGIC DIAGRAMS FOR CD40102BMS AND CD40103BMS

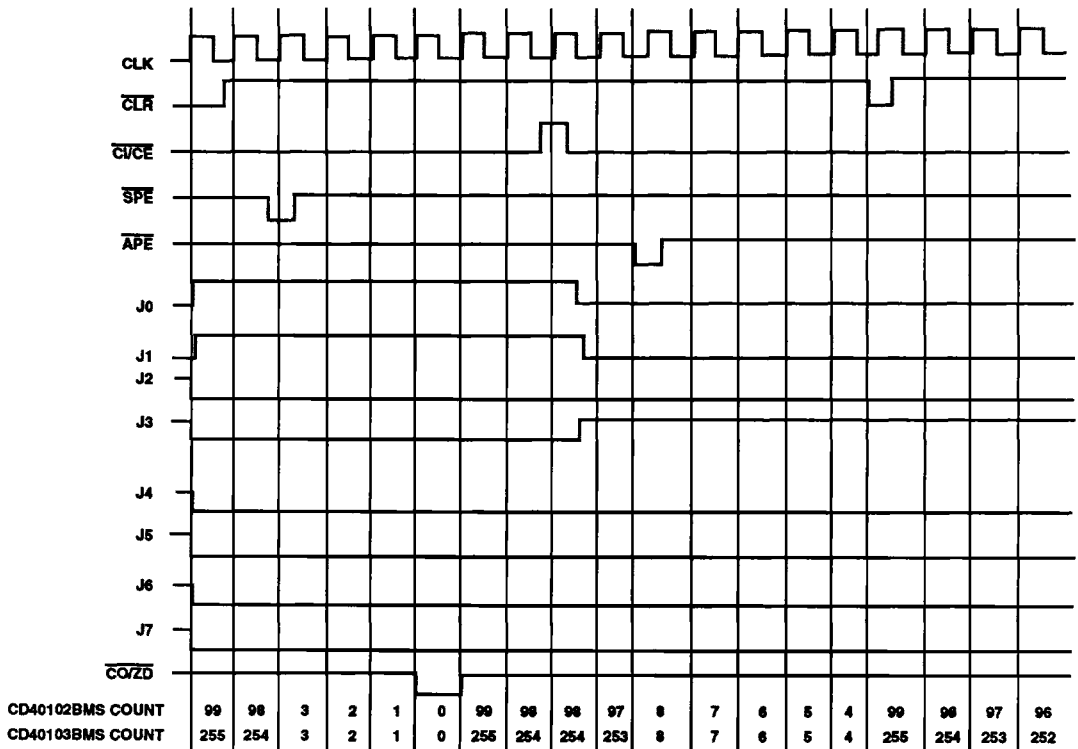


FIGURE 12. TIMING DIAGRAM FOR CD40102BMS AND CD40103BMS

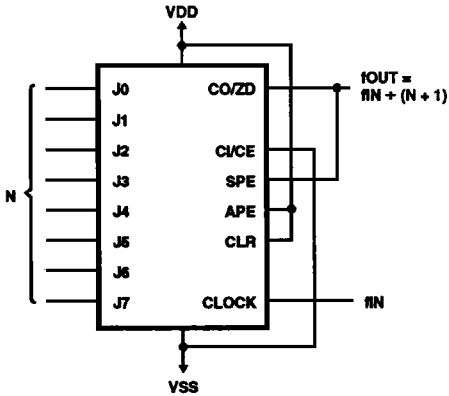


FIGURE 13. DIVIDE-BY- "N" COUNTER

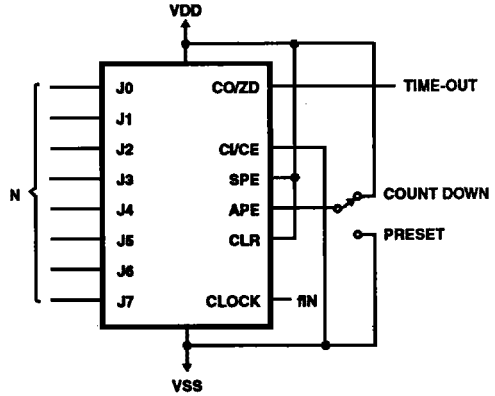


FIGURE 14. PROGRAMMABLE TIMER

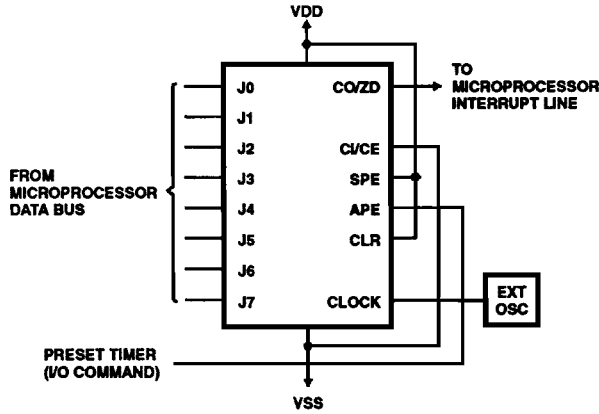
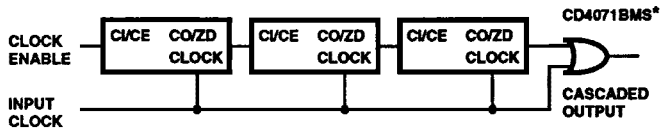


FIGURE 15. MICROPROCESSOR INTERRUPT TIMER



*An output spike (180ns at VDD = 5V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

FIGURE 16. SYNCHRONOUS CASCADING

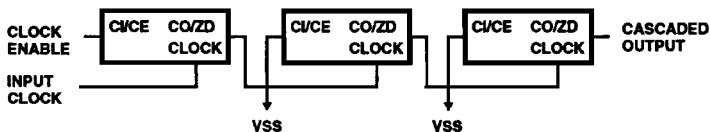
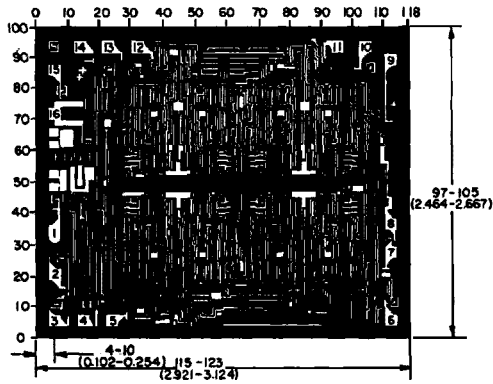


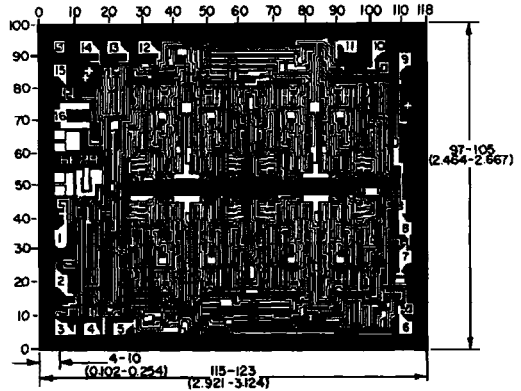
FIGURE 17. RIPPLE CASCADING

CD40102BMS, CD40103BMS

Chip Dimensions and Pad Layouts



CD40102BMS



CD40103BMS

Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10-3 inch).

METALLIZATION: Thickness: $11\text{k}\text{\AA}$ - $14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA}$ - $15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches