Integrated Device Technology, Inc.

3.3V CMOS OCTAL BUFFER/LINE DRIVER

PRELIMINARY
IDT54/74FCT3244/A

FEATURES:

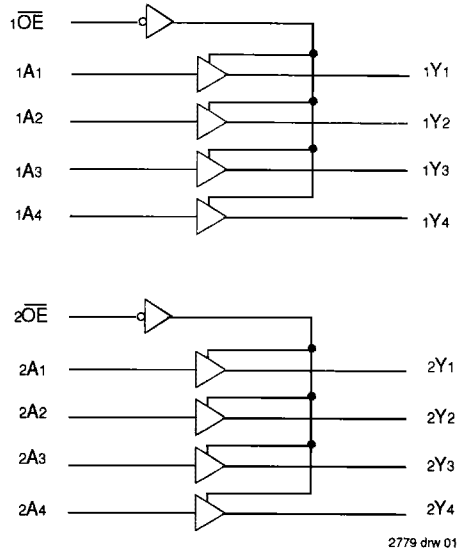
- 0.5 MICRON CEMOS™ Technology
- **Can serve as 5V to 3.3V translator**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The IDT54/74FCT3244/A octal buffer/line drivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power buffers are designed to be used as memory data and address drivers, clock drivers, and bus-oriented transmitter/receivers. The three-state controls are designed to operate these devices in a dual-nibble or single-byte mode. All inputs are designed with hysteresis for improved noise margin.

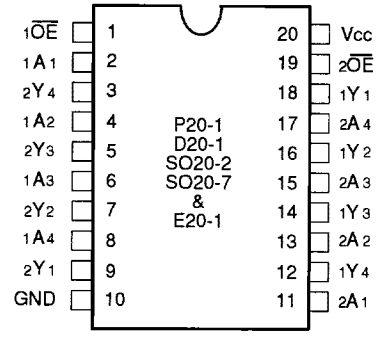
The data(xAx) and output enable ($x\overline{OE}$) inputs of these buffers can be driven from either 3.3V or 5V devices. This feature enables the IDT54/74FCT3244/A buffers to be used as 5V to 3.3V unidirectional translators in a 5V/3.3V mixed supply system.

FUNCTIONAL BLOCK DIAGRAM

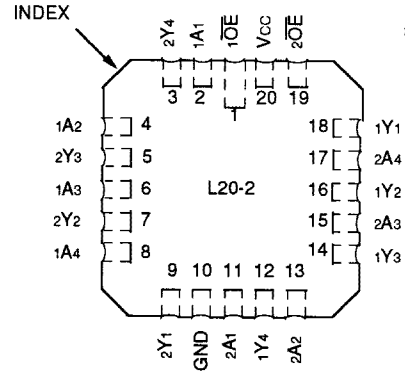


2779 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

2779 drw 02

2779 drw 03

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PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

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FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2779 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 2779 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2779 lnk 04
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} -0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} − 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open 50% Duty Cycle $x\overline{OE}$ = GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	85	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	0.7	2.4	mA
		50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = 2.4V V_{IN} = GND	—	0.7	2.6	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	1.3	3.3[5]	
		50% Duty Cycle $x\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 2.4V V_{IN} = GND	—	1.5	5.2[5]	

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NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT3244				FCT3244A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

2779 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.