PRELIMINARY

CY7C101A
CY7C102A

256K x 4 Static RAM with Separate I/O

Features

- **High speed**
  - **—t_{AA} = 12 ns**
- **Transparent write (7C101A)**
- **CMOS for optimum speed/power**
- **Low active power**
  - **—910 mW**
- **Low standby power**
  - **—275 mW**
- **2.0V data retention (optional)**
  - **—100 µW**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C101A and CY7C102A are high-performance CMOS static RAMs organized as 262,144 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by more than 65% when deselected.

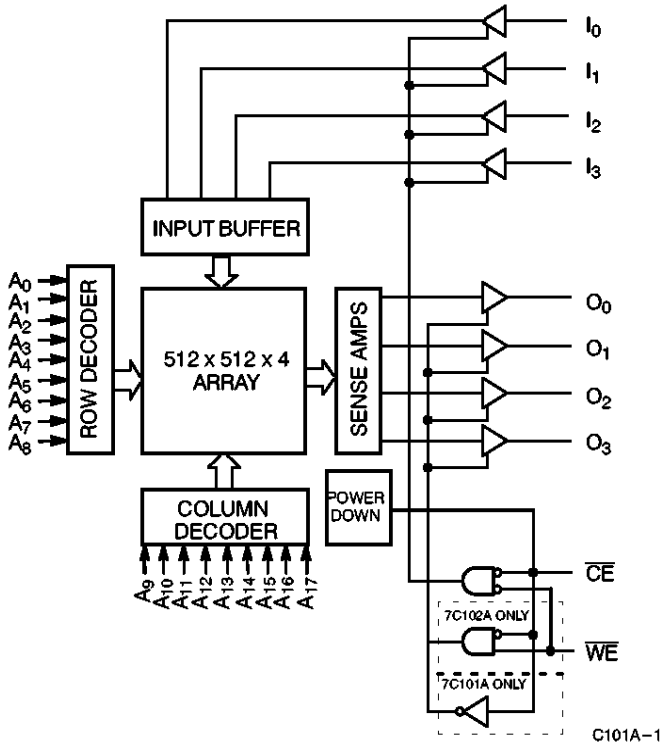
Writing to the device is accomplished by taking both chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

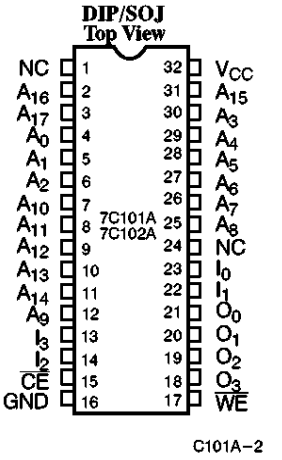
The data output pins on the CY7C101A and the CY7C102A are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH). The CY7C102A's outputs are also placed in a high-impedance state during a write operation ($\overline{CE}$ and $\overline{WE}$ LOW). In a write operation on the CY7C101A, the output pins will carry the same data as the inputs after a specified delay.

The CY7C101A and CY7C102A are available in standard 400-mil-wide DIPs and SOJs.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C101A–12 7C102A–12	7C101A–15 7C102A–15	7C101A–20 7C102A–20	7C101A–25 7C102A–25	7C101A–35 7C102A–35
Maximum Access Time (ns)		12	15	20	25	35
Maximum Operating Current (mA)	Commercial	165	155	140	130	125
	Military		165	150	140	135
Maximum Standby Current (mA)	Commercial	50	40	30	30	25
	Military		40	30	30	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[1] ..... −0.5V to V_{CC} +0.5V

DC Input Voltage[1] ..... −0.5V to V_{CC} +0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Notes:

1. V_{IL} (min.) = −2.0V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C101A−12 7C102A−12 Min.	7C101A−12 7C102A−12 Max.	7C101A−15 7C102A−15 Min.	7C101A−15 7C102A−15 Max.	7C101A−20 7C102A−20 Min.	7C101A−20 7C102A−20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		165		155		140	mA
			Mil				165		150	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		50		40		30	mA
			Mil				40		30	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2		2	mA
			Mil				2		2	

Electrical Characteristics Over the Operating Range[3] (continued)

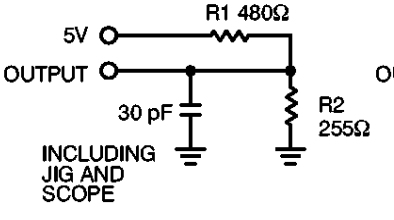
Parameter	Description	Test Conditions		7C101A–25 7C102A–25 Min.	7C101A–25 7C102A–25 Max.	7C101A–35 7C102A–35 Min.	7C101A–35 7C102A–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			−0.3	0.8	−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1	+1	−1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−5	+5	−5	+5	µA
I_{OS}	Output Short Circuit Current[NO TAG]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		130		125	mA
			Mil		140		135	
I_{SB1}	Automatic CE Power-Down Current — TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l		30		25	mA
			Mil		30		25	
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f=0	Com'l		2		2	mA
			Mil		2		2	

Capacitance[5]

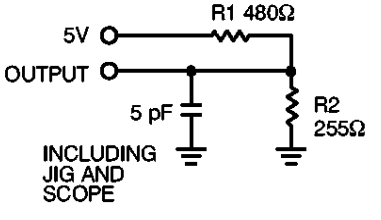
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

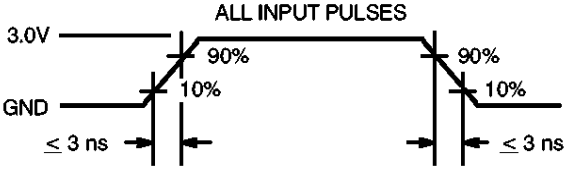
AC Test Loads and Waveforms



(a)

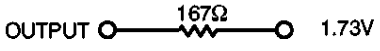


(b) C101A–3



C101A–4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3, 6]

Parameter	Description	7C101A–12 7C102A–12		7C101A–15 7C102A–15		7C101A–20 7C102A–20		7C101A–25 7C102A–25		7C101A–35 7C102A–35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	12		15		20		25		35		ns
t_{AA}	Address to Data Valid		12		15		20		25		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		6		7		8		10		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	12		15		20		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		15		20		25		ns
t_{AW}	Address Set-Up to Write End	10		12		15		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		20		25		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		6		7		8		10		10	ns
t_{DWE}	$\overline{WE}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t_{DCE}	$\overline{CE}$ LOW to Data Valid (7C101A)		12		15		20		25		35	ns
t_{ADV}	Data Valid to Output Valid (7C101A)		12		15		20		25		35	ns

Notes:

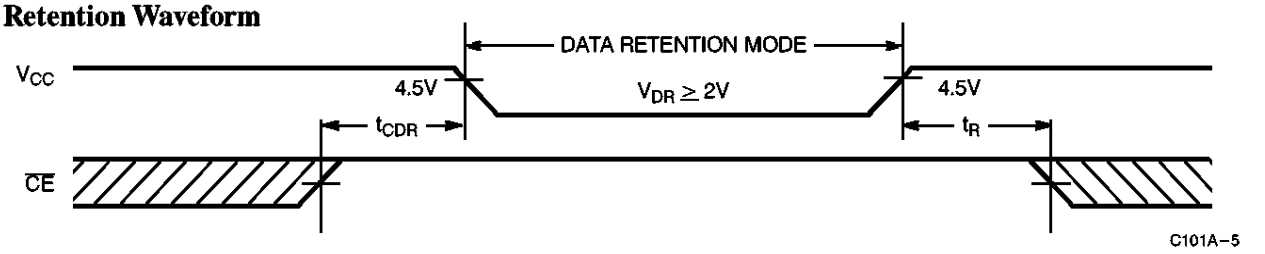
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Conditions[10]	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data		2.0		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3$ or $V_{IN} \leq 0.3V$		50		70	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		t_{RC}		t_{RC}		ns

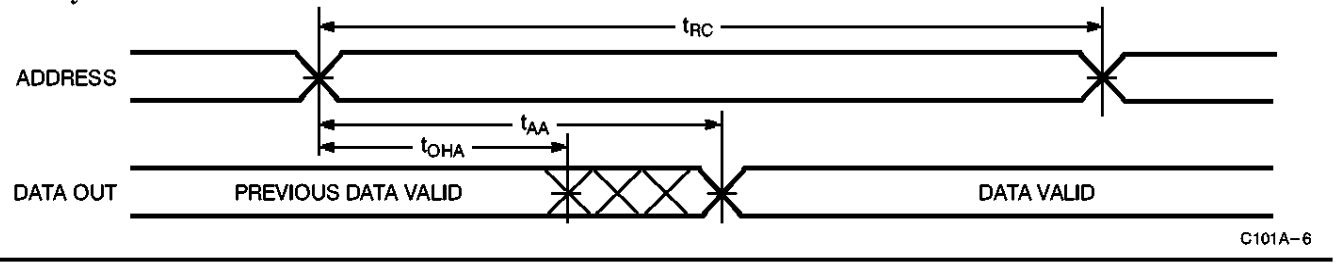
Note:
10. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

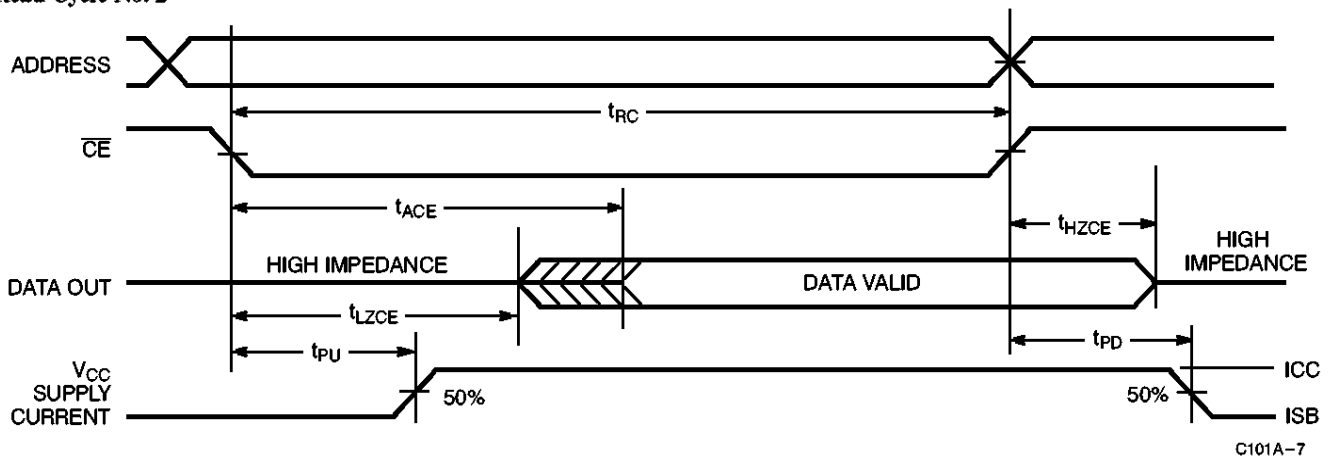


Switching Waveforms

Read Cycle No. 1[11, 12]



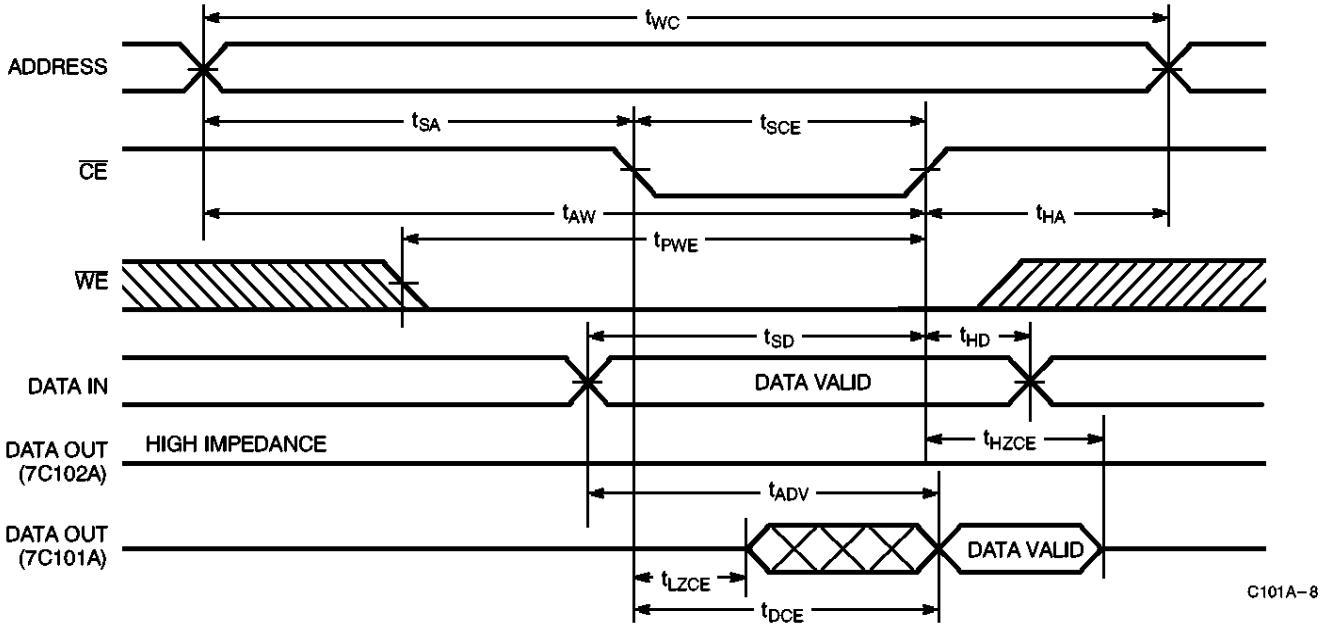
Read Cycle No. 2[12, 13]



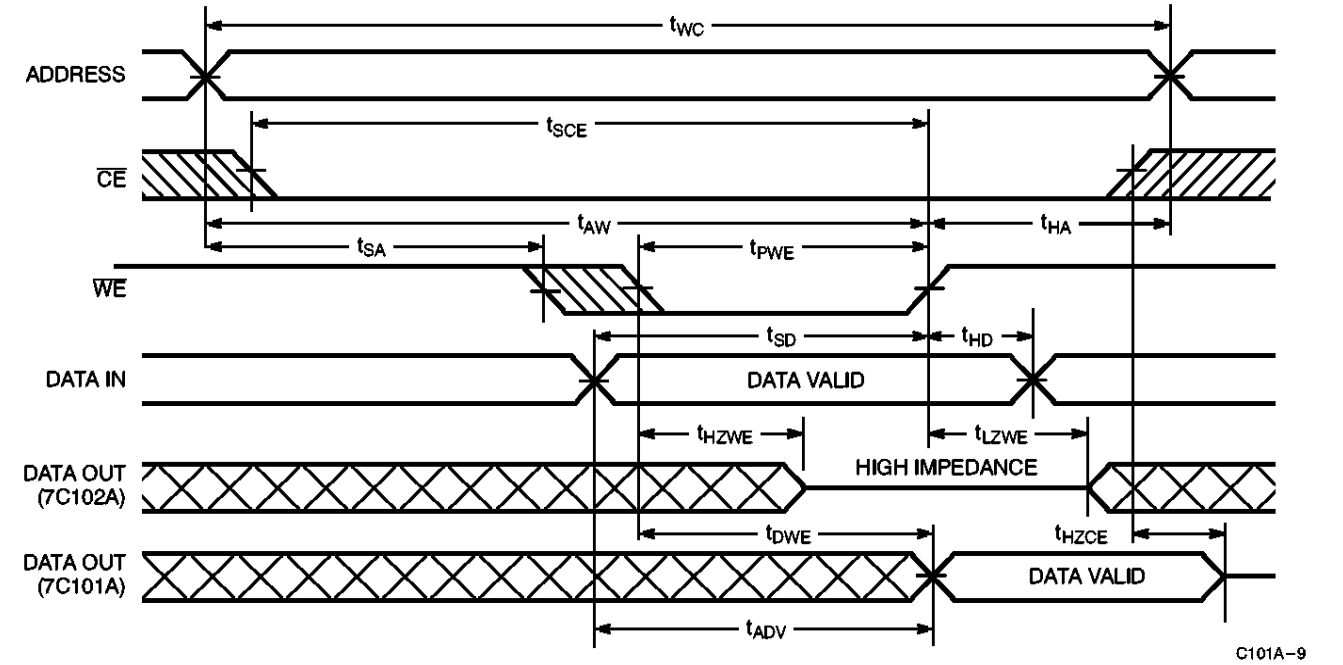
Notes:
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[9, 14]



Write Cycle No. 2 ($\overline{WE}$ Controlled)[9]



Note:
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state (7C102A only).

Truth Table

$\overline{CE}$	$\overline{WE}$	$O_0 - O_3$	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	High Z	7C102A: Standard Write	Active (I_{CC})
L	L	Input Tracking	7C101A: Transparent Write[15]	Active (I_{CC})

Note:
15. Outputs track inputs after specified delay.

Ordering Information

Speed (ns)	Ordering Code	Package Name	PackageType	Operating Range
12	CY7C101A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C101A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C101A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C101A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C101A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C101A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C101A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

Contact factory for "L" version availability.

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C102A–12PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C102A–15PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–15VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–15DMB	D44	32-Lead (400-Mil) CerDIP	Military
20	CY7C102A–20PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–20VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–20DMB	D44	32-Lead (400-Mil) CerDIP	Military
25	CY7C102A–25PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–25VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–25DMB	D44	32-Lead (400-Mil) CerDIP	Military
35	CY7C102A–35PC	P43	32-Lead (400-Mil) Molded DIP	Commercial
	CY7C102A–35VC	V33	32-Lead (400-Mil) Molded SOJ	
	CY7C102A–35DMB	D44	32-Lead (400-Mil) CerDIP	Military

Contact factory for "L" version availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

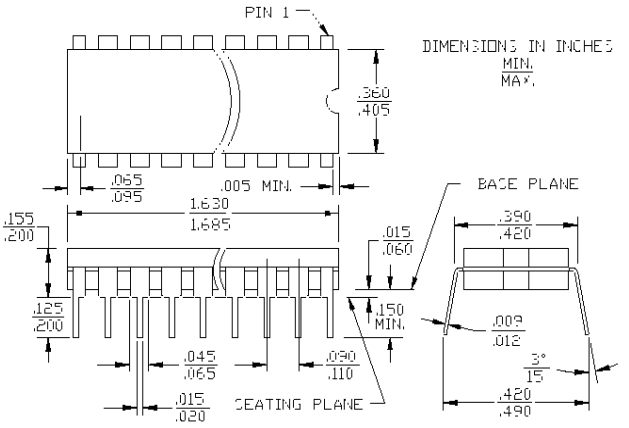
Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{DWE}[16]	7, 8, 9, 10, 11
t_{ADV}[16]	7, 8, 9, 10, 11

Note:
16. 7C101A only.

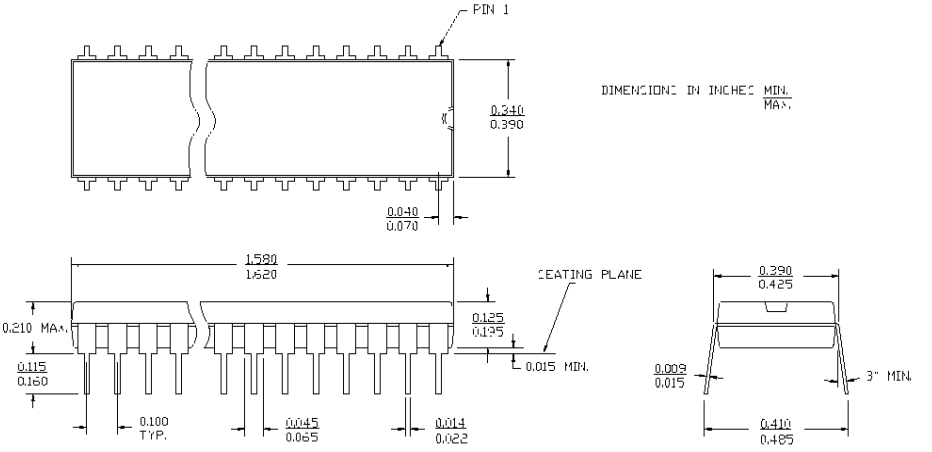
Document #: 38−00231−A

Package Diagrams

32-Lead (400-Mil) CerDIP D44



32-Lead (400-Mil) Molded DIP P43



Package Diagrams (continued)

32-Lead (400-Mil) Molded SOJ V33