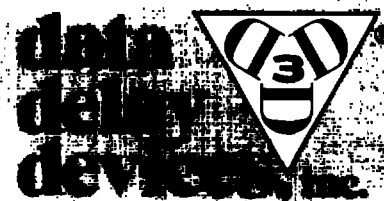


5 Taps — Delay Lines

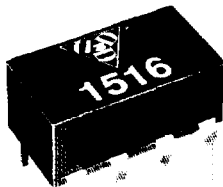
SERIES: **1516 (DIP)**
1516S (SMD)

$$T_D/T_R = 3/1$$



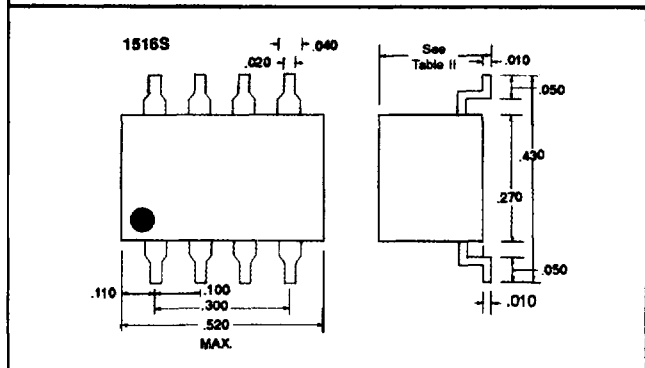
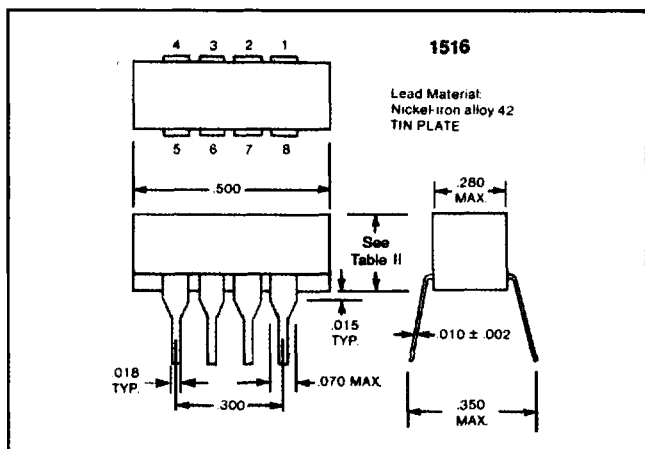
FEATURES:

- 200 ns delay.
- 5 taps.
- Standard 8 pins DIP & SMD cases.
- Low D.C. resistance.
- Fast delivery.



SPECIFICATIONS:

- Delay accuracy: $\pm 5\%$ (others on request)
- No. taps: 5 equally spaced taps
- Taps accuracy: $\pm 5\%$ of tap delay
- Impedance tolerance: $\pm 10\%$ (others on request)
- Rise-time: 30% of time delay
- Withstanding voltage: 50 Vdc min.
- Temperature coefficient: 100 PPM/ $^{\circ}$ C.
- Environment: Meets or exceeds MIL-D-23859C.



PART NUMBER MAKE-UP

SERIES **1516S** MOUNTING HEIGHT CODE **A** DELAY TIME **101** IMPEDANCE **151** PIN SEQUENCE CODE **A**

MOUNTING HEIGHT CODE (see Table II)

DELAY TIME: Expressed in nanoseconds (ns)
 First two digits are significant figures.
 Last digit specifies number of zeros to follow.

IMPEDANCE: Expressed in ohms. First two digits are significant. Last digit specifies number of zeros to follow.

PIN SEQUENCE CODE: (SEE Table III). "STANDARD" Pin sequence if omitted.

TABLE I

Td (ns) ¹	Td/tap (ns) ² ($\pm 5\%$)	Tr (ns) Max.	ATTENUATION (%) TYPICAL PER IMPEDANCE				
			50	100	200	300	500
5	1	3		5			
10	2	4	3	5	5		
15	3	5	3	5	5		
20	4	6	3	5	5	5	
25	5	7	3	5	5	5	7
30	6	10	3	5	5	5	7
40	8	13	3	5	5	5	7
50	10	15	3	5	5	7	7
60	12	20	3	5	6	7	8
75	15	25	3	5	6	7	8
80	16	26	4	5	6	7	8
100	20	30	4	5	6	7	8
110	22	32	4	5	6	7	8
125	25	40	4	5	6	7	8
150	30	50		5	8	10	10
180	36	60		7	8	10	10
200	40	70		8	10	12	12

¹ Or ± 2 ns, whichever is greater.
² Or ± 1 ns, whichever is greater, referenced from input.

TABLE II

MOUNTING HEIGHT	
CODE	DIMENSIONS (MAX)
A	.187
B	.240
C	.290

TABLE III

CODE	IN	20%	40	60%	80%	OUT	GROUND
STANDARD	2	3	4	5	6	7	1, 8
A	1	2	3	4	6	7	5, 8
B	1	7	3	6	4	5	8
C	7	2	6	3	5	4	1, 8
D	1	2	7	3	6	4	5, 8

Other pin sequences available