ULTRA PRECISION DUAL 2:1 CML MUX WITH INTERNAL I/O TERMINATION

Precision Edge® SY58025U

FEATURES

- **Two independent differential 2:1 multiplexers**
- **Guaranteed AC performance over temperature and voltage:**
  - **DC-to >10.7Gbps data rate throughput**
  - **<290ps IN-to-Out t_{pd}**
  - **<70ps t_r / t_f times**
- **Unique, patent-pending input isolation design minimizes crosstalk**
- **Ultra-low jitter design:**
  - **<1ps$_{RMS}$ random jitter**
  - **<10ps$_{PP}$ deterministic jitter**
  - **<10ps$_{PP}$ total jitter (clock)**
  - **<0.7ps$_{RMS}$ crosstalk-induced jitter**
- **Unique, patent-pending 50Ω input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, LVDS, PECL)**
- **Typical 400mV CML output swing (R_L = 50Ω)**
- **Internal 50Ω input termination**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **–40°C to +85°C temperature range**
- **Available in 32-pin (5mm × 5mm) MLF® package**

Precision Edge®

DESCRIPTION

The SY58025U features two ultra-fast, low jitter 2:1 differential muxes with a guaranteed maximum data or clock throughput of 10.7Gbps or 7GHz, respectively.

The SY58025U differential inputs include a unique, internal termination design that allows access to the termination network through a VT pin. The device easily interfaces to different logic standards, both AC- and DC-coupled, without external resistor-bias and termination networks. The result is a clean, stub-free, low jitter interface solution. The differential CML output is optimized for 50Ω environments with internal 50Ω source termination and a 400mV output swing.

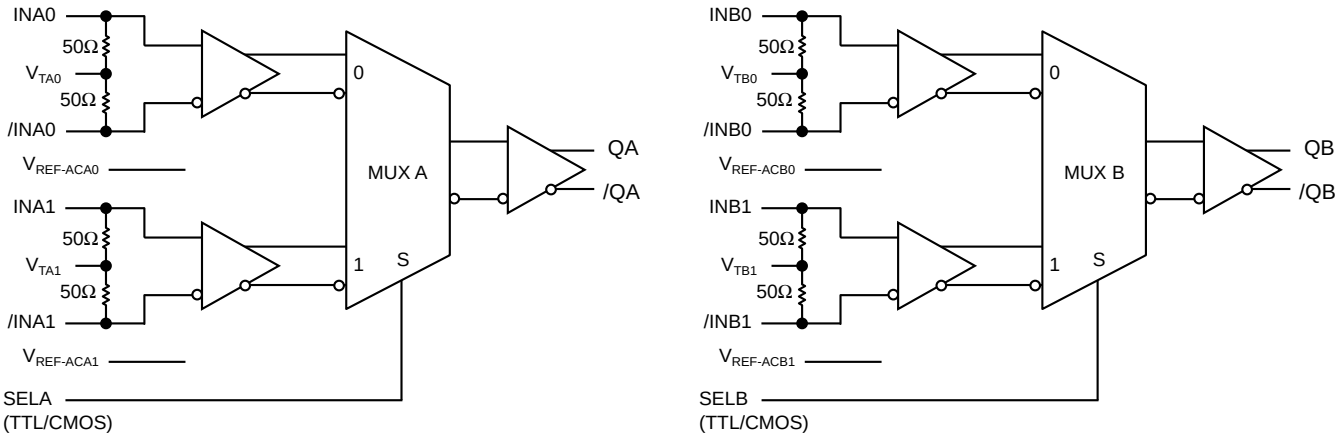
The SY58025U operates from a 2.5V or 3.3V supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY58025U is part of Micrel's Precision Edge® product family.

All support documentation can be found on Micrel's web site at www.micrel.com.

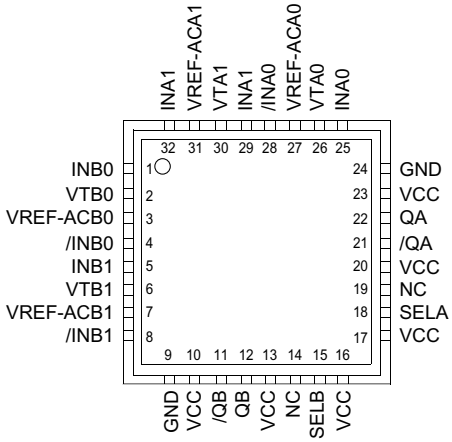
APPLICATIONS

- **Data communication systems**
- **All SONET OC3-OC-768 applications**
- **All Fibre Channel applications**
- **All GigE applications**

FUNCTIONAL BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58025UMI	MLF-32	Industrial	SY58025U	Sn-Pb
SY58025UMITR[2]	MLF-32	Industrial	SY58025U	Sn-Pb
SY58025UMG[3]	MLF-32	Industrial	SY58025Uwith Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58025UMGTR[2, 3]	MLF-32	Industrial	SY58025U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
25, 28, 29, 32, 1, 4, 5, 8	INA0, /INA0, INA1, /INA1, INB0, /INB0, INB1, /INB1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to V_{CC} and the complementary input to GND through a 1kΩ resistor. The VT pin is to be left open in this configuration. Please refer to the "Input Interface Applications" section for more details.
26, 30, 2, 6	VTA0 , VTA1, VTB0, VTB1	Input Termination Center-Tap: Each side of the differential input pair, terminates to a VT pin. Each V_T pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
18, 15	SELA, SELB	Bank A, Bank B Input Channel Select (TTL/CMOS): These TTL/CMOS-compatible inputs select the inputs to the multiplexers. These inputs are internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is V_{CC}/2.
27, 31, 3, 7	VREF-ACA0, VREF-ACA1, VREF-ACB0, VREF-ACB1	Reference Output Voltage: These outputs bias to V_{CC} –1.2V. Connect to the VT pin when AC-coupling the data inputs. Bypass with 0.01µF low ESR capacitor to V_{CC}. Maximum current source or sink is 0.5mA. See "Input Interface Applications" section.
10, 13, 16, 17, 20, 23	VCC	Positive Power Supply: Bypass with 0.1µF‖0.01µF low ESR capacitors.
22, 21, 12, 11	QA, /QA, QB, /QB	Differential CML Outputs: MUX A and MUX B selected CML outputs. See "Output Interface Applications" section for termination. Refer to the "Truth Table" for logic operation.
9, 24	GND, Exposed pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
14, 19	NC	Not connected.

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC}–1.0V to V_{CC}+0.5V
Termination Current(3)
  Source or sink current on V_T pin ..... ±100mA
Input Current
  Source or sink current on IN, /IN pin ..... ±50mA
Current (V_{REF-AC})
  Source or sink current on V_{REF-AC}(3) ..... ±1.5mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings(2)

Power Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance(4)
  MLF® (θ_{JA})
    Still-Air ..... 35°C/W
  MLF® (ψ_{JB})
    Junction-to-board ..... 20°C/W

DC ELECTRICAL CHARACTERISTICS(5)

T_A = –40°C to +85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}.(6)		115	140	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		40	50	60	Ω
V_{IH}	Input High Voltage (IN, /IN)		V_{CC} –1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH} –0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN - /IN|	See Figure 1b.	0.2		3.4	V
$V_{T\ IN}$	In to V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if the ratings in “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential (GND) on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50Ω pull-ups. See Figure 1b.

CML OUTPUT DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 100Ω across each output pair, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage Q, /Q		V_{CC}–0.020		V_{CC}	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	325	400		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	650	800		mV
R_{OUT}	Output Source Impedance Q, /Q		40	50	60	Ω

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to 85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		50	µA
I_{IL}	Input LOW Current		–300			µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 100Ω across each output pair, or equivalent, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	10.7			Gbps
		V_{OUT} ≥ 200mV Clock		6		GHz
t_{pd}	Propagation Delay IN-to-Q SEL-to-Q		 140 100		 290 400	 ps ps
t_{SKEW}	Input-to-Input Skew (Within-Bank)	**Note 9**		3	15	ps
	Bank-to-Bank Skew	**Note 10**		5	20	ps
	Part-to-Part Skew	**Note 11**			100	ps
t_{JITTER}	Data Random Jitter (RJ)	**Note 12**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 13**			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	**Note 14**			1	ps_{RMS}
	Total Jitter (TJ)	**Note 15**			10	ps_{PP}
	Crosstalk-Induced Jitter Channel-to-Channel	 **Note 16,** Within-bank.			 0.7	 ps_{RMS}
t_r, t_f	Output Rise/Fall Time 20% to 80%	At full swing.	20	50	70	ps

Notes:

8. High-speed AC parameters are guaranteed by design and characterization. V_{IN} swing ≥ 100mV unless otherwise noted.
9. Input-to-input skew is the difference in time between two inputs to the output within a bank.
10. Bank-to-bank skew is the difference in time from input to the output between bank.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
12. Random jitter is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps/3.2Gbps.
13. Deterministic jitter is measured at 2.5Gbps/3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern
14. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.
15. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
16. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

TRUTH TABLES

INA0	/INA0	INA1	/INA1	SELA	QA	/QA
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

INB0	/INB0	INB1	/INB1	SELB	QB	/QB
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

SINGLE-ENDED AND DIFFERENTIAL SWINGS

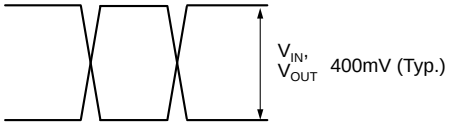


Figure 1a. Single-Ended Voltage Swing

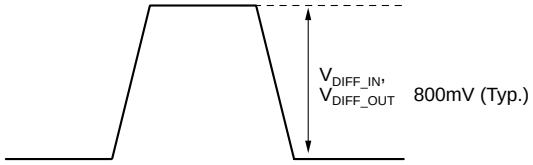
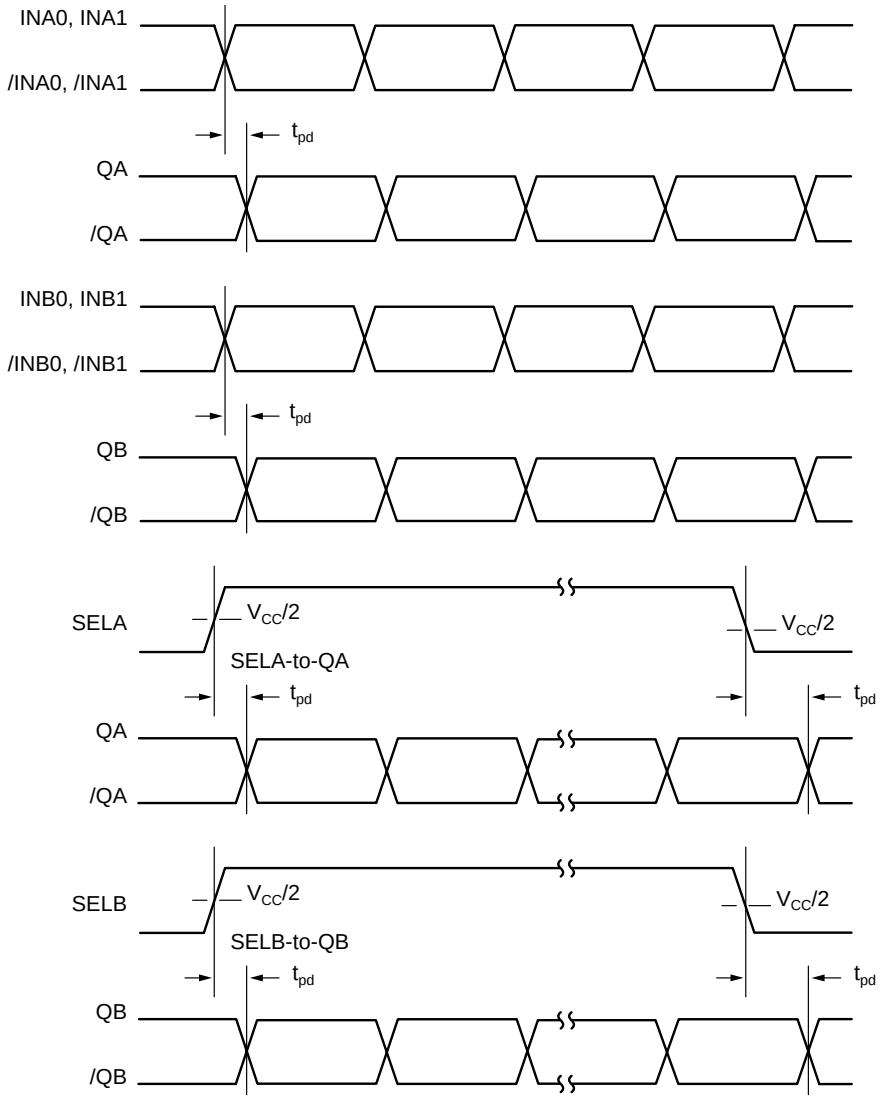


Figure 1b. Differential Voltage Swing

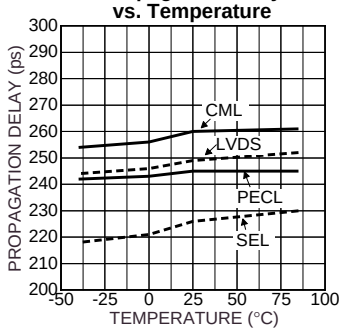
TIMING DIAGRAMS



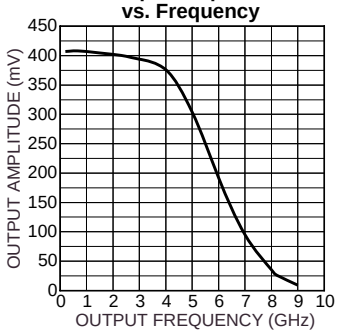
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, T_A = 25°C, R_L = 100Ω across each pair, DC-coupled, unless otherwise stated.

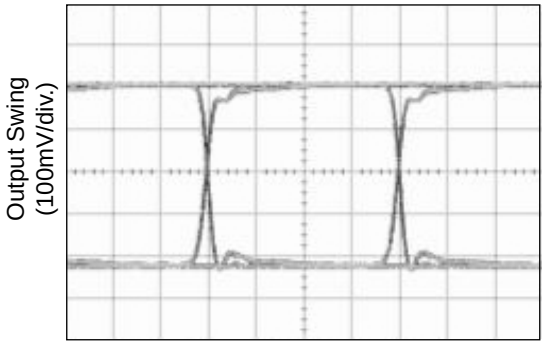
Propagation Delay vs. Temperature



Output Amplitude vs. Frequency

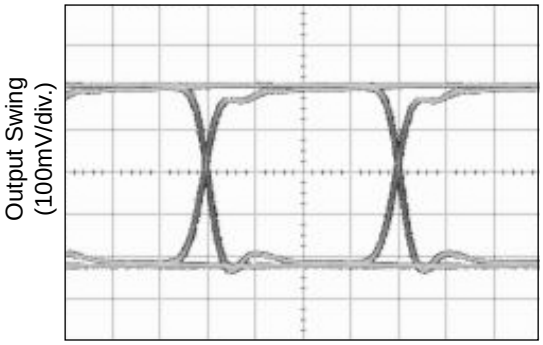


125Mbps Output (2^{23}—1 PRBS)



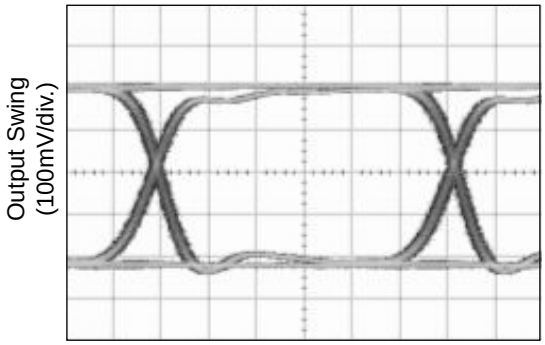
TIME (200ps/div.)

2.5Gbps Output (2^{23}—1 PRBS)



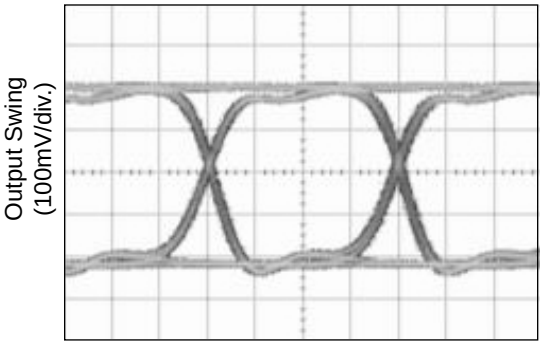
TIME (100ps/div.)

3.2Gbps Output (2^{23}—1 PRBS)



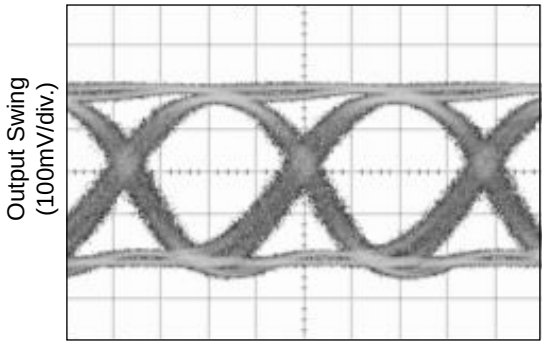
TIME (50ps/div.)

5Gbps Output (2^{23}—1 PRBS)



TIME (50ps/div.)

10.7Gbps Output (2^{23}—1 PRBS)

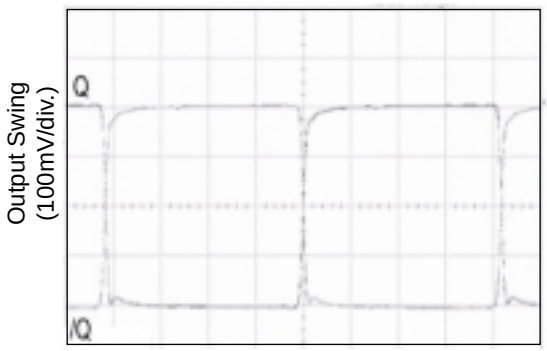


TIME (25ps/div.)

TYPICAL OPERATING CHARACTERISTICS

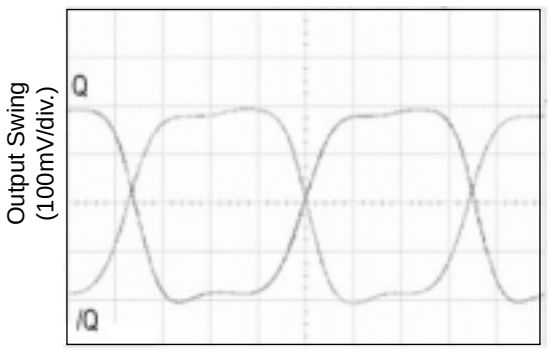
V_{CC} = 3.3V, T_A = 25°C, R_L = 100Ω across each pair, DC-coupled, unless otherwise stated.

200MHz Clock



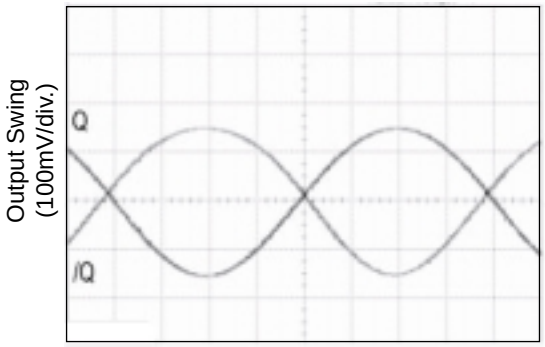
TIME (600ps/div.)

2GHz Clock



TIME (70ps/div.)

5GHz Clock



TIME (25ps/div.)

INPUT AND OUTPUT STAGE INTERNAL TERMINATION

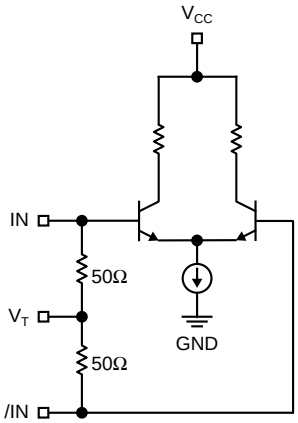


Figure 2a. Simplified Differential Input Stage

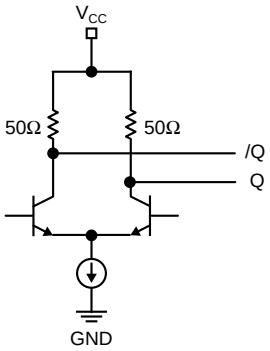
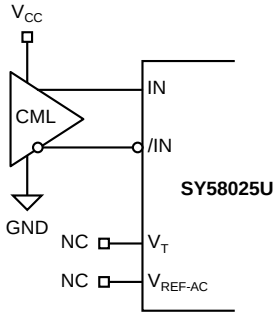


Figure 2b. Simplified CML Output Stage

INPUT INTERFACE APPLICATIONS



Option: may connect V_T to V_{CC}.

Figure 3a. DC-Coupled CML Interface

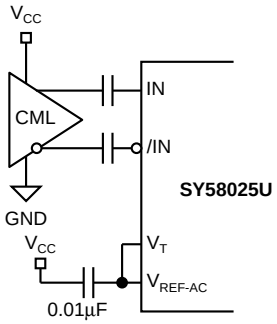


Figure 3b. AC-Coupled CML Interface

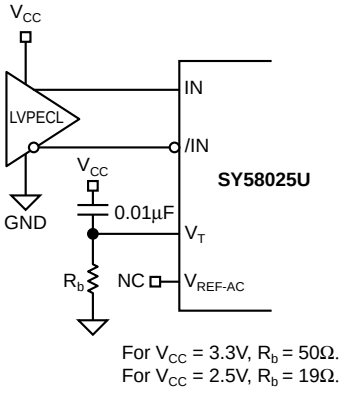


Figure 3c. DC-Coupled PECL Interface

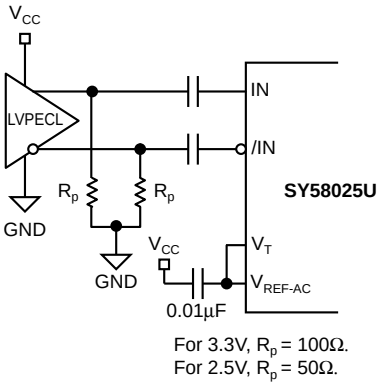


Figure 3d. AC-Coupled PECL Interface

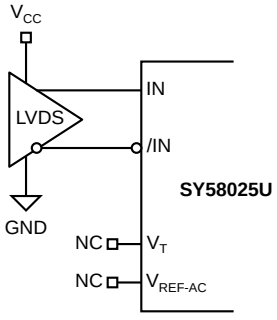


Figure 3e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

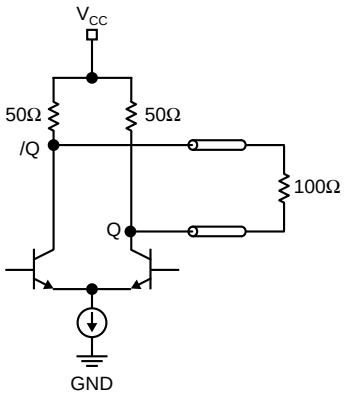


Figure 4. CML DC-Coupled Termination

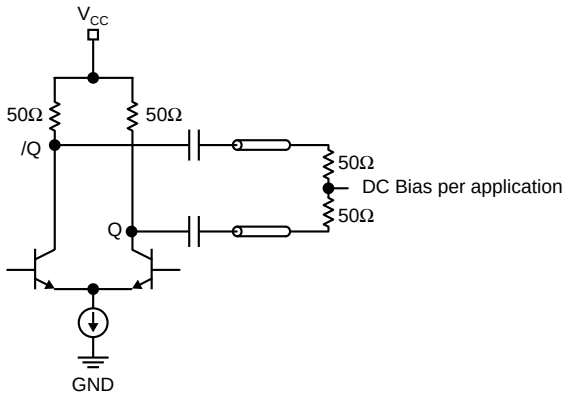
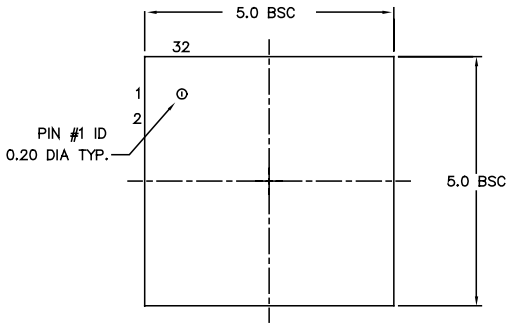


Figure 5. CML AC-Coupled Termination

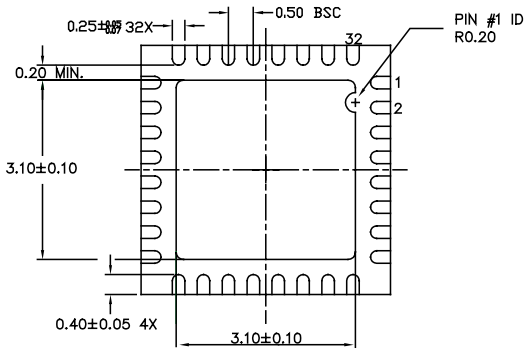
RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/ Receiver with Internal Termination	http://www.micrel.com/product-info/products/sy58016l.shtml
SY58017U	10.7Gbps Differential CML 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58017u.shtml
SY58018U	5Gbps LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58018u.shtml
SY58019U	10.7Gbps 400mV LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58019u.shtml
SY58026U	5Gbps Dual 2:1 LVPECL MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58026u.shtml
SY58027U	10.7Gbps Dual 2:1 400mV LVPECL MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58027u.shtml
SY58051U	10.7Gbps AnyGate® with Internal Input and Output Termination	http://www.micrel.com/product-info/products/sy58051u.shtml
SY58052U	10Gbps Clock/Data Retimer with 50Ω InpuT Termination	http://www.micrel.com/product-info/products/sy58052u.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

32-PIN *Micro*LeadFrame® (MLF-32)

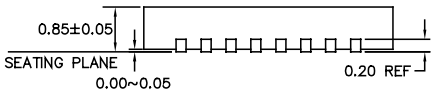


TOP VIEW

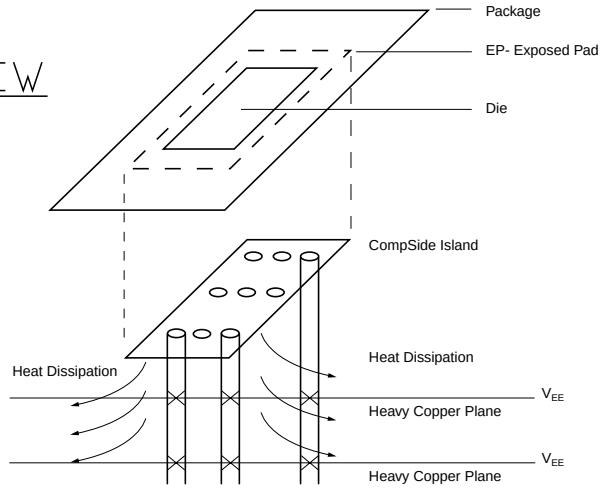


BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW



PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com