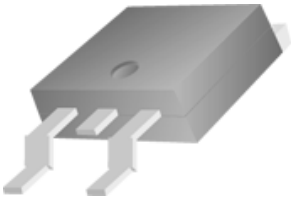
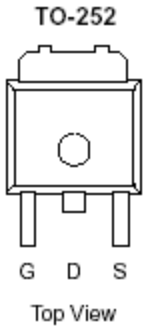
P-Channel 60-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ mΩ	I_D (A)
-60	135 @ V_{GS} = -10V	16
	190 @ V_{GS} = -4.5V	14

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology





ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current[a]	T_A=25°C	I_D	16	A
Pulsed Drain Current[b]		I_{DM}	±40	
Continuous Source Current (Diode Conduction)[a]		I_S	-15	A
Power Dissipation[a]	T_A=25°C	P_D	50	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient[a]	$R_{\theta JA}$	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	°C/W

Notes

a. Surface Mounted on 1” x 1” FR4 Board.

b. Pulse width limited by maximum junction temperature

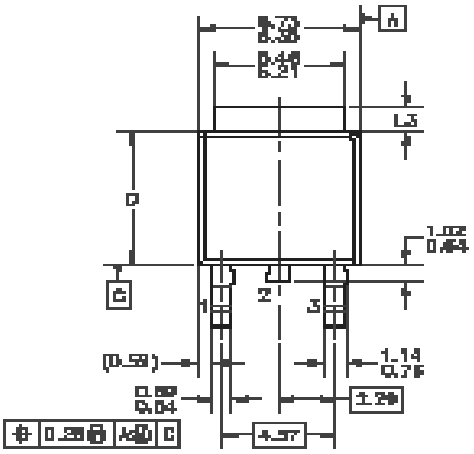
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 uA	-1			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V			-1	uA
		V_{DS} = -48 V, V_{GS} = 0 V, T_J = 55°C			-10	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	-20			A
Drain-Source On-Resistance[A]	$r_{DS(on)}$	V_{GS} = -10 V, I_D = -28 A			135	mΩ
		V_{GS} = -4.5 V, I_D = -14 A			190	
Forward Tranconductance[A]	g_{fs}	V_{DS} = -15 V, I_D = -28 A		8		S
Diode Forward Voltage	V_{SD}	I_S = -2.5 A, V_{GS} = 0 V			-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -30 V, V_{GS} = -4.5 V, I_D = -28 A		18		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			2		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -30 V, R_L = 30Ω , ID= -1 A, VGEN= -10 V, RG= 6Ω		8		nS
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall-Time	t_f			12		

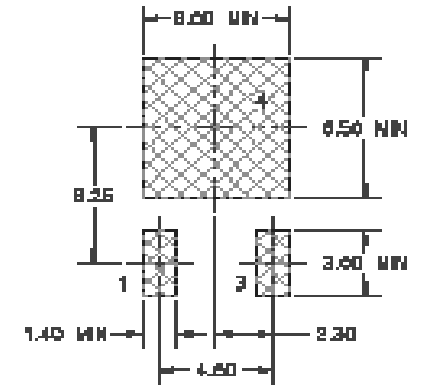
Notes

a. Pulse test: PW <= 300us duty cycle <= 2%.

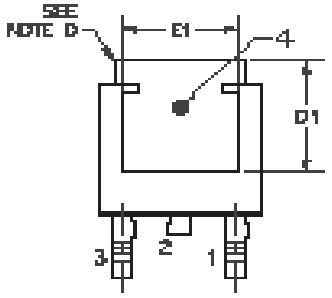
b. Guaranteed by design, not subject to production testing.

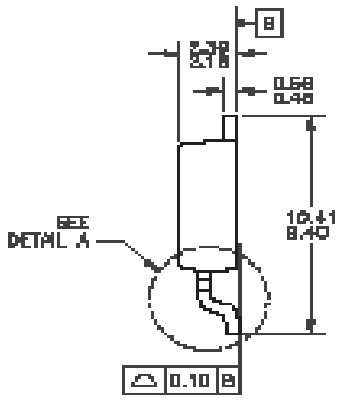
Package Information

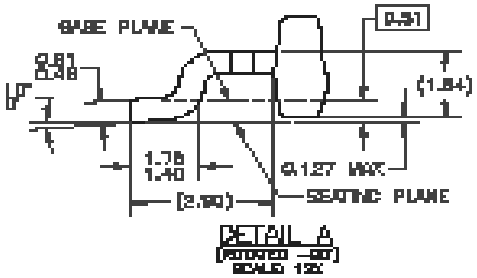




LAND PATTERN RECOMMENDATION







NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) THIS PACKAGE CONFORMS TO JEDEC, TO-263, ISSUE C, VARIATION AA, Ø REF, DATED NOV. 1989.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION A1	OPTION A2
L3	0.08~1.27	1.02~2.69
D	8.07~8.83	8.44~9.09
E1	4.82 MIN	3.81 MIN
D1	3.81 MIN	4.57 MIN