MC74HCT273A

Octal D Flip-Flop with Common Clock and Reset with LSTTL-Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT273A may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

The HCT273A is identical in pinout to the LS273.

This device consists of eight D flip–flops with common Clock and Reset inputs. Each flip–flop is loaded with a low–to–high transition of the Clock input. Reset is asynchronous and active low.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 284 FETs or 71 Equivalent Gates

LOGIC DIAGRAM

PIN 20 = V_{CC}
PIN 10 = GND
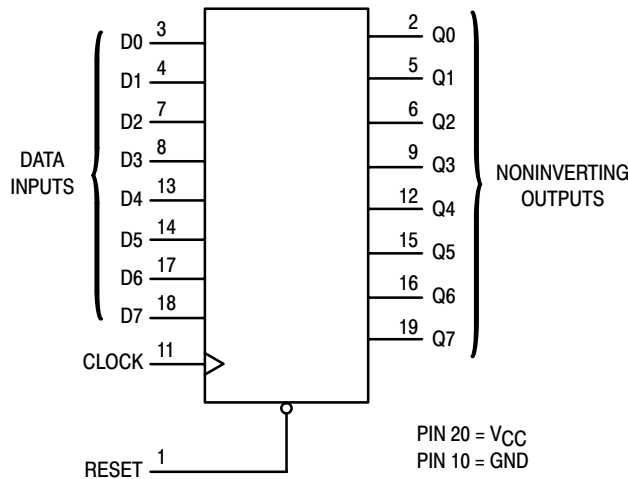
FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	⌐	H	H
H	⌐	L	L
H	L	X	No Change
H	⌐	X	No Change

X = Don't Care
Z = High Impedance

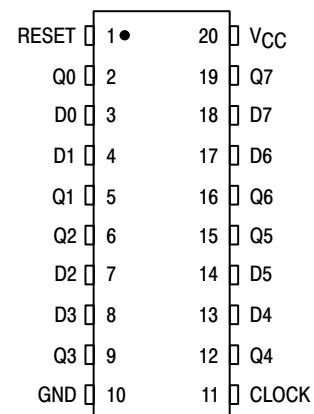**ON Semiconductor**

MARKING DIAGRAMS
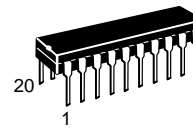
PDIP–20
N SUFFIX
CASE 738

MC74HCT273AN
AWLYYWW
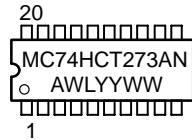
SOIC WIDE–20
DW SUFFIX
CASE 751D

HCT273A
AWLYYWW

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN ASSIGNMENT

RESET	1	20	V_{CC}
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	CLOCK

ORDERING INFORMATION

Device	Package	Shipping
MC74HCT273AN	PDIP–20	1440 / Box
MC74HCT273ADW	SOIC–WIDE	38 / Rail
MC74HCT273ADWR2	SOIC–WIDE	1000 / Reel

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MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		− 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)		− 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)		− 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin		± 20	mA
I_{out}	DC Output Current, per Pin		± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 50	mA
P_D	Power Dissipation in Still Air	Plastic DIP†	750	mW
		SOIC Package†	500	
T_{stg}	Storage Temperature		− 65 to + 150	C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or Plastic DIP)		260	C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND $\leq$ (V_{in} or V_{out}) $\leq$ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/ C from 65 to 125 C
SOIC Package: – 7 mW/ C from 65 to 125 C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	− 55	+ 125	C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				− 55 to 25 C	$\leq$ 85 C	$\leq$ 125 C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $|I_{out}|$ $\leq$ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $|I_{out}|$ $\leq$ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $|I_{out}|$ $\leq$ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $|I_{out}|$ $\leq$ 4.0 mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $|I_{out}|$ $\leq$ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $|I_{out}|$ $\leq$ 4.0 mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA		$\geq$ −55 C	25 C to 125 C		
			5.5	2.9	2.4		mA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit			Unit
			− 55 to 25 C	≤ 85 C	≤ 125 C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	1, 4	30	24	20	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q	1, 4	25	28	35	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q	2, 4	25	28	35	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	1, 5	18	20	22	ns

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	30	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

TIMING REQUIREMENTS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			− 55 to 25 C		≤ 85 C		≤ 125 C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	3	10		12		15		ns
t_h	Minimum Hold Time, Clock to Data	3	3.0		3.0		3.0		ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock	2	5.0		5.0		5.0		ns
t_w	Minimum Pulse Width, Clock	1	12		15		18		ns
t_w	Minimum Pulse Width, Set or Reset	2	12		15		18		ns
t_r, t_f	Maximum Input Rise and Fall Times	1		500		500		500	ns

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SWITCHING WAVEFORMS

Figure 1.

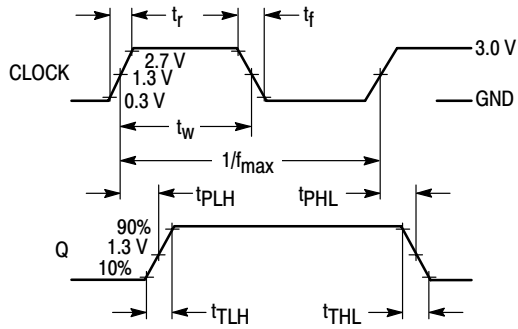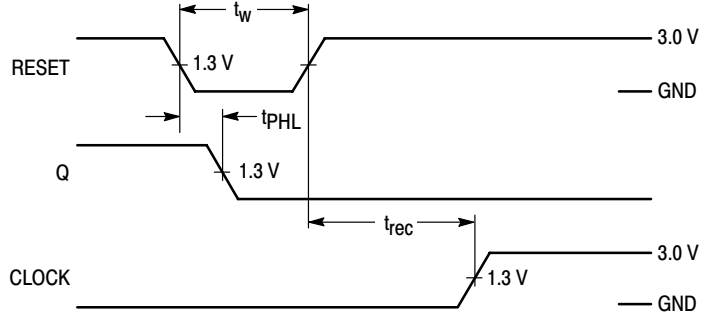**Figure 2.**

Figure 3.
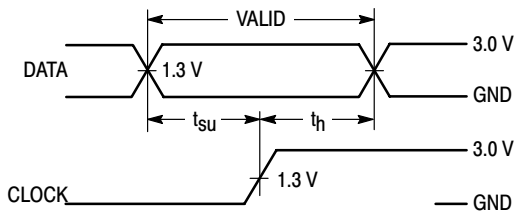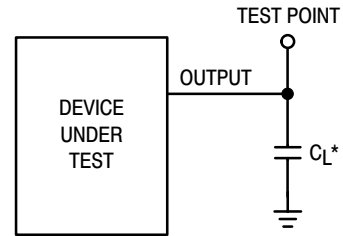

*Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM