

# MC10E1652

## 5V ECL Dual ECL Output Comparator with Latch

The MC10E1652 is fabricated using ON Semiconductor's advanced MOSAIC III™ process and is output compatible with 10H logic devices. In addition, the device is available in both a 16-pin DIP and a 20-pin surface mount package. However, the MC10E1652 provides user programmable hysteresis.

The latch enable ( $\overline{LEN}_a$  and  $\overline{LEN}_b$ ) input pins operate from standard ECL 10H logic levels. When the latch enable is at a logic high level, the MC10E1652 acts as a comparator; hence, Q will be at a logic high level if  $V_1 > V_2$  ( $V_1$  is more positive than  $V_2$ ).  $\overline{Q}$  is the complement of Q. When the latch enable input goes to a low logic level, the outputs are latched in their present state, providing the latch enable setup and hold time constraints are met. The level of input hysteresis is controlled by applying a bias voltage to the HYS pin.

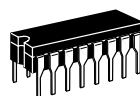
The 100 Series contains temperature compensation.

- Typical 3.0 dB Bandwidth > 1.0 GHz
- Typical V to Q Propagation Delay of 775 ps
- Typical Output Rise/Fall of 350 ps
- Common Mode Range -2.0 V to +3.0 V
- Individual Latch Enables
- Differential Outputs
- Operating Mode:  $V_{CC} = 5.0$  V,  $V_{EE} = -5.2$  V
- Programmable Input Hysteresis
- No Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",  
Oxygen Index 28 to 34
- Transistor Count = 85 devices



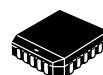
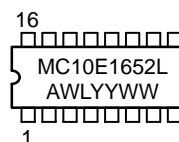
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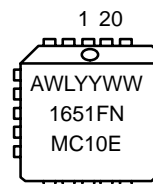


CDIP-16  
L SUFFIX  
CASE 620

### MARKING DIAGRAMS



PLCC-20  
FN SUFFIX  
CASE 775

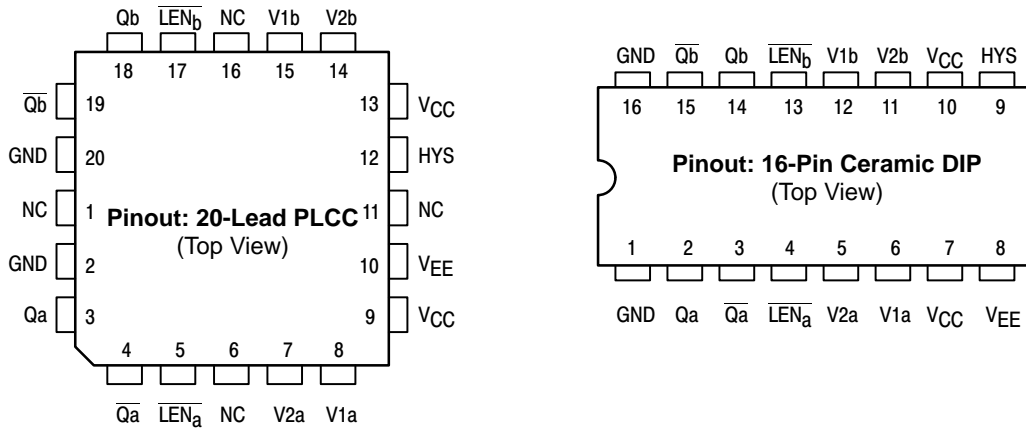


A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC10E1652L	CDIP-16	25 Units/Rail
MC10E1652FN	PLCC-20	46 Units/Rail
MC10E1652FNR2	PLCC-20	500 Units/Reel

# MC10E1652



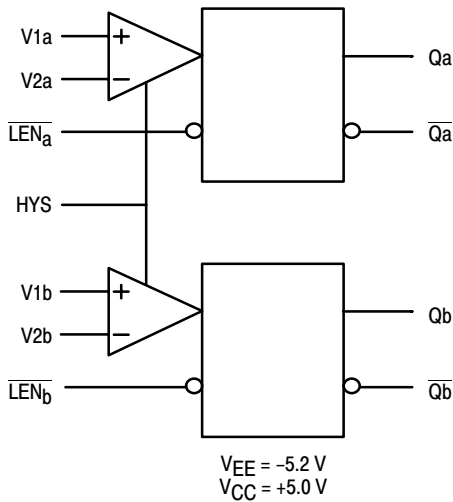
\* All VCC and VCCO pins are NOT tied together on the die.

Warning: All VCC, GND, and VEE pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Logic Diagrams and Pinout Assignments

## PIN DESCRIPTION

PIN	FUNCTION
Qa, $\overline{Qa}$	ECL Differential Outputs (a)
Qb, $\overline{Qb}$	ECL Differential Outputs (b)
$\overline{LENa}$ , $\overline{LENb}$	ECL Latch Enable
V1a, V1b	ECL Input Comparator 1
V2a, V2b	ECL Input Comparator 2
HYS	ECL Hysteresis Control
VCC	Positive Supply
VEE	Negative Supply
NC	No Connect
GND	Ground



## FUNCTION TABLE

$\overline{LEN}$	V1, V2	Function
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

Figure 2. Logic Diagram

# MC10E1652

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
VSUP	Total Supply Voltage	$ V_{EE}  +  V_{CC} $		12.0	V
VPP	Differential Input Voltage	$ V_1 - V_2 $		3.7	V
V <sub>I</sub>	PECL Mode Input Voltage	$V_{EE} = 0\text{ V}$	$V_I \leq V_{CC}$	12	V
	NECL Mode Input Voltage	$V_{CC} = 0\text{ V}$	$V_I \geq V_{EE}$	-12	V
I <sub>out</sub>	Output Current	Continuous Surge		50	mA
				100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM	28 PLCC	63.5	°C/W
		500 LFPM	28 PLCC	43.5	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V <sub>EE</sub>	PECL Operating Range			4.2 to 5.7	V
	NECL Operating Range			-5.7 to -4.2	V
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## DC CHARACTERISTICS $V_{CC} = +5.0\text{ V} \pm 5\%$ ; $V_{EE} = -5.2\text{ V} \pm 5\%$ (Note 2)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V <sub>OH</sub>	Output HIGH Voltage (Note 3)	-1020		-840	-980		-810	-920		-735	mV
V <sub>OL</sub>	Output Low Voltage (Note 3)	-1950		-1630	-1950		-1630	-1950		-1600	mV
V <sub>IL</sub>	Input LOW Voltage ( $\overline{LEN}$ )	-1.95		-1.48	-1.95		-1.48	-1.95		-1.45	mV
V <sub>IH</sub>	Input HIGH Voltage ( $\overline{LEN}$ )	-1.17		-0.84	-1.13		-0.81	-1.07		-0.735	mV
I <sub>I</sub>	Input Current (V <sub>1</sub> , V <sub>2</sub> )			65			65			65	μA
	Input HIGH Current ( $\overline{LEN}$ )			150			150			150	μA
I <sub>CC</sub>	Positive Supply Current			50			50			50	mA
	Negative Supply Current			-55			-55			-55	mA
V <sub>CMR</sub>	Common Mode Range (Note 4)	-2.0		3.0	-2.0		3.0	-2.0		3.0	V
Hys	Hysteresis (Note 5)		27			27			30		mV
V <sub>skew</sub>	Hysteresis Skew (Note 6)		-1.0			-1.0			0		mV
C <sub>in</sub>	Input Capacitance			3			3			3	pF
				DIP			2			PLCC	

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with  $V_{CC}$ .
- Outputs are terminated through a 50 ohm resistor to GND-2 volts.
- V<sub>CMR</sub> Min varies 1:1 with  $V_{EE}$ ; Max varies 1:1 with  $V_{CC}$ .
- The HYS pin programming characterization information is shown in Figure 2. The hysteresis values indicated in the data sheet are for the condition in which the voltage on the HYS pin is set to  $V_{EE}$ .
- Hysteresis skew ( $V_{skew}$ ) is provided to indicate the offset of the hysteresis window. For example, at 25°C the nominal hysteresis value is 27 mV and the  $V_{skew}$  value indicates that the hysteresis was skewed from the reference level by 1 mV in the negative direction. Hence the hysteresis window ranged from 14 mV below the reference level to 13 mV above the reference level. All hysteresis measurements were determined using a reference voltage of 0 mV. The hysteresis skew values apply over the programming range shown in Figure 2.

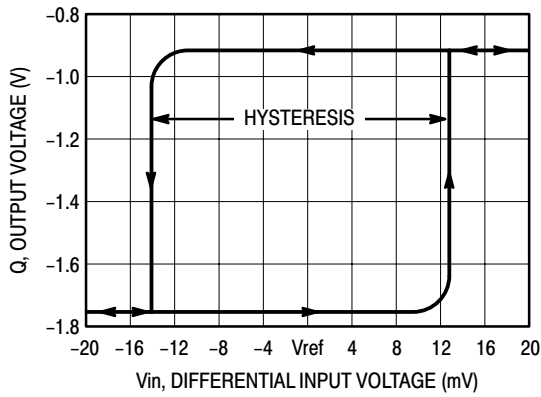


Figure 3. Typical Hysteresis Curve

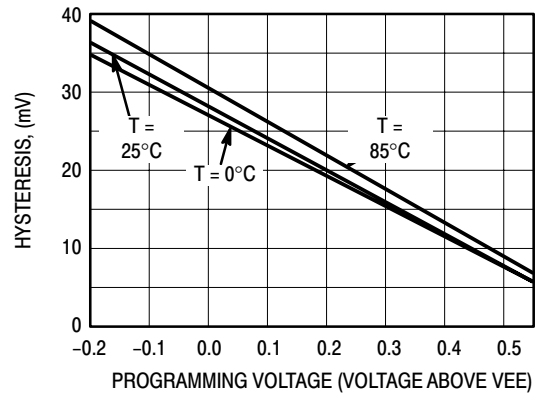


Figure 4. Hysteresis Programming Voltage

AC CHARACTERISTICS  $V_{CC} = +5.0\text{ V} \pm 5\%$ ;  $V_{EE} = -5.2\text{ V} \pm 5\%$  (Note 7)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency		TBD			> 1.0			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output (Note 8) V to Q LEN to Q	600 400	750 575	900 750	625 400	775 575	925 750	700 500	850 650	1050 850	ps
$t_s$	Setup Time V	450	300		450	300		550	350		ps
$t_h$	Enable Hold Time V	-50	-250		-50	-250		-100	-250		ps
$t_{pw}$	Minimum Pulse Width LEN	400			400			400			ps
$t_{skew}$	Within Device Skew (Note 9)		15			15			15		ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$T_{DE}$	Delay Dispersion (ECL Levels) (Notes 10, 11) (Notes 10, 12)					100 60					ps
$T_{DL}$	Delay Dispersion (TTL Levels) (Notes 13, 14) (Notes 12, 13)					350 100					ps
VPP	Differential Input Voltage  V1 - V2			3.7			3.7			3.7	V
$t_r$ $t_f$	Rise/Fall Times (20-80%)	225	325	475	225	325	475	250	375	500	ps

7. Input and output parameters vary 1:1 with  $V_{CC}$ .
8. The propagation delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and  $\bar{Q}$  output signals. For propagation delay measurements the threshold level ( $V_{THR}$ ) is centered about an 850 mV input logic swing with a slew rate of 0.75 V/NS. There is an insignificant change in the propagation delay over the input common mode range.
9.  $t_{skew}$  is the propagation delay skew between comparator A and comparator B for a particular part under identical input conditions.
10. Refer to Figure 4 and note that the input is at 850 mV ECL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and  $\bar{Q}$  output signals.
11. The slew rate is 0.25 V/NS for input rising edges.
12. The slew rate is 0.75 V/NS for input rising edges.
13. Refer to Figure 5 and note that the input is at 2.5 V TTL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and  $\bar{Q}$  output signals.
14. The slew rate is 0.3 V/NS for input rising edges.

## APPLICATIONS INFORMATION

The timing diagram (Figure 5.) is presented to illustrate the MC10E1652's compare and latch features. When the signal on the  $\overline{\text{LEN}}$  pin is at a logic high level, the device is operating in the "compare mode," and the signal on the input arrives at the output after a nominal propagation delay ( $t_{\text{PHL}}$ ,  $t_{\text{PLH}}$ ). The input signal must be asserted for a time,  $t_s$ , prior to the negative going transition on  $\overline{\text{LEN}}$  and held for a time,  $t_h$ , after the  $\overline{\text{LEN}}$  transition. After time  $t_h$ , the latch is operating in the "latch mode," thus transitions on the input do not appear at the output. The device continues to operate in the "latch mode" until the latch is asserted once again. Moreover, the  $\overline{\text{LEN}}$  pulse must meet the minimum pulse width ( $t_{\text{pw}}$ ) requirement to effect the correct input-output relationship. Note that the  $\overline{\text{LEN}}$  waveform in Figure 5. shows the  $\overline{\text{LEN}}$  signal swinging around a reference labeled  $\text{VBB}_{\text{INT}}$ ; this waveform emphasizes the requirement that  $\overline{\text{LEN}}$  follow typical ECL 10KH logic levels because

$\text{VBB}_{\text{INT}}$  is the internally generated reference level, hence is nominally at the ECL VBB level.

Finally,  $\text{V}_{\text{OD}}$  is the input voltage overdrive and represents the voltage level beyond the threshold level ( $\text{V}_{\text{THR}}$ ) to which the input is driven. As an example, if the threshold level is set on one of the comparator inputs as 80 mV and the input signal swing on the complementary input is from zero to 100 mV, the positive going overdrive would be 20 mV and the negative going overdrive would be 80 mV. The result of differing overdrive levels is that the devices have shorter propagation delays with greater overdrive because the threshold level is crossed sooner than the case of lower overdrive levels. Typically, semiconductor manufactures refer to the threshold voltage as the input offset voltage ( $\text{V}_{\text{OS}}$ ) since the threshold voltage is the sum of the externally supplied reference voltage and inherent device offset voltage.

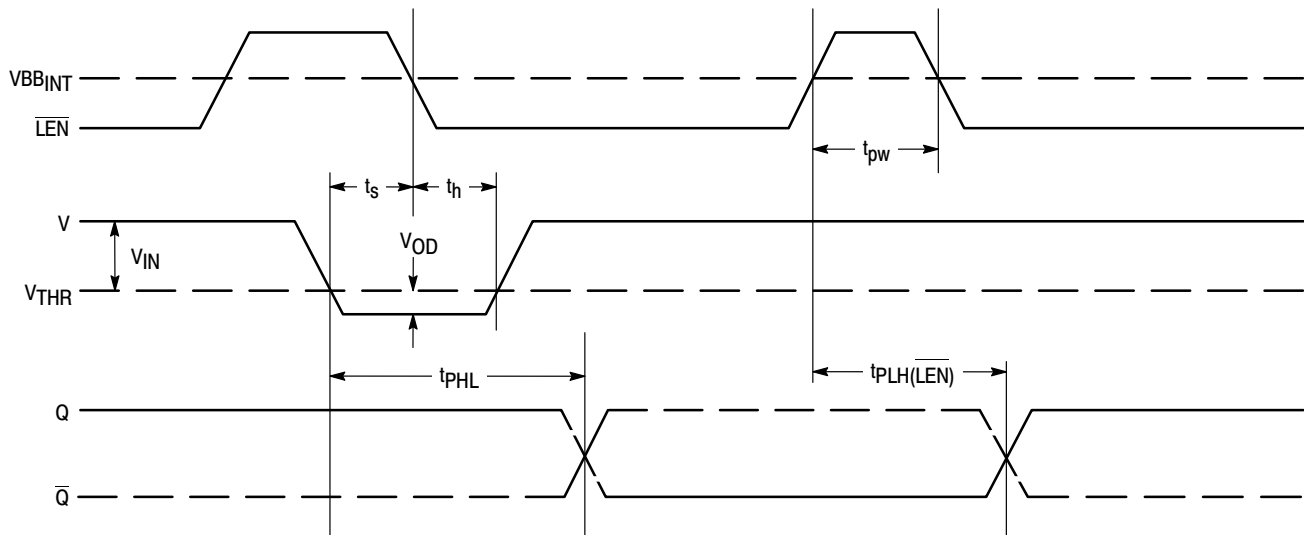


Figure 5. Input/Output Timing Diagram

DELAY DISPERSION

Under a constant set of input conditions comparators have a specified nominal propagation delay. However, since propagation delay is a function of input slew rate and input voltage overdrive the delay dispersion parameters,  $T_{DE}$  and  $T_{DT}$ , are provided to allow the user to adjust for these variables (where  $T_{DE}$  and  $T_{DT}$  apply to inputs with standard ECL and TTL levels, respectively).

Figure 6. and Figure 7. define a range of input conditions which incorporate varying input slew rates and input voltage overdrive. For input parameters that adhere to these constraints the propagation delay can be described as:

$$T_{NOM} \pm T_{DE} \text{ (or } T_{DT}\text{)}$$

where  $T_{NOM}$  is the nominal propagation delay.  $T_{NOM}$  accounts for nonuniformity introduced by temperature and voltage variability, whereas the delay dispersion parameter takes into consideration input slew rate and input voltage overdrive variability. Thus a modified propagation delay can be approximated to account for the effects of input conditions that differ from those under which the parts were tested. For example, an application may specify an ECL input with a slew rate of 0.25 V/NS, an overdrive of 17 mV and a temperature of 25°C, the delay dispersion parameter would be 100 ps. The modified propagation delay would be 775 ps  $\pm$  100 ps

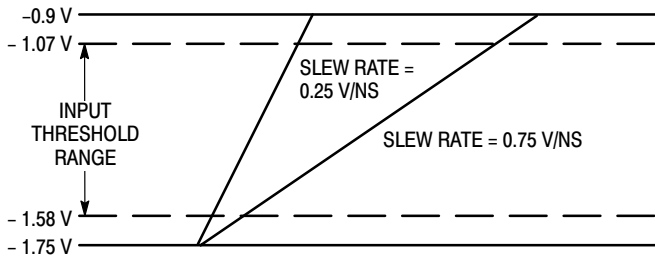


Figure 6. ECL Dispersion Test Input Conditions

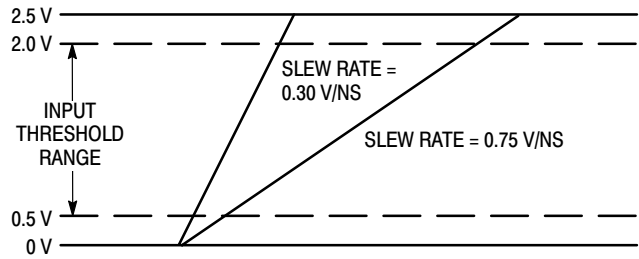
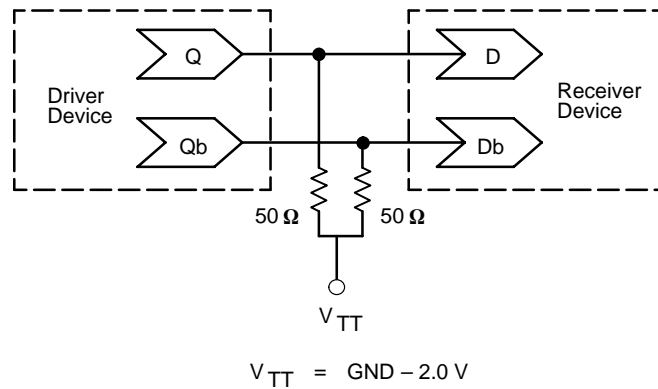


Figure 7. TTL Dispersion Test Input Conditions



**Figure 8. Typical Termination for Output Driver and Device Evaluation**  
 (See Application Note AND8020 – Termination of ECL Logic Devices.)

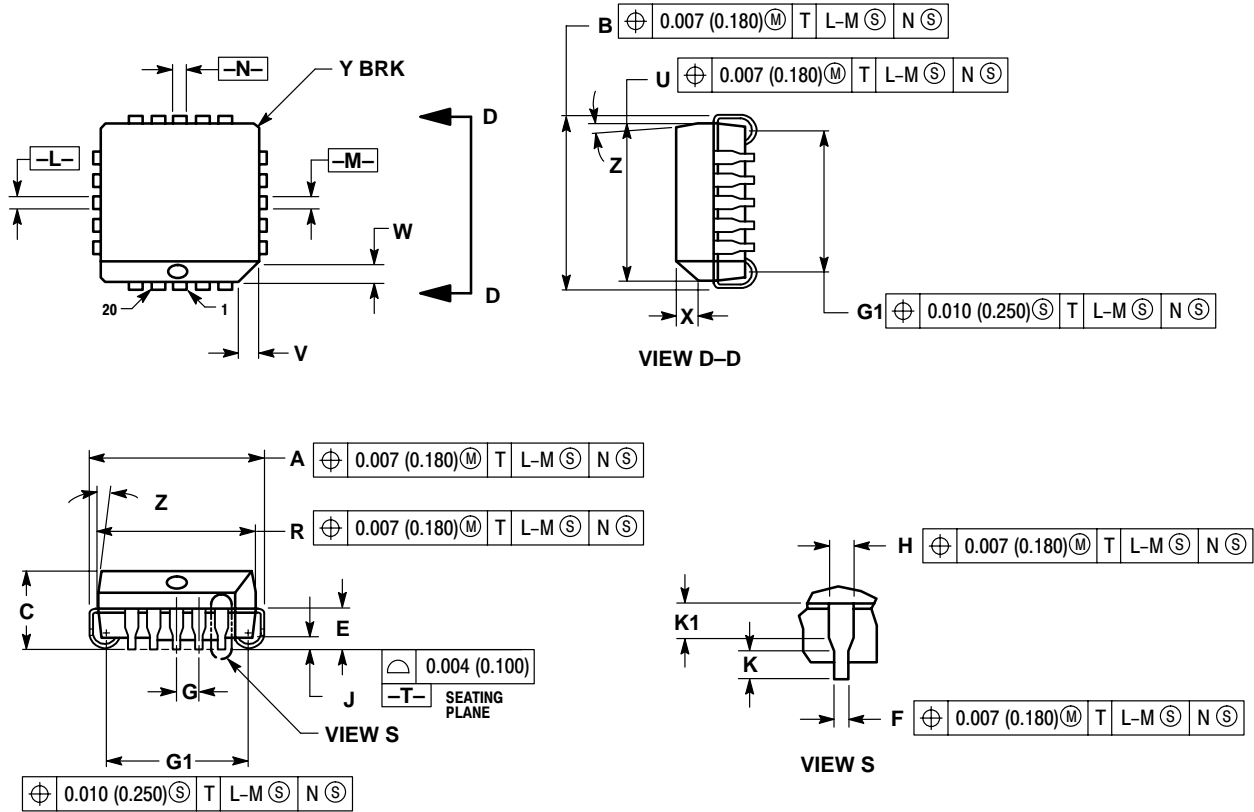
#### Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC10E1652

## PACKAGE DIMENSIONS

PLCC-20  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 775-02  
ISSUE D



### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

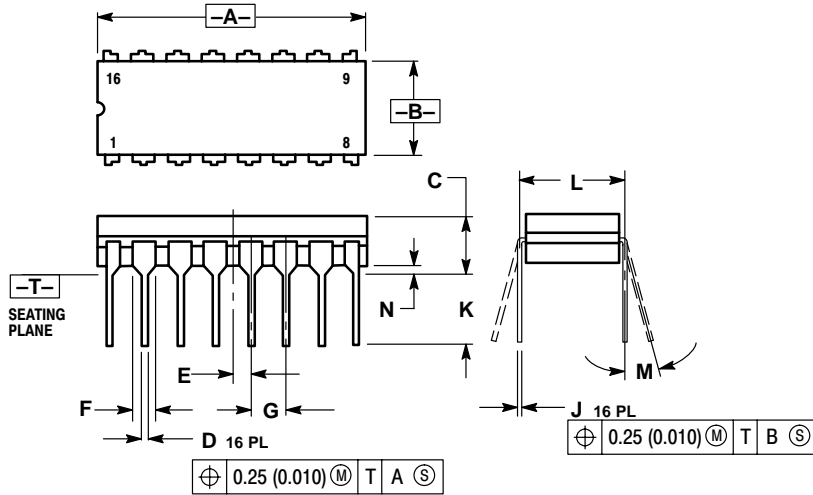
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---



# MC10E1652

## PACKAGE DIMENSIONS

CDIP-16  
L SUFFIX  
CERAMIC DIP PACKAGE  
CASE 620-10  
ISSUE T




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**Notes**

**Notes**

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