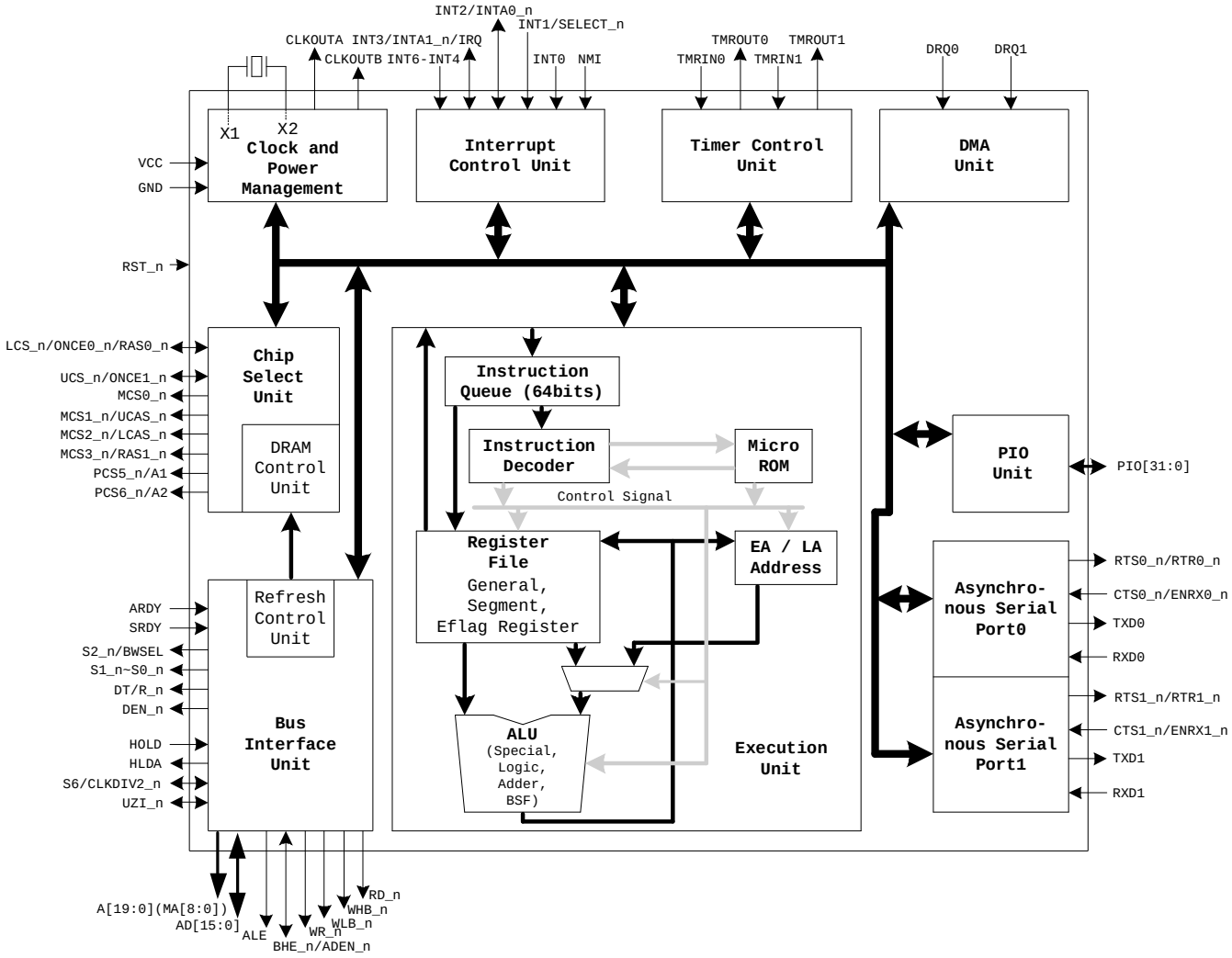
R8822I
Brief Sheet
16-BIT RISC MICROCONTROLLER

1. Features

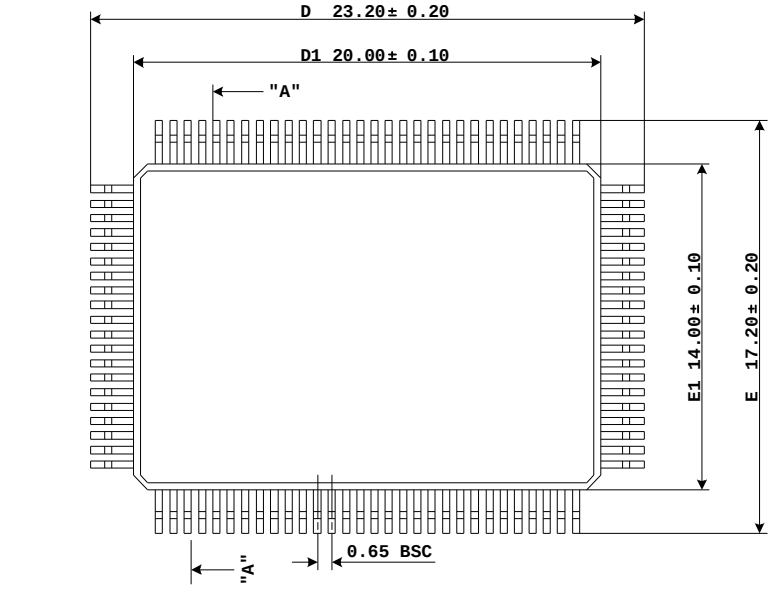
- CPU Core
  - RDC's proprietary RISC architecture
  - Five-stage pipeline
  - CPU Clock speed: 40MHz
  - Supports CPU ID
  - Supports 32 PIO pins
  - Static & synthesizable design
- Bus Interface
  - Multiplexed address and data bus
  - With 8-bit or 16-bit boot ROM bus size
  - Supports a non-multiplexed address bus A[19:0]
  - 8-bit or 16-bit external bus dynamic access
- ROM/RAM/DRAM Controller and Addressing Space
  - 1M-byte memory address space
  - 64K-byte I/O space
  - Supports 64Kx16, 128Kx16, 256Kx16 EDO or FP DRAM with auto-refresh control
- Two Independent DMA Channels
- Asynchronous Serial Channels
  - Supports two asynchronous serial channels with hardware handshaking signals
- Interrupt Controller
  - The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt
- Programmable Chip-select Logic
- Programmable wait-state generators
  - Programmable chip-select logic for memory or I/O bus cycle decoder
- Counters/Timers
  - Three independent 16-bit timers and one independent programmable watchdog timer
- Software Compatible with The 80C186 Microprocessor
- Operating Voltage Range
  - Core voltage: 5V ± 10%
  - I/O voltage: 5V ± 10%
- Ambient Temperature: -40 ~ +85°C
- Package Type
  - 100-pin PQFP
  - 100-pin LQFP
- A Green product

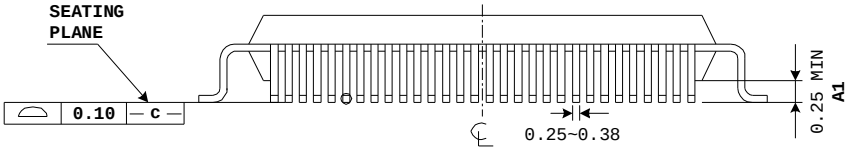
2. Block Diagram

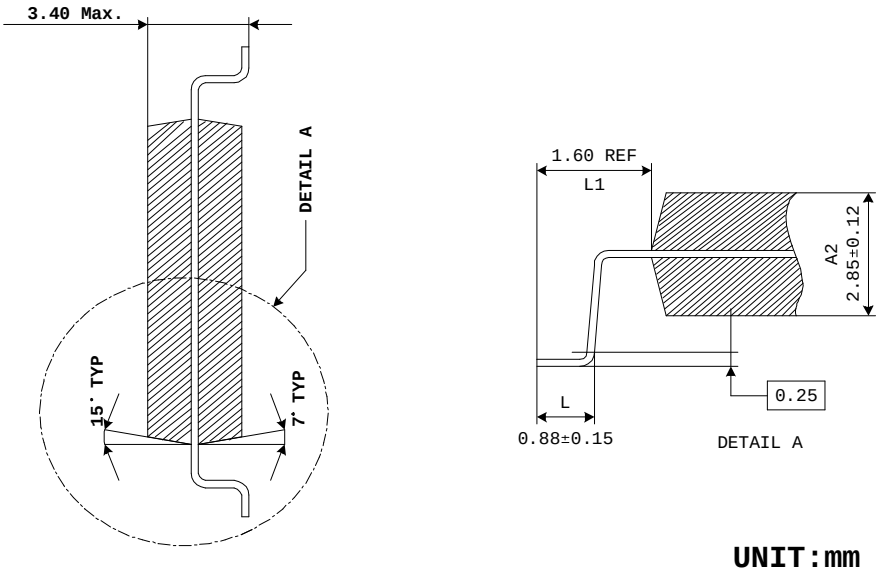


3. Package Information

PQFP 100 pins







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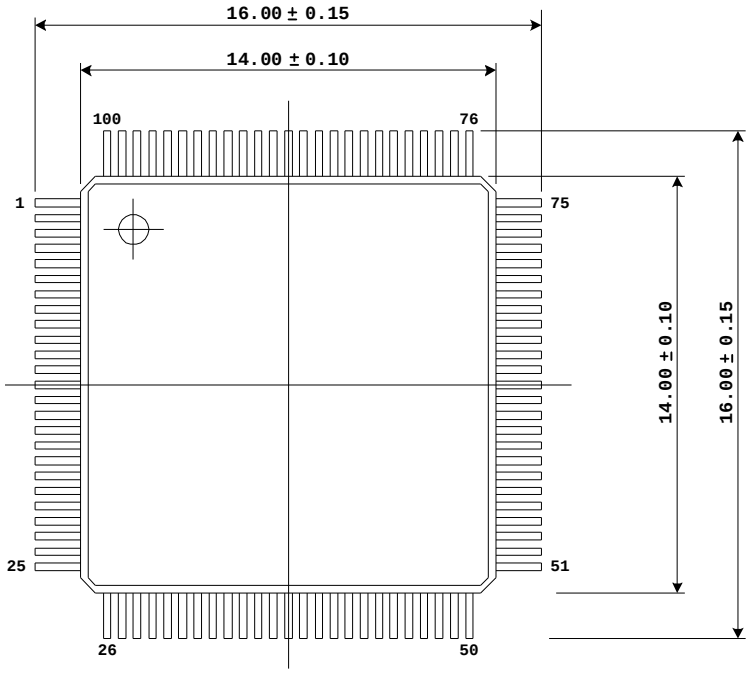
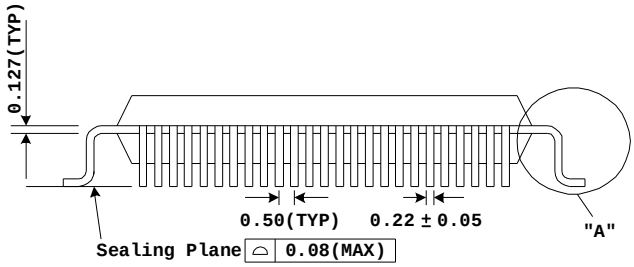
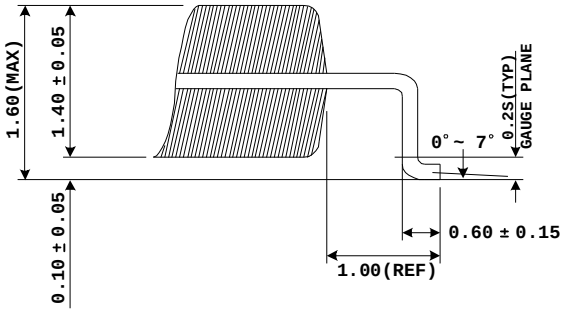
LQFP 100 pins







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