MC74VHC1GT66

Single Supply Analog Switch

The MC74VHC1GT66 is an advanced high speed CMOS bilateral analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The MC74VHC1GT66 is compatible in function to a single gate of the very High Speed CMOS MC74VHCT4066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage.

The ON/OFF Control input is compatible with TTL–type input thresholds allowing the device to be used as a logic–level translator from 3.0 V CMOS logic to 5.0 V CMOS logic or from 1.8 V CMOS logic to 3.0 V CMOS logic while operating at the high–voltage power supply. The input protection circuitry on this device allows overvoltage tolerance on the input, which provides protection when voltages of up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT66 to be used to interface 5 V circuits to 3 V circuits.

- High Speed: t_{PD} = 20 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage
- On/Off Control Input Has OVT
- Chip Complexity: FETs = 11; Equivalent Gates = 3

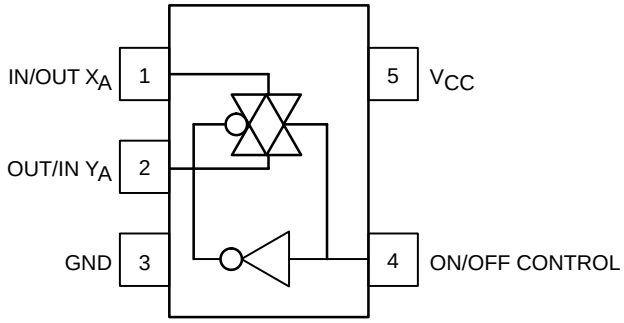


Figure 1. Pinout

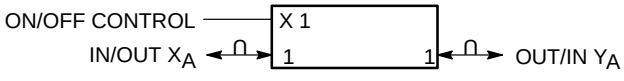


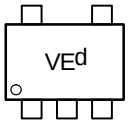
Figure 2. Logic Symbol

ON Semiconductor®

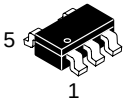
http://onsemi.com

MARKING DIAGRAMS

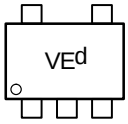
SC70–5/SC–88A/SOT–353
DF SUFFIX
CASE 419A



Pin 1



SOT23–5/TSOP–5/SC59–5
DT SUFFIX
CASE 483



Pin 1

d = Date Code

PIN ASSIGNMENT	
1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	V_{CC}

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		–0.5 to +7.0	V
V_{IN}	DC Input Voltage		–0.5 to +7.0	V
V_{IS}	Analog Output Voltage		–0.5 to 7.0	V
I_{IK}	Input Diode Current		–20	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+25	mA
T_{STG}	Storage Temperature Range		− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+ 150	°C
θ_{JA}	Thermal Resistance	SC70–5/SC–88A/SOT–353 (Note 1) SOT23–5/TSOP–5/SC59–5	350 230	°C/W
P_D	Power Dissipation in Still Air at 85°C	SC70–5/SC–88A/SOT–353 SOT23–5/TSOP–5/SC59–5	150 200	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{LATCH–UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm–by–1 inch, 2–ounce copper trace with no air flow.
2. Tested to EIA/JESD22–A114–A.
3. Tested to EIA/JESD22–A115–A.
4. Tested to JESD22–C101–A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	Digital Input Voltage		GND	5.5	V
V_{IS}	Analog Input Voltage		GND	V_{CC}	V
T_A	Operating Temperature Range		–55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

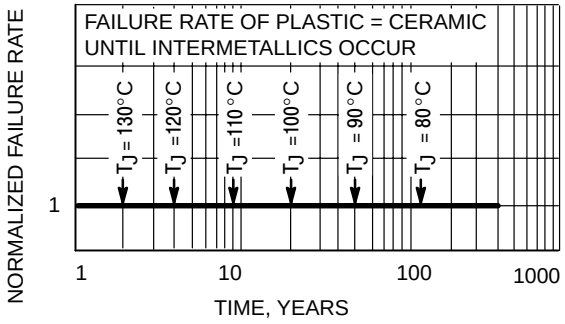


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55°C \le T_A \le 125°C$ Min	$-55°C \le T_A \le 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0		1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5		0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	V_{IN} = V_{CC} or GND	0 to 5.5		±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND V_{IO} = 0 V	5.5		1.0		20		40	μA
I_{CCT}	Quiescent Supply Current	ON/OFF Control at 3.4 V	5.5		1.35		1.5		1.65	mA
R_{ON}	Maximum "ON" Resistance	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\lvert I_{IS} \rvert \le$ 10 mA (Figure 4.)	3.0 4.5 5.5		60 45 40		70 50 45		100 60 55	Ω
I_{OFF}	Maximum Off–Channel Leakage Current	V_{IN} = V_{IL} V_{IS} = V_{CC} or GND Switch Off (Figure 5.)	5.5		0.1		0.5		1.0	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r/t_f = 3.0 ns

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	$-55°C \le T_A \le 125°C$ Min	$-55°C \le T_A \le 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input X to Y	Y_A = Open (Figure 14.)	2.0 3.0 4.5 5.5		1 0.6 0.6 0.6	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω (Figure 15.)	2.0 3.0 4.5 5.5		32 28 24 20	40 35 30 25		45 40 35 30		50 45 40 35	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω (Figure 15.)	2.0 3.0 4.5 5.5		32 28 24 20	40 35 30 25		45 40 35 30		50 45 40 35	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Control Input = GND Analog I/O Feedthrough	5.0		 4 4	 10 10		 10 10		 10 10	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	18	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 10.)	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3 dB R_L = 50 Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 180	MHz
ISO_{off}	Off–Channel Feedthrough Isolation (Figure 11.)	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	3.0 4.5 5.5	–80 –80 –80	dB
$NOISE_{feed}$	Feedthrough Noise Control to Switch (Figure 12.)	$V_{in} \leq$ 1 MHz Square Wave ($t_r = t_f$ = 2ns) R_L = 600 Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 130	mV_{PP}
THD	Total Harmonic Distortion (Figure 13.)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF THD = $THD_{Measured} - THD_{Source}$ V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 5.5	 0.30 0.15	%

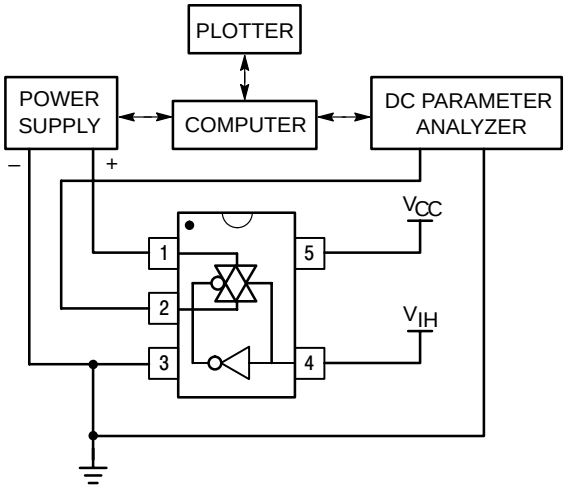


Figure 4. On Resistance Test Set–Up

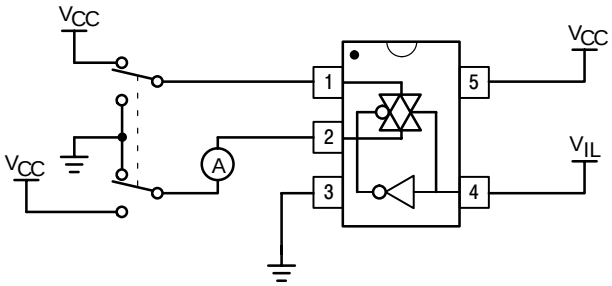


Figure 5. Maximum Off–Channel Leakage Current Test Set–Up

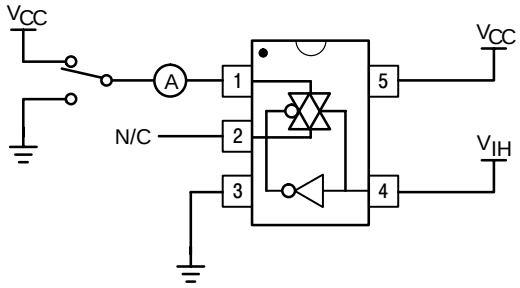


Figure 6. Maximum On–Channel Leakage Current Test Set–Up

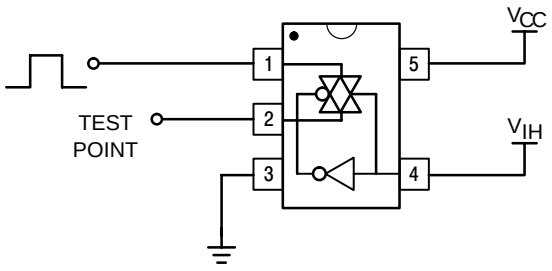


Figure 7. Propagation Delay Test Set–Up

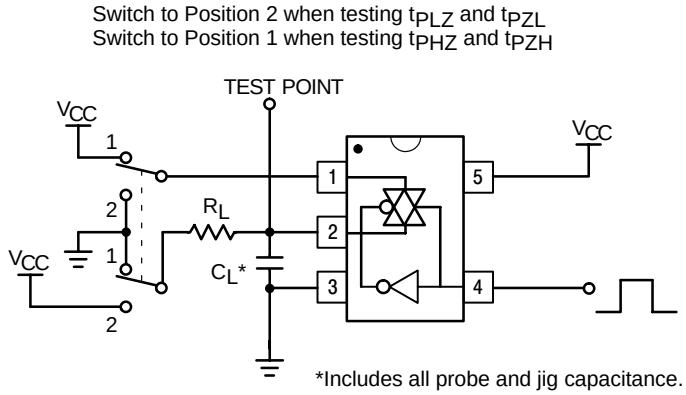


Figure 8. Propagation Delay Output Enable/Disable Test Set–Up

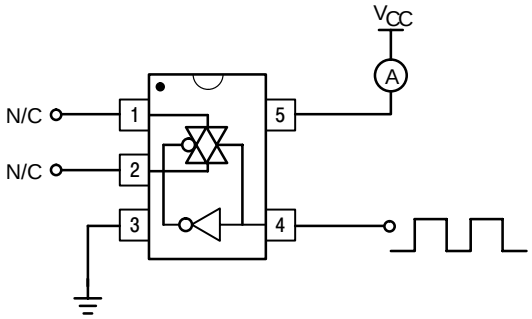


Figure 9. Power Dissipation Capacitance Test Set–Up

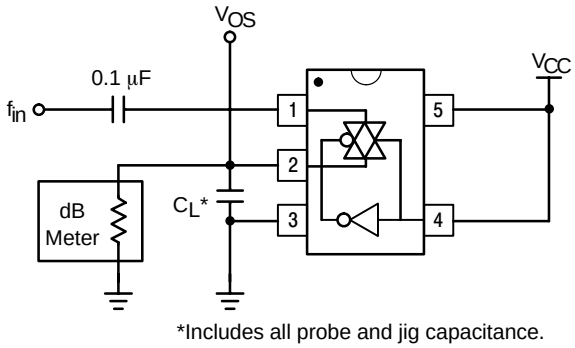


Figure 10. Maximum On–Channel Bandwidth Test Set–Up

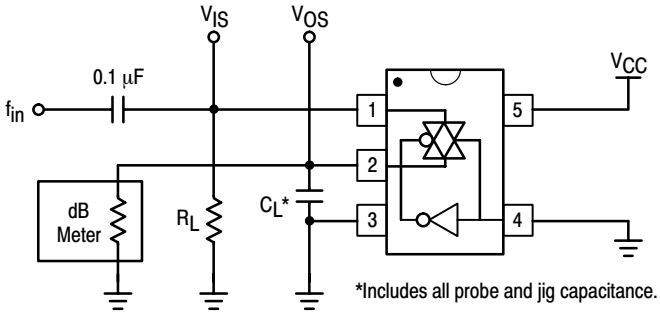


Figure 11. Off–Channel Feedthrough Isolation Test Set–Up

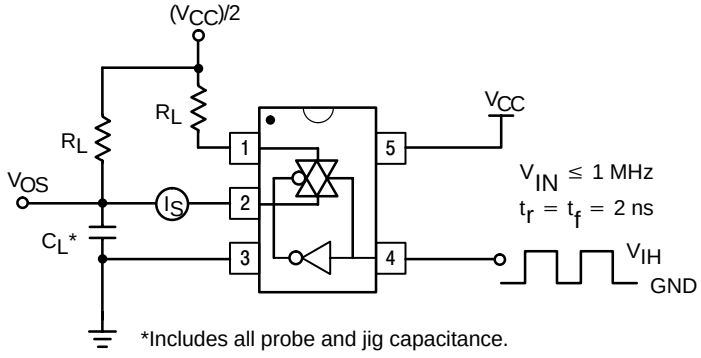


Figure 12. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

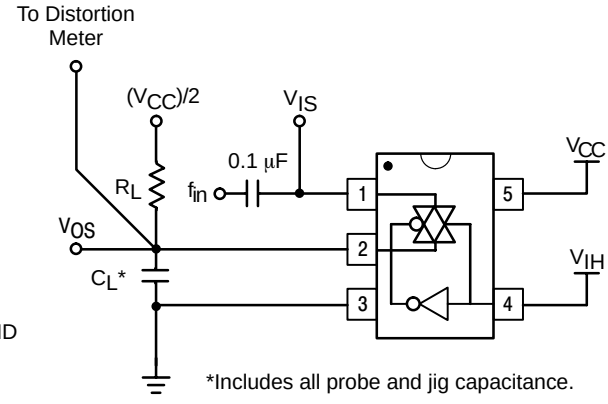


Figure 13. Total Harmonic Distortion Test Set–Up

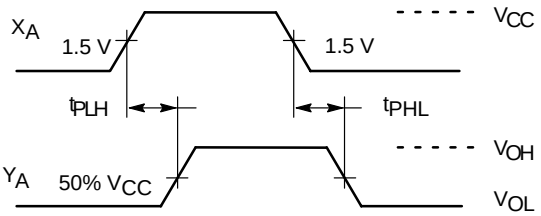


Figure 14. Propagation Delay, Analog In to Analog Out Waveforms

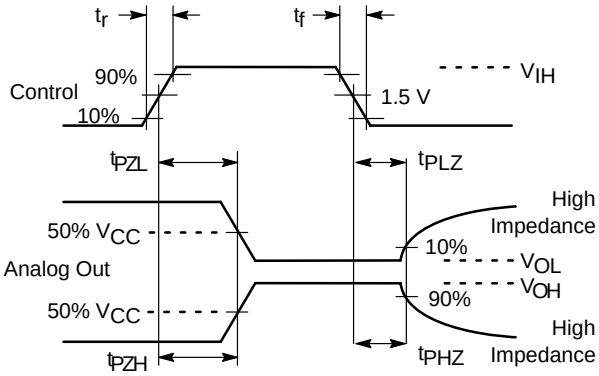


Figure 15. Propagation Delay, ON/OFF Control

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT66DFT1	MC	74	VHC1G	T66	DF	T1	SC70–5/SC–88A/ SOT–353	178 mm (7”) 3000 Unit
MC74VHC1GT66DFT2	MC	74	VHC1G	T66	DF	T2	SC70–5/SC–88A/ SOT–353	178 mm (7”) 3000 Unit
MC74VHC1GT66DTT1	MC	74	VHC1G	T66	DT	T1	SOT23–5/TSOP–5/ SC59–5	178 mm (7”) 3000 Unit

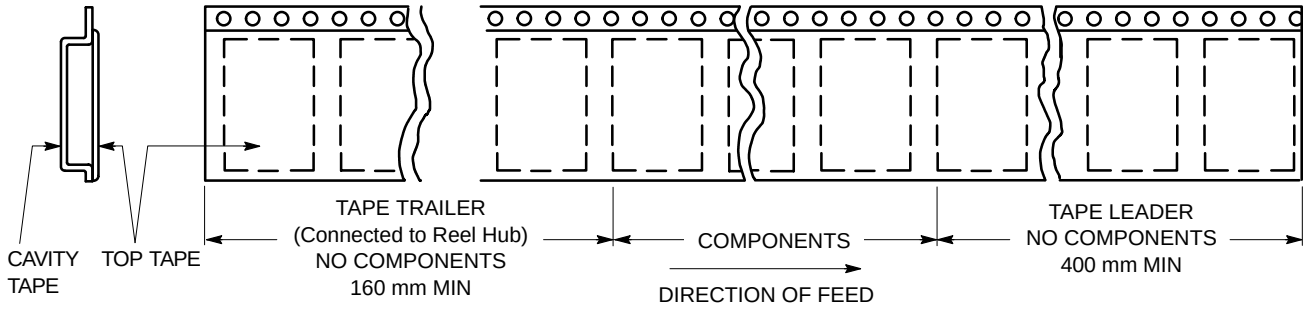


Figure 16. Tape Ends for Finished Goods

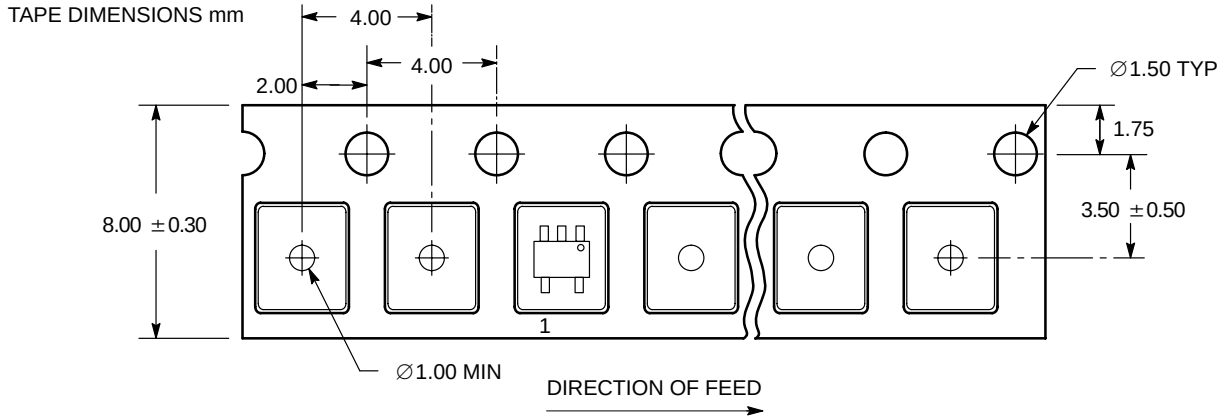


Figure 17. SC−70−5/SC−88A/SOT−353 DFT1 Reel Configuration/Orientation

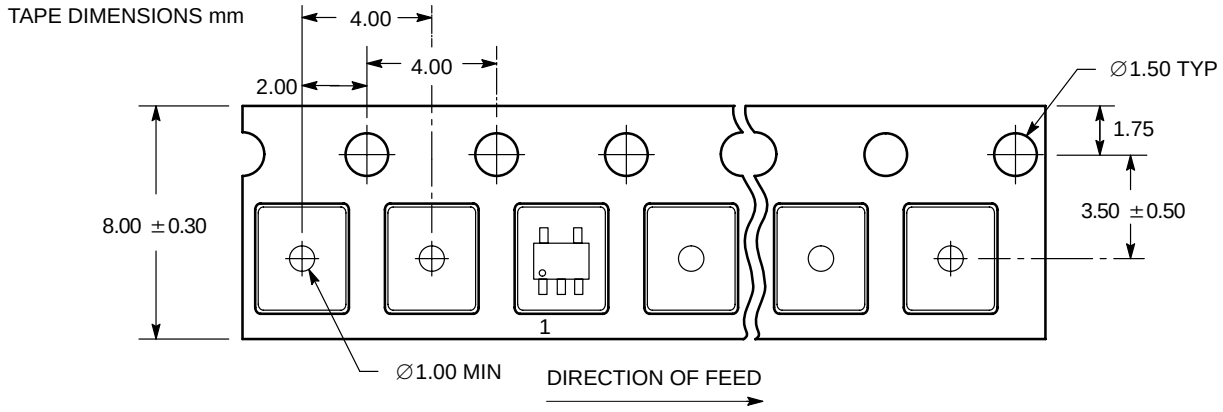


Figure 18. SC−70/SC−88A/SOT−353 DFT2 and SOT23−5/TSOP−5/SC59−5 DTT1 Reel Configuration/Orientation

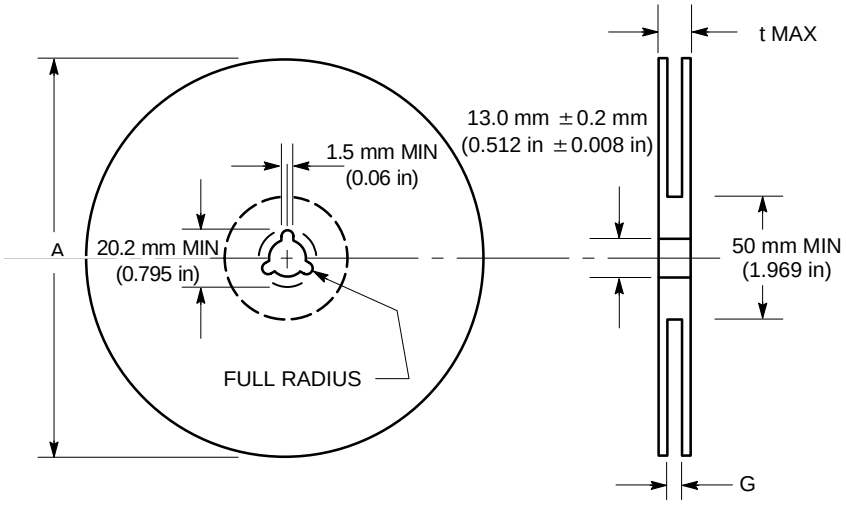


Figure 19. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, –0.0 (0.33 in + 0.059 in, –0.00)	14.4 mm (0.56 in)

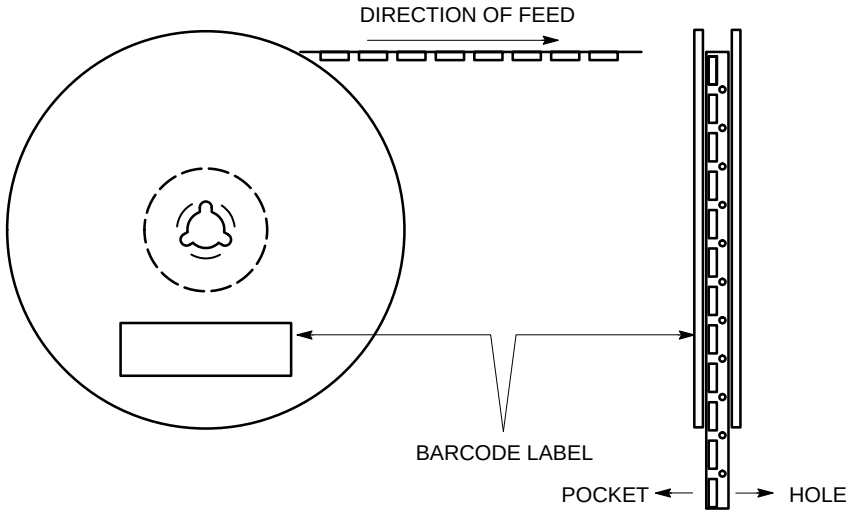
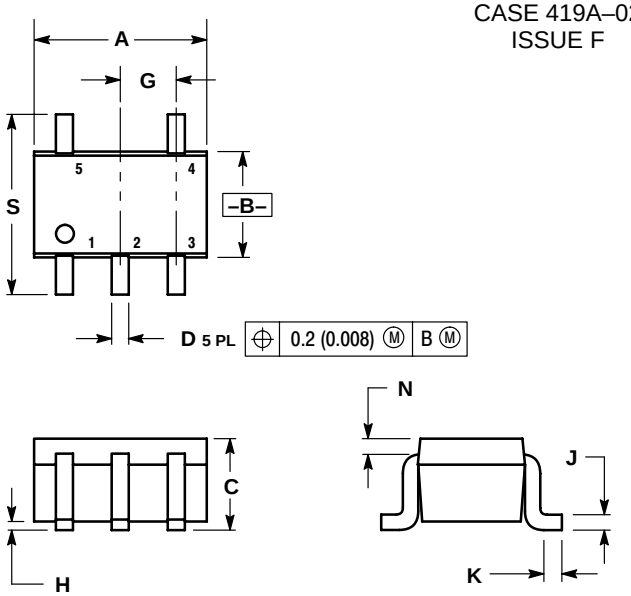


Figure 20. Reel Winding Direction

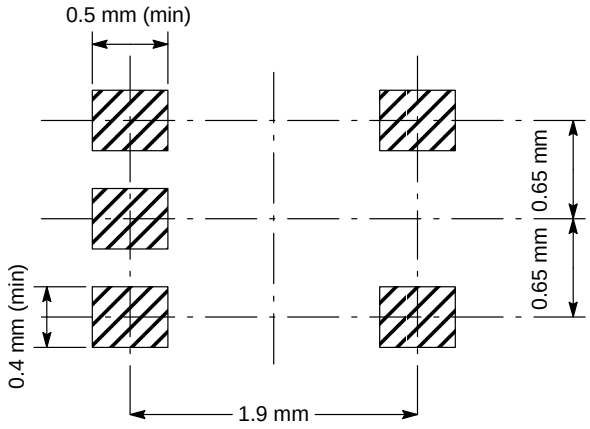
PACKAGE DIMENSIONS

SC70–5/SC–88A/SOT–353
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–02
ISSUE F



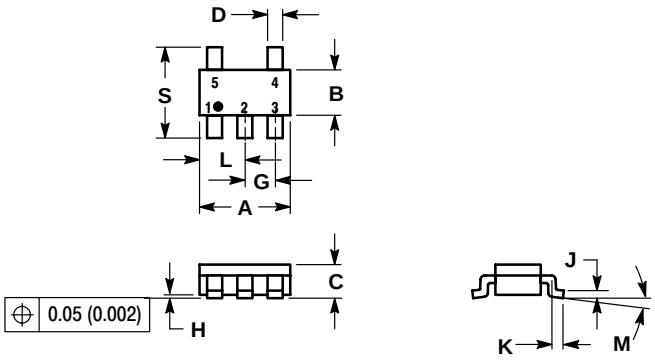
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A–01 OBSOLETE. NEW STANDARD 419A–02.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



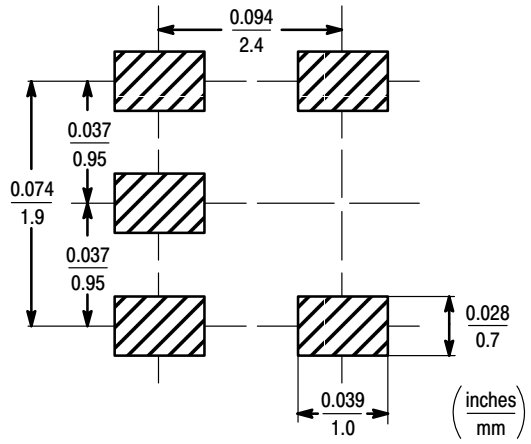
PACKAGE DIMENSIONS

SOT23–5/TSOP–5/SC59–5
DT SUFFIX
5–LEAD PACKAGE
CASE 483–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181



Notes

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.