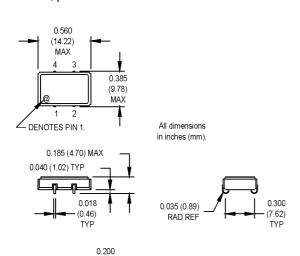
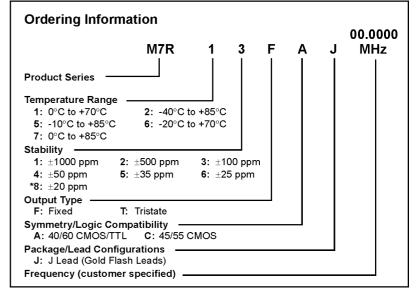
M7R Series 5.0 Volt HCMOS/TTL **Compatible Surface Mount Oscillators**





These are non-PLL based high frequency oscillators intended for applications that require low phase jitter. For frequencies 80.000 MHz and below, please see the M7S series.





^{*}Consult factory for availability.

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SUGGEST	ED SO	LDER PAD	LAYOUT
-	ł †	 0.200	(5.08)
-	-	0.05	0 (1.27)
			0.346
[A A		(8.80)
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		1	Į.

(5.08)TYP

Pin Connections

PIN	FUNCTION			
1	N/C or Tri-state			
2	Ground			
3	Output			
4	+Vdd			

	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition		
suc	Frequency Range	F	80.001		125	MHz			
	Frequency Stability	∆F/F	(See Order	ring Info	rmation)				
	Operating Temperature	Ta	(See Ordering Information)						
	Storage Temperature	Ts	-55		+125	°C			
atic	Input Voltage	Vdd	4.5	5.0	5.5	V			
al Specifications	Input Current	ldd			90	mA			
	Symmetry (Duty Cycle)		(See Ordering Information)				See Note 1		
	Load		10 TTL or 15 pF				See Note 2		
l Ë	Rise/Fall Time	Tr/Tf			5	ns	See Note 3		
Electrical	Logic "1" Level	Voh	90% Vdd			٧	HCMOS load		
			Vdd -0.5			V	TTL load		
	Logic "0" Level	Vol			10% Vdd	V	HCMOS load		
					0.5	V	TTL load		
	Cycle to Cycle Jitter			5	20	ps RMS	1 Sigma		
	Tri-state Function		Pin 1 logic	"1" or flo					
			Pin 1 logic	"0"; outp					
a	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C							
Environmental	Vibration	Per MIL-STD-202, Method 201 & 204							
	Reflow Solder Conditions	240°C for 10 s max.							
Vir	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10° atm.cc/s of helium)							
Ë	Solderability	Per EIAJ-STD-002							

- 1. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
 2. TTL load See load circuit diagram #1 on page 92. HCMOS load See load circuit diagram #2 on page 92.
- 3. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load.

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