Dual Programmable Buck Regulators with Integrated MOSFETs and Digital Control

FEATURES & APPLICATIONS

FEATURES

- **Dual Step-Down DC-DC Outputs**
  - **Integrated power MOSFET switches**
  - **1A-3A output current with built in current limit**
  - **Input voltage range: +4.5V to +16V**
  - **Output voltage +0.8V to +5.0V (+/-2.5% accuracy)**
  - **Automatic PFM mode for light load efficiency**
  - **Integrated frequency compensation**
- **Integrated Power Control and Programmability**
  - **I^2C Digital or Pin Control (Enable)**
  - **Static and Dynamic Programmable Output Voltage**
    - **128 levels of output voltage settings**
    - **"Coarse" nominal setpoint**
      - **0.8V-1.8V and 2.3/2.5/3.0/3.3/5.0V**
    - **"Fine" Margining**
      - **+1.14% to +7.95% (vs. coarse setting)**
  - **PWM frequency 500-1000kHz with 180° interleave**
  - **Output enable and power up/down sequence**
  - **Programmable output softstart/stop**
  - **Output UV monitoring with PGOOD/RESET output**

APPLICATIONS

- **Digital LCD/Plasma TV**
- **Digital Set-Top Box/PVR/DVR**
- **Datacom/Telecom Equipment**

INTRODUCTION

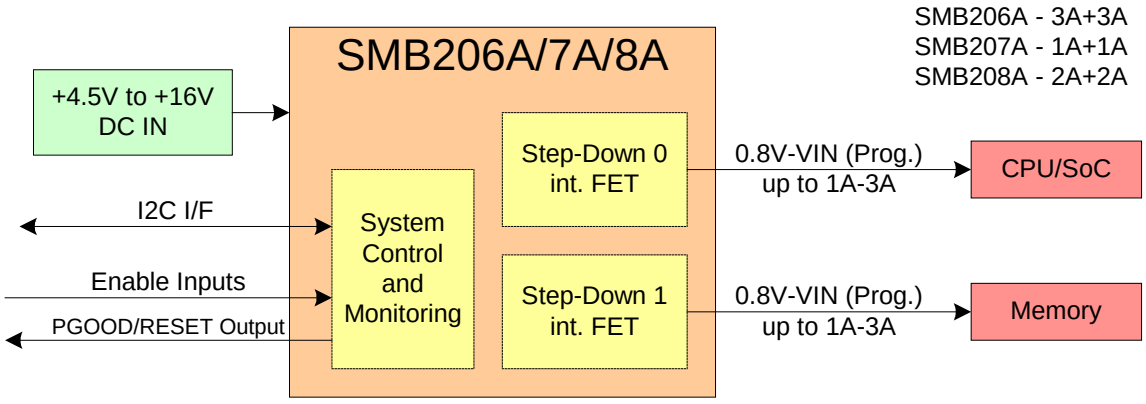
The SMB206A/7A/8A are highly integrated and flexible dual-output DC-DC regulators designed for use in a wide variety of applications. High integration reduces system cost and component count, while the built-in non-volatile digital programmability cuts development time by allowing system designers to custom tailor the device to suit almost any application.

The SMB206A/7A/8A includes integrated high-side MOSFET switches for up to 1A-3A continuous output current. Programmable output voltages as low as +0.8V support the latest VLSI digital cores. Minimum external components result in a very compact solution size for space constrained applications.

Sophisticated power control/monitoring functions required by many systems are built-in and accessible via digital I^2C interface. These include digitally programmable output voltage setpoint, power-up/down softstart and sequencing, independent enable/disable, output UV monitoring with PowerGood/Reset output. Additionally, fine resolution voltage margining is provided to allow for sophisticated system optimization.

The integration of features and built-in flexibility of the SMB206A/7A/8A allow the system designer to create a "platform solution" that can be easily modified without hardware changes. The SMB206A/7A/8A are well suited to applications with an input range of +4.5V to +16V. The operating temperature range is -40°C to +85°C and the available packages are 3mm X 3mm 20-pad QFN or 6.5mm X 6.4mm TSSOP-24.

Figure 1 - SIMPLIFIED APPLICATION



GENERAL DESCRIPTION

DIGITAL INTERFACE/NON-VOLATILE PROGRAMMING

The built-in serial digital I^2C/SMBus compatible port and built-in non-volatile programming bring several benefits to power supply design with the SMB206A/7A/8A. Many external components are eliminated that would otherwise be used to set configuration and parametric values. Additionally, the digital interface allows for quick and easy development and debug without hardware changes. Finally, after the non-volatile power-up configuration, the serial port can be used to re-program the SMB206A/7A/8A by host software after the system is running. For quick programming development and debug use Summit's prebuilt evaluation kit including a PC-based graphical user interface (GUI).

DUAL PWM DC-DC REGULATORS

The SMB206A/7A/8A contains two integrated PWM DC-DC step-down (buck) regulator(s) with identical features and functions. The input voltage range is +4.5V to +16V to support a wide variety of system applications. The outputs support a full 1A-3A continuous output current with a built-in cycle-by-cycle current limit. The output voltage range is +0.8V and +5.0V and fully programmable in non-volatile (static) or volatile (dynamic, on-the-fly) via the serial digital interface. The nominal "coarse" (100mV steps) voltage programming provides flexibility for various types of loads without hardware changes. In the SMB206A/7A/8A the "fine" programming provides "margining" capability for sophisticated system validation and optimization.

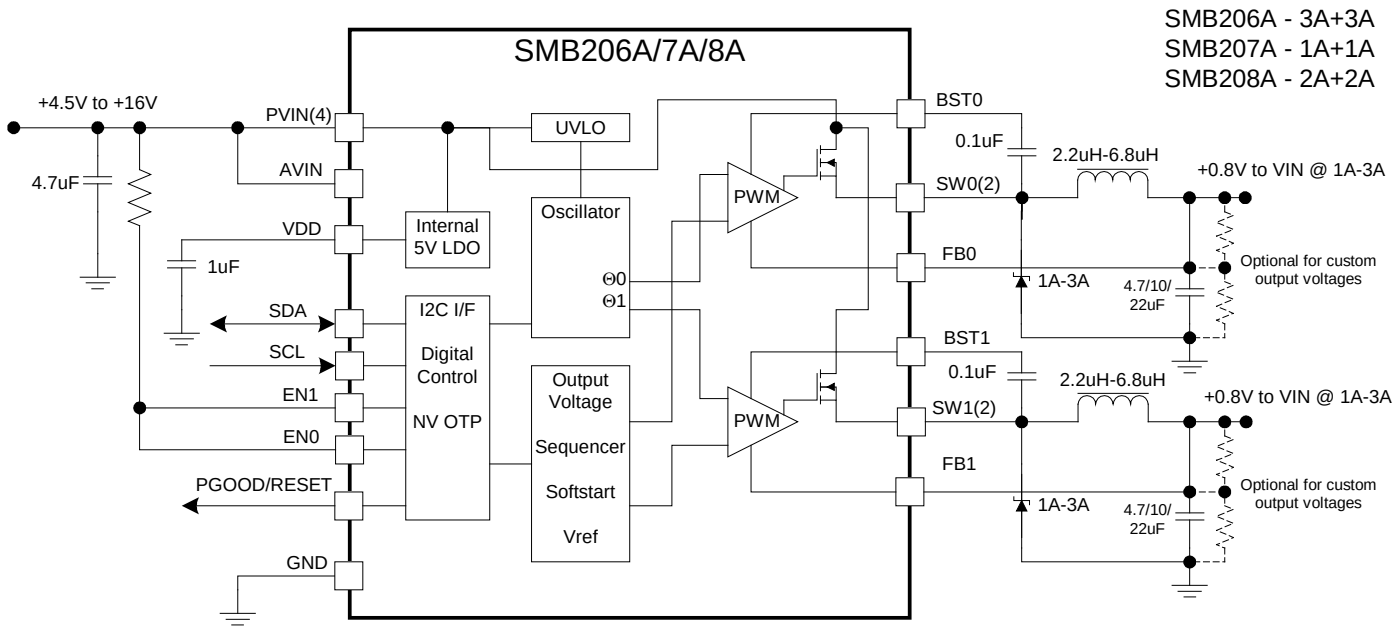
Built-in high-side MOSFETs work in conjunction with external Schottky diode rectifiers in constant frequency PWM-mode at high load currents or high efficiency pulse skipping PFM-mode at light loads. Switching frequency is programmable (500kHz/1000kHz) to trade off efficiency and component size. Each output switches 180^o out of phase with the other to reduce input ripple current, switching noise and input capacitance requirement. Bootstrapped high-side drive improves efficiency and extends the operating voltage range. Frequency compensation is fully integrated to further reduce component count and cost.

POWER CONTROL/MANAGEMENT FUNCTIONS

The SMB206A/7A/8A integrates several power management functions that are typically otherwise performed by external circuits. These include output sequencing with programmable timing, hardware or software-based output enable/disable, and programmable softstart timing. Also, the output voltages are monitored with a programmable PGOOD/RESET output (PGOOD asserts immediately, RESET delays 125ms). Software Enable bits and hardware Enable pins work together to provide flexible power up/down and manual/auto sequencing.

The SMB206A/7A/8A also supports digitally programmable dynamic output voltage. The non-volatile setting determines the power-up/static value but it can be re-programmed by software via the serial interface. The settings are +0.8V to +5.0V and can support dynamic voltage/clock CPU cores or low power memory modes.

Figure 2 - TYPICAL APPLICATION

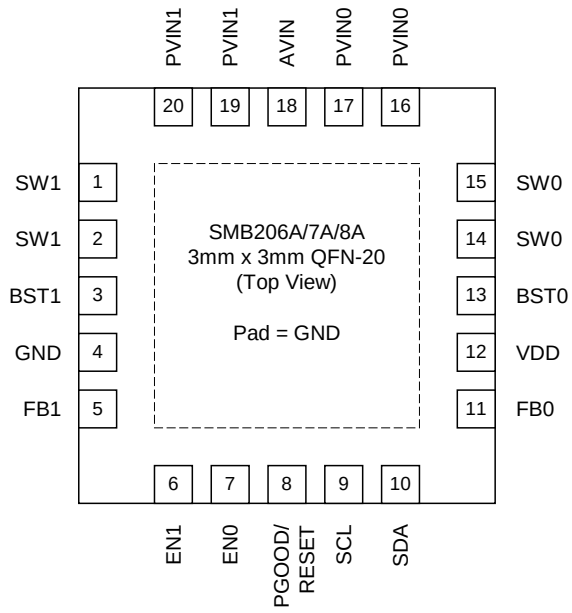


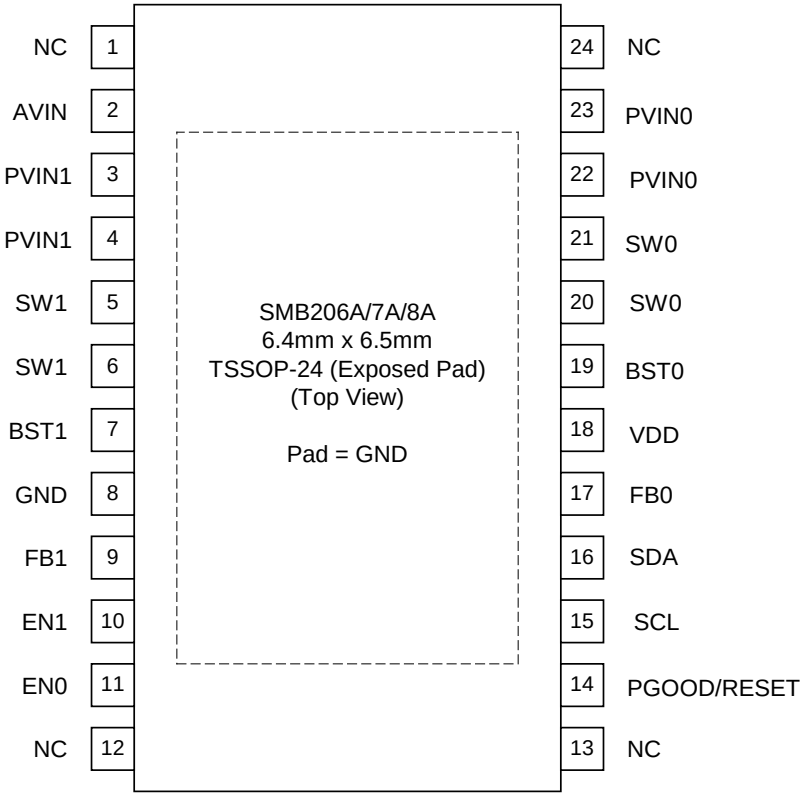
PIN DESCRIPTION

QFN-20 Pin #	TSSOP Pin #*	Pin Name	Pin Type	Pin Description
16, 17, 19, 20	3, 4, 22, 23	PVIN	Power	Power Input - Connect to +4.5V to +16V source. Bypass with 4.7uF MLCC
18	2	AVIN	Power	Analog Power Input - Connect to +4.5V to +16V source (same as PVIN)
12	18	VDD	Power	Internal VDD - +5V internal supply. Bypass with 1uF typical MLCC
4, PAD	8, PAD	GND	Ground	Ground – Connect to PCB isolated ground
9	15	SCL	Input	I^2C Clock
10	16	SDA	I/O	I^2C Data
7,6	11, 10	EN(0/1)	Input	Enable 0/1 – Enables output, high true
14, 15, 1, 2	20, 21, 5, 6	SW0/1	Output	Switch Node 0/1 – Connect to output inductors
13, 3	19, 7	BST0/1	Input	Bootstrap Input – Connect to 0.1uF capacitor to switch node
11, 5	17, 9	FB0/1	Input	Feedback Input 0/1 – Connect to output sense node
8	14	PGOOD/ RESET	Output	PowerGood/RESET Output – Output UV monitor signal (high true, open drain)
NA	1, 12, 13, 24	NC	NC	Not Connected

**Contact factory for TSSOP package*

Figure 3 - PACKAGE AND PINOUT





**Contact factory for TSSOP package*

Figure 4 - TYPICAL OUTPUT TIMING DIAGRAM

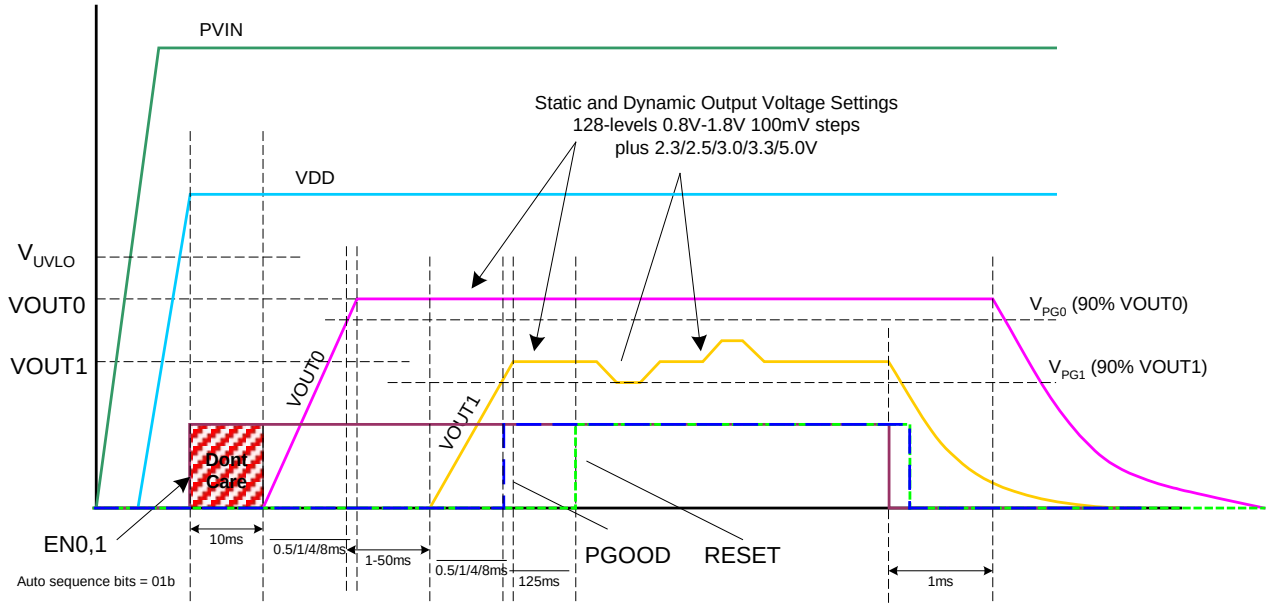
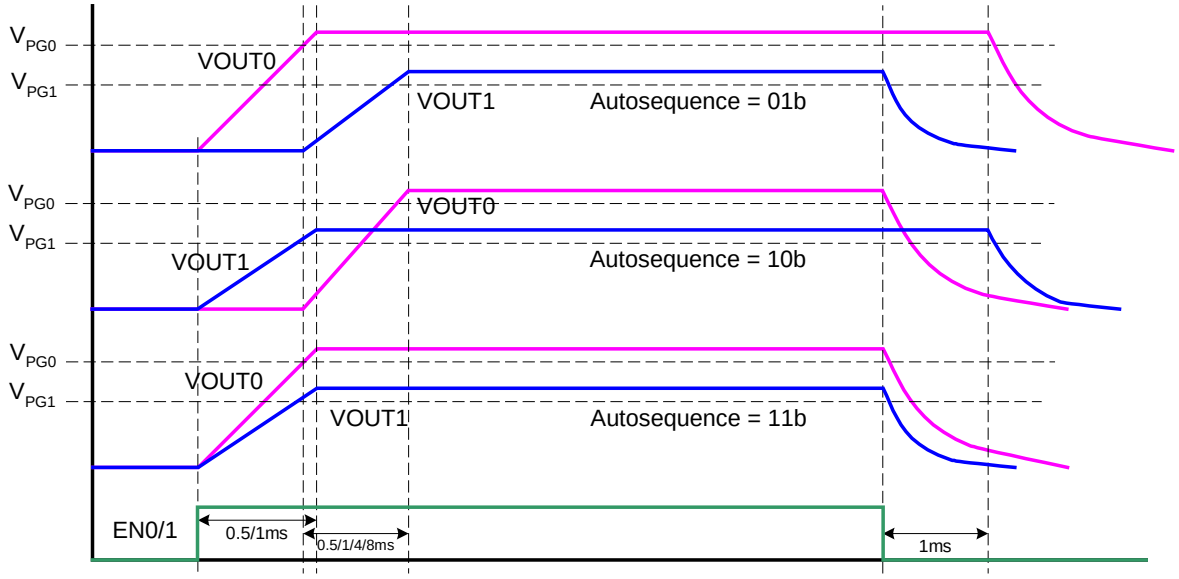


Figure 5 - TYPICAL OUTPUT SEQUENCE DIAGRAM



NOTE: Sequence delay = 0ms, [03h] = 00

OUTPUT STATE/SEQUENCE LOGIC TABLES

OUTPUT STATES

EN0 Pin	EN1 Pin	CH0 enable bit	CH1 enable bit	Chip State	Output Behavior	
					CH0	CH1
Low	Low	X	X	Shutdown	Disabled	Disabled
Low	High	X	0	Shutdown	Disabled	Disabled
High	Low	0	X	Standby	Disabled	Disabled
Low	High	X	1	Shutdown	Disabled	Enabled
High	Low	1	X	Active	Enabled	Disabled
High	High	0	0	Standby	Disabled	Disabled
High	High	0	1	Active	Disabled	Enabled
High	High	1	0	Active	Enabled	Disabled
High	High	1	1	Active	Enabled	Enabled

Note: "X" denotes a "Don't Care" state

OUTPUT SEQUENCING

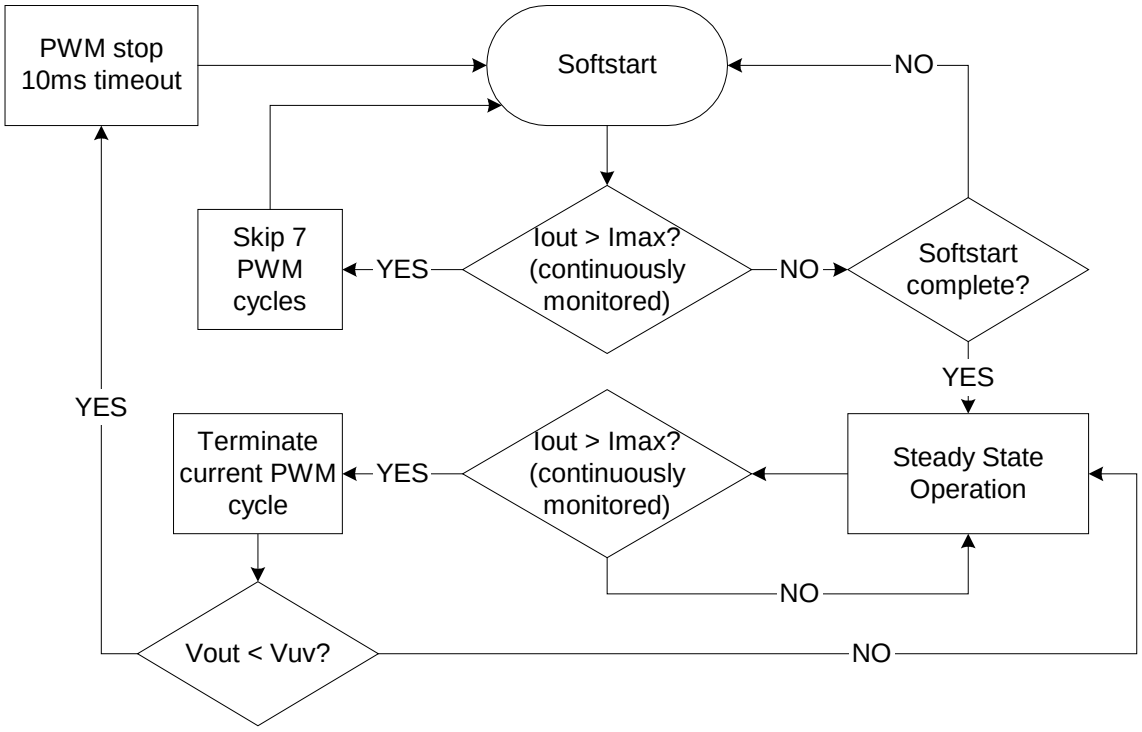
Auto Sequence [02h bits3:2]		Output Behavior*
0	0	CH0/CH1 respond independently to enable pins/bits, no auto-sequence
0	1	CH1 is dependent on CH0 state. CH1 always turns on after and turns off before CH0 (based on PGOOD signals)**
1	0	CH0 is dependent on CH1 state. CH0 always turns on after and turns off before CH1 (based on PGOOD signals)**
1	1	CH0 and CH1 turn on and off together**

**Power down timing is not specifically controlled and is dependent on load current and output capacitance - slew rate is not guaranteed. Assumes input UVLO is cleared. If auto-sequence bit are other than 00b then fault conditions (OC, OT etc.) may shutdown both outputs.*
***Assumes EN pins and enable bits are in the intended states per the Output State Table.*

POWERGOOD/RESET OUTPUT LOGIC TABLE

PGOOD/RESET Assignment [02h bits7:6]	VOUT0	VOUT1	PGOOD/RESET Output
00	VOUT0 < V_{PG0}	VOUT1 < V_{PG1}	Low
	VOUT0 < V_{PG0}	VOUT1 > V_{PG1}	Low
	VOUT0 > V_{PG0}	VOUT1 < V_{PG1}	Low
	VOUT0 > V_{PG0}	VOUT1 > V_{PG1}	High
01	Don't Care	VOUT1 < V_{PG1}	Low
	Don't Care	VOUT1 > V_{PG1}	High
10	VOUT0 < V_{PG0}	Don't Care	Low
	VOUT0 > V_{PG0}	Don't Care	High
11	Don't Care	Don't Care	High

Figure 6 - OVERCURRENT BEHAVIOR (PER OUTPUT)



ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -65°C to +150°C
Junction Temperature ..... -55°C to +150°C
Lead Solder Temperature (10s) ..... 300°C
Terminal Voltage with Respect to GND:
- PVIN, AVIN, SW, EN0/1 ..... +18V
- BST, PVIN ..... +6.5V
- All Others ..... +6.5V

Output Short Circuit Current (Any single pin) 3A
ESD Rating per JEDEC (HBM)
- VDD 1000V
- All Other Pins 2000V

Latch-Up testing per JEDEC ..... ±100mA

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Ambient Temperature Range ..... -40°C to +85°C
Junction Temperature Range ..... -40°C to +125°C
PVIN, AVIN ..... +4.5V to +16V
Package Thermal Resistance (θ_{JA})
20 Pad 3mm x 3mm QFN ..... 47°C/W
24 Pin 6.5mm x 6.4mm TSSOP* ..... 38°C/W
Moisture Classification .....
..... Level 3 (MSL 3) per J-STD- 020

RELIABILITY CHARACTERISTICS
Data Retention ..... 20 Years

**Contact factory for TSSOP package*

ELECTRICAL OPERATING CHARACTERISTICS

PVIN = +12V, VDD = +5V, $T_A = T_J$ = -40°C to +85°C unless otherwise noted. Typical values are +25°C, Note 1,2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main Supply						
V_{IN}	Main input supply voltage (PVIN)		4.5		16	V
V_{DD}	Internal LDO supply voltage (VDD)	V_{IN}>5.5V, I_{DD}<10mA	4.5		5.5	V
I_{IN}	Input supply current (PVIN)	Outputs enabled, no load		2	10	mA
$I_{IN-STBY}$	Standby supply current	EN pins high, Output enable bits disabled, I^2C active		0.3	1	mA
$I_{IN-SHDN}$	Shutdown supply current	EN pins low		1	5	uA
V_{UVLO}	Input Undervoltage lockout (VDD monitored)	VDD Rising	3.75	4.0	4.25	V
		VDD Falling (relative to VDD Rising)		-10		%
T_{SHDN}	Thermal shutdown threshold	Temp rising		140	150	°C
T_{HYST}	Thermal shutdown hysteresis			20		°C

Note 1: Parametric tolerances are only guaranteed for factory-programmed settings. Changing configuration settings from that reflected in the customer specific CSIR code may result in inaccuracies exceeding those specified above.
Note 2: MIN/MAX limits are guaranteed by test, characterization or design.

ELECTRICAL OPERATING CHARACTERISTICS (CONTINUED)

PVIN = +12V, VDD = +5V, T_A = T_J = -40°C to +85°C unless otherwise noted. Typical values are at +25°C, Note 1,2						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Step-down regulators (CH0,1)						
V_{OUT}	Coarse Output Voltage	Programmable 0.8V-1.8V (100mV steps) and 2.3/2.5/3.0/3.3/5.0V 0.1A to Full DC Load	-2.5		+2.5	%
DV_{OUTF}	Fine Output Voltage Offset	Programmable +1.14% to 7.95% relative to coarse output voltage (3-bits)	0		+7.95	%
SRV_{OUT}	Dynamic Output Voltage Slew Rate (Note 3)	V_{FB} slew from completion of I^2C write (0.8V-1.8V only)	103	128	153	us/step
ΔV_{LINE}	Line regulation	$\Delta V_{OUT}/\Delta V_{IN}$ (10V < V_{IN} < 14V)		1	3	mV/V
I_{FB}	Feedback pin current			1		uA
F_{SW}	PWM Switching frequency	Programmable 500/1000kHz	-15		15	%
Θ	Phase interleave	CH0 vs. CH1		180		deg
R_{DSH}	High side FET switch resistance	SMB206A/7A/8A		250	400	mΩ
R_{DSL}	Low side FET switch resistance			10		Ω
I_{LIM}	Switch Peak Current Limit	SMB207A (CH0/CH1)		1.5/1.5	2/2	A
		SMB208A (CH0/CH1)		3/3	4/4	A
		SMB206A (CH0/CH1)		4.5/4.5	6/6	A
T_{HO}	Startup holdoff time			10		ms
T_{SS}	Softstart/stop slew	Programmable 0.5/1.0ms (1 bit)	-20		+20	%
T_{SEQ}	Sequence delay	Programmable 1.5-50ms (2 bits)	-20		+20	%
$V_{PG0,1}$	Output PGOOD/RESET threshold	$V_{OUT0,1}$ rising Relative to nominal coarse setting	85	90	95	%
T_{BPG}	PGOOD/RESET blanking time	After last step of V_{FB} during dynamic output voltage (Note 3)		192		us
T_{UVPG}	Output PGOOD/RESET glitch filter	V_{OUT} falling		32		us
T_{RST}	RESET Output Delay	V_{OUT} rising	100	125	200	ms
V_{UV}	Output undervoltage threshold (short circuit)	% of V_{OUT}, V_{OUT} falling	52.5	62.5	72.5	%
$V_{HYST-UV}$	UV threshold hysteresis (short circuit)	% of V_{OUT}, V_{OUT} rising		3		%
Logic Inputs/Outputs (EN0/1, SDA/SCL, PGOOD/RESET)						
V_{IH}	Input high voltage		1.4			V
V_{IL}	Input low				0.6	V
V_{OL}	Open drain outputs	I_{SINK} = 3mA		0.3		V

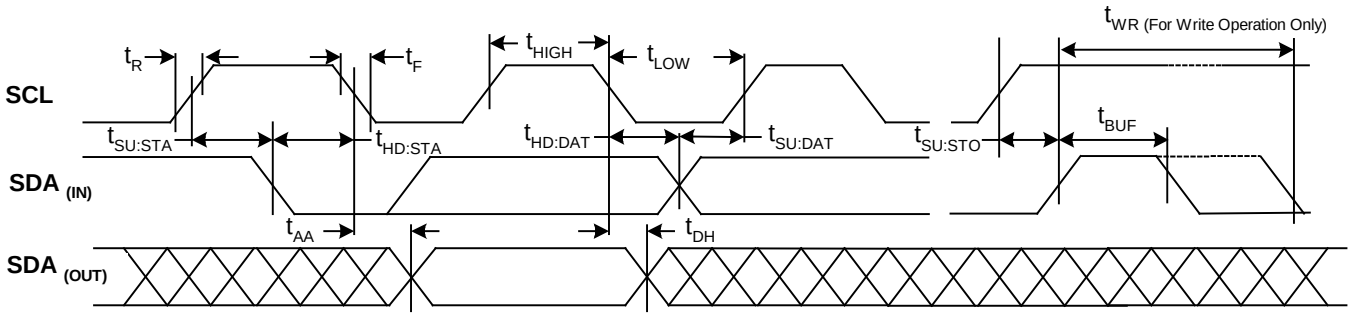
Note 1: Parametric tolerances are only guaranteed for factory-programmed settings. Changing configuration settings from that reflected in the customer specific CSIR code may result in inaccuracies exceeding those specified above.
Note 2: MIN/MAX limits guaranteed by test, characterization or design.
Note 3: "Coarse" volatile output voltage writes above 1.8V setting requires a channel disable/re-enable to take effect.

I²C/SMBus SERIAL INTERFACE ELECTRICAL SPECIFICATIONS

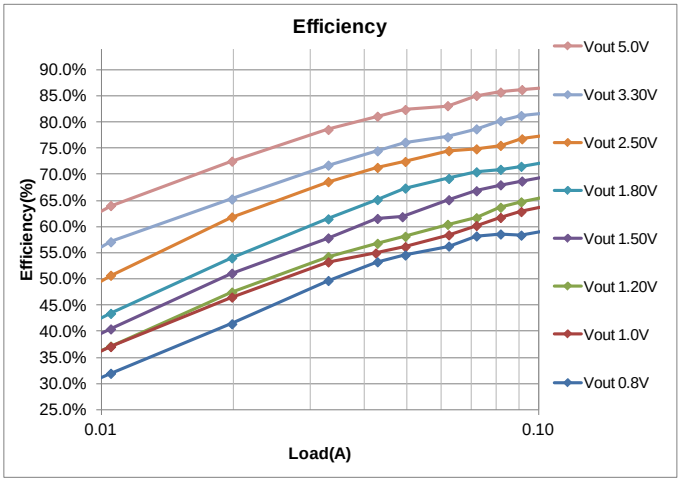
PVIN = +12V, VDD = +5V, T_A = 0°C to +85°C unless otherwise noted. Typical values are +25°C, Note 1,2						
Symbol	**Parameter**	**Conditions**	**400kHz**			
			Min	**Typ**	**Max**	**Units**
f_{SCL}	SCL clock frequency		0		400	kHz
T_{LOW}	Clock low period		1.3			µs
T_{HIGH}	Clock high period		0.6			µs
t_{BUF}	Bus free time between a STOP and a START condition	Before new transmission - Note 1	1.3			µs
$t_{SU:STA}$	Start condition setup time		0.6			µs
$t_{HD:STA}$	Start condition hold time		0.6			µs
$t_{SU:STO}$	Stop condition setup time		0.6			µs
t_R	SCL and SDA rise time		20 + 0.1C_b		300	ns
t_F	SCL and SDA fall time		20 + 0.1C_b		300	ns
$t_{SU:DAT}$	Data in setup time		100			ns
$t_{HD:DAT}$	Data in hold time		0		0.9	µs
t_N	Noise filter SCL and SDA	Noise suppression		100		ns

Note 1: Parametric tolerances are only guaranteed for factory-programmed settings. Changing configuration settings from that reflected in the customer specific CSIR code may result in inaccuracies exceeding those specified above.
Note 2: MIN/MAX limits guaranteed by test, characterization or design.

Figure 7 - I²C/SMBus TIMING DIAGRAM

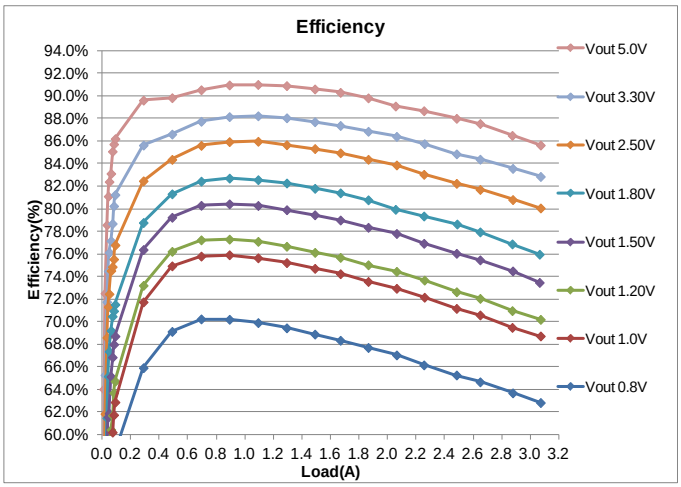


TYPICAL PERFORMANCE GRAPHS



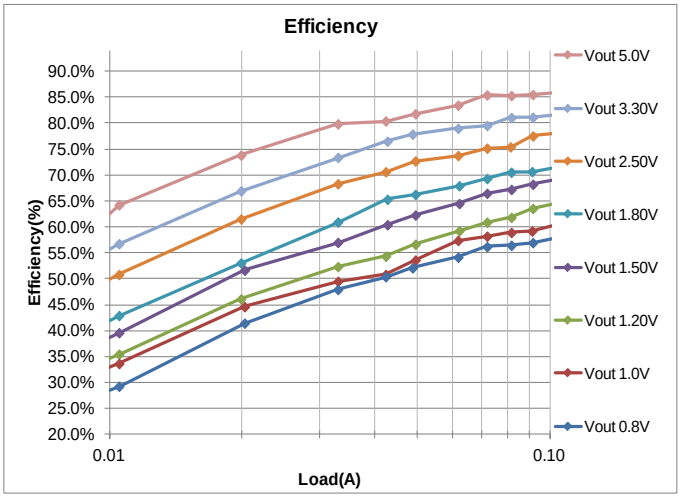
Conditions: Vin = 12V, Vout = 0.8V, 1V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V, Freq = 500KHz

Figure 8: SMB206A Light Load Efficiency Graph



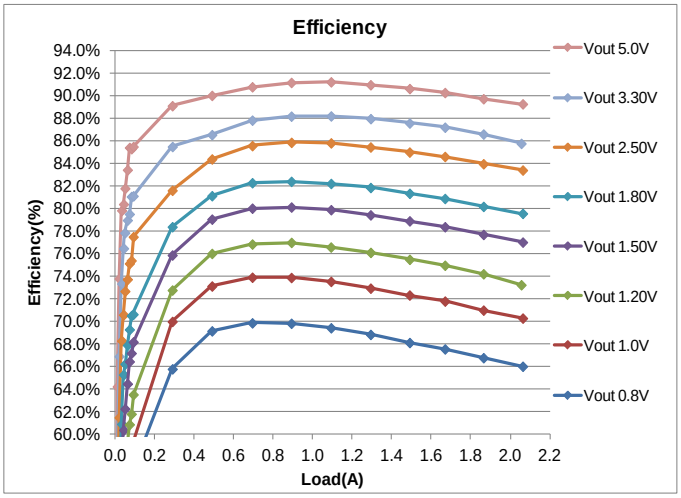
Conditions: Vin = 12V, Vout = 0.8V, 1V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V, Freq = 500KHz

Figure 9: SMB206A Full Load Efficiency Graph



Conditions: Vin = 12V, Vout = 0.8V, 1V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V, Freq = 500KHz

Figure 10: SMB208A Light Load Efficiency Graph



Conditions: Vin = 12V, Vout = 0.8V, 1V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5.0V, Freq = 500KHz

Figure 11: SMB208A Full Load Efficiency Graph

TYPICAL PERFORMANCE GRAPHS (CONTINUED)

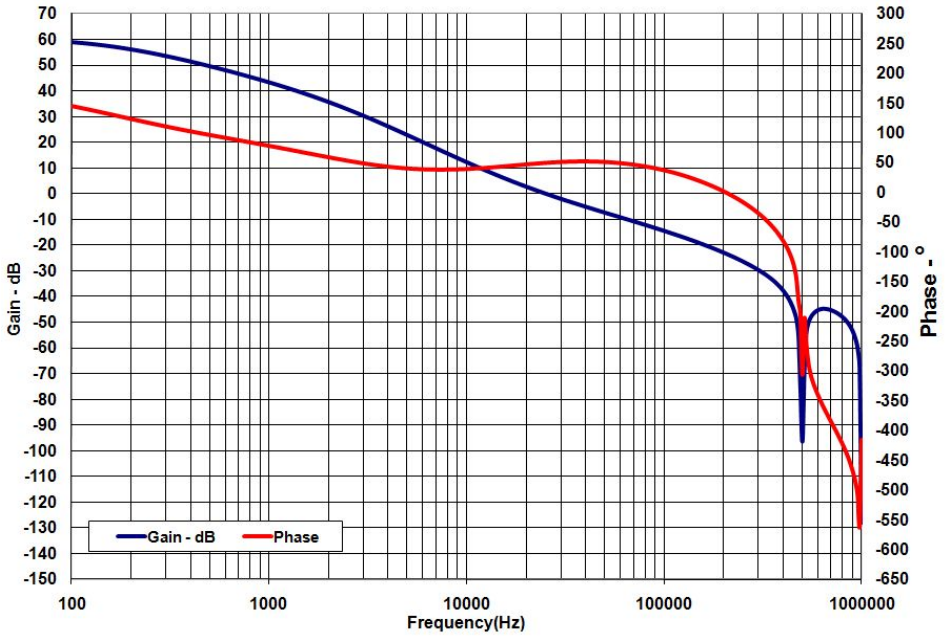


Figure 12: Bode plot of SMB208A circuit displayed in Figure 20 with full load

CONFIGURATION REGISTERS

00h – I²C Slave Address (NV, R/W) – Factory programmable only								
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**I²C Slave Address (read only)**
0	0	0	0	0	0	0	X	LSB for R/W in I²C format
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Volatile Writes to 01h/02h***
X	X	X	X	X	X	X	0	0 = Enable volatile writes to Vout 1 = Disable volatile writes to Vout

01h/02h – Channel 0/1 Output Voltage (NV, R/W)								
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Coarse/Nominal Output Voltage (V)**
0	0	0	0	X	X	X	X	0.800
0	0	0	1	X	X	X	X	0.900
								. .
1	0	0	1	X	X	X	X	1.700
1	0	1	0	X	X	X	X	1.800
1	0	1	1	X	X	X	X	2.300
1	1	0	0	X	X	X	X	2.500
1	1	0	1	X	X	X	X	3.000
1	1	1	0	X	X	X	X	3.300
1	1	1	1	X	X	X	X	5.000
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Fine Output Voltage Offset %**
X	X	X	X	0	0	0	X	0
X	X	X	X	0	0	1	X	+1.14
X	X	X	X	0	1	0	X	+2.27
X	X	X	X	0	1	1	X	+3.41
X	X	X	X	1	0	0	X	+4.55
X	X	X	X	1	0	1	X	+5.68
X	X	X	X	1	1	0	X	+6.82
X	X	X	X	1	1	1	X	+7.95
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Reserved**
X	X	X	X	X	X	X	0	Unused

**"Coarse" volatile output voltage writes above 1.8V setting requires a channel disable/re-enable to take effect*

CONFIGURATION REGISTERS (CONTINUED)

03h – Output Sequencing/Softstart (NV, R/W)								
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**PGOOD/RESET Assignment**
0	0	X	X	X	X	X	X	00 = Both Outputs (dual output only) 01 = CH1 only (dual output only) 10 = CH0 only 11 = None (ignore)
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**PGOOD/RESET**
X	X	0	X	X	X	X	X	0 = PGOOD 1 = RESET
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Output Softstart (ms)**
X	X	X	0	X	X	X	X	See below
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Automatic Output Power-Up Sequence (dual output only)**
X	X	X	X	0	0	X	X	00 = Disabled (pin/bit control) 01 = CH0 then CH1 10 = CH1 then CH0 11 = CH1 and CH0 start together
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**CH1 Output Enable (dual output only)**
X	X	X	X	X	X	0	X	0 = Disable 1 = Enable
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**CH0 Output Enable**
X	X	X	X	X	X	X	0	0 = Disable 1 = Enable

04h – Output Sequencing/Softstart (NV, R/W)								
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Reserved**
0	0	0	0	0	X	X	X	Unused
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Output Softstart (ms)**
X	X	X	0	X	X	X	X	See below
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**PWM frequency (kHz)**
X	X	X	X	X	0	X	X	0 = 500 1= 1000
Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Sequence Delay (ms) (dual output only)**
X	X	X	X	X	X	0	0	00 = 1.5 01 = 12.5 10 = 25 11 = 50

03h[4]	04h[3]	Output Softstart Time (ms)
0	0	1
0	1	8
1	0	0.5
1	1	4

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY (PVIN, AVIN, VDD, GND)

The SMB206A/7A/8A can be powered from an input voltage of between 4.5V -16V applied to the PVIN pins, AVIN and ground. An internal LDO (VDD) is used to supply 5.0V for the gate drive of the internal N-channel MOSFET. Once the voltage applied to PVIN is above 4.0V (UVLO) and an ENx pin is taken high, the channel assigned to the ENx pin will begin switching provided the SMB206A/7A/8A is programmed for pin control (see "POWER-ON/OFF CONTROL" sections). Please note that the EN pin(s) serve dual functions both enabling/disabling channels and serving to place the SMB206A/7A/8A in shutdown or Standby modes.

POWER-ON/OFF CONTROL (EN0, EN1, I^2C Control)

The output(s) on the SMB206A/7A/8A can be turned on/off in a number of different ways:

The ENx pins can be pulled high (to VIN) and once power is applied, the channels will turn on according to one of the following user assigned (programmed) sequences:

1. Channels turn on according to ENx pin(s)
2. Channel 0 followed by Channel 1
3. Channel 1 followed by Channel 0
4. Channel 0 and Channel 1 Start Together

The SMB206A/7A/8A also employs I^2C control of the outputs, requiring only that the ENx pins be pulled high in order to facilitate this control. Using I^2C control allows all the above sequence combinations. Finally, taking EN0 low places the part in low current shutdown mode (see "OUTPUT STATE/SEQUENCE LOGIC TABLES" section).

SWx PIN(S)

The internal N-channel MOSFET(s)' source connection appears at the SW nodes where the external inductor, Bootstrap capacitor, and Schottky diode are all connected. The internal MOSFET gate is driven by the VDD supply working in conjunction with the Bootstrap capacitor to allow the MOSFET gate to be driven to VIN plus 5V. The MOSFET current is internally limited and the switching cycle is terminated when the current limit threshold is exceeded. An internal low current, low-side, N-channel MOSFET is provided for keeping the Bootstrap capacitor charged when there is no or minimal load on the output. This MOSFET is not to be used in place of the external Schottky as it will not support high currents.

Connections to the inductor, Schottky, and Bootstrap capacitor must be as short as possible and the trace width maximized to the inductor and Schottky paths. Minimum trace width should be at least 0.050".

FB

Each channel has a unique FB (Feedback) pin where the output voltage is internally connected to the inverting input of the internal transconductance amplifier. The SMB206A/7A/8A requires no external resistive divider from the output to the FB node for output voltages between 0.8V to 5.0V. Further, the SMB206A/7A/8A requires no external compensation components as the compensation is optimized internal to the part.

PGOOD/RESET

This open drain pin indicates that all channels assigned to this pin are functional and within the user-programmed values plus or minus the amount for under and overvoltage.

Each output can have a PGOOD/RESET associated with it or one can choose not to have this function associated with one or all channels.

The RESET pin is low when the channel is off, or out of spec for voltage, or an overcurrent and will go high when the channels(s) are within spec after a delay of 125mS. The PGOOD function acts as the RESET with the exception that is has no delay once all channels are within spec (see "POWERGOOD/RESET OUTPUT LOGIC TABLE" section).

BOOTSTRAP

This pin connects to a high quality, low-ESR ceramic capacitor of 0.1uF to power the internal gate drive to VIN plus VDD (5.0V nominal). The BST capacitor is initially charged to 5.0V when the part is turned on and the output is off. When the output is turned on, the capacitor voltage is refreshed each time the internal MOSFET is turned off via the external Schottky when it is forward biased. When there is little or no load, the SMB206A/7A/8A refreshes the Bootstrap capacitor as required.

OVERTEMPERATURE

The SMB206A/7A/8A family contains an overtemperature shutdown circuit that shuts down all channels when the die temperature exceeds 140°C (nominal). Operation may resume when the internal die temperature falls to below 120°C (nominal).

APPLICATIONS INFORMATION

PROGRAMMABLE DEVICE PARAMETERS

OUTPUT VOLTAGE(S)

Output voltages for all channels are user programmable from 0.8V to 5.0V according to the below:

0.8V to 1.8V in 0.1V increments followed by;
2.3V, 2.5V, 3.0V, 3.3V, 5.0V

For any setting, a fine adjust is available whereby the user can fine tune the output voltage in steps of +1.14% of nominal up to +7.95% of nominal.

OPERATING FREQUENCY SELECTION

The SMB206A/7A/8A switch frequency is user programmable to operate at 500kHz or 1MHz. This setting must not be changed when the outputs are enabled. First, disable the output and then select the frequency.

SOFT START

Two soft start ramp times are available, affecting both channels. With a selection of 0.5mS or 1.0mS, choose the value that best suits the application keeping in mind that these softstart periods apply to the programmed output voltage and will cause higher turn-on slew rates when higher output voltages are programmed.

Note: When using large values of output capacitance use the below formula to ensure the output can start within the programmed soft start interval:

$$\frac{C_{OUT} * V_{OUT}}{Softstart(t)} + I_{OUT} \leq I_{LIM}$$

Where:
C_{OUT} = Total output capacitance in Farads
V_{OUT} = Nominal output voltage setting
I_{OUT} = Maximum output load current (during the SS interval)
Softsstart = softstart time in seconds
I_{LIM} = 3A

Using too large of output capacitance combined with the output load can lead to a failed softstart event which will force the part to rest for 10mS and retry (see Figure 6).

POWER-ON SEQUENCING SLOTS

Power on sequencing with multiple channels is user programmable as shown below:

1. Ch 0 > Ch 1
2. Ch 1 > Ch 0
3. Ch 0 & Ch 1 turn on are coincident
4. Disabled. This mean the channels will not turn on until the associated EN pin is pulled high.

POWER-ON SEQUENCING DELAY(S)

Four sequence on time delays are available: 1.5mS, 12.5mS, 25mS, and 50mS. This is the delay time between the first channel reaching 90% of nominal to the time the second channel begins turning on (Figure 13). This same delay time applies to turn off but the channel sequence position is reversed (Figure 14).

CASCADED SEQUENCING

As shown in Figure 13, the SMB206A/7A/8A Family of controllers features cascaded channel sequencing whereby a channel (in a dual-channel device) will turn on once the first channel has reached its UV threshold and the “Power On Sequencing Delay” period is expired. Note that in Figure 14, the channels sequence off in the opposite order. Cascaded sequencing requires the controller be programmed for the channels to come on at different times.

Cascaded sequencing between devices is also possible by connecting the PGOOD pin of the first controller to the ENABLE of the second or subsequent controller. This allows cascaded sequencing for power-on but does not permit power off sequencing.

APPLICATIONS INFORMATION

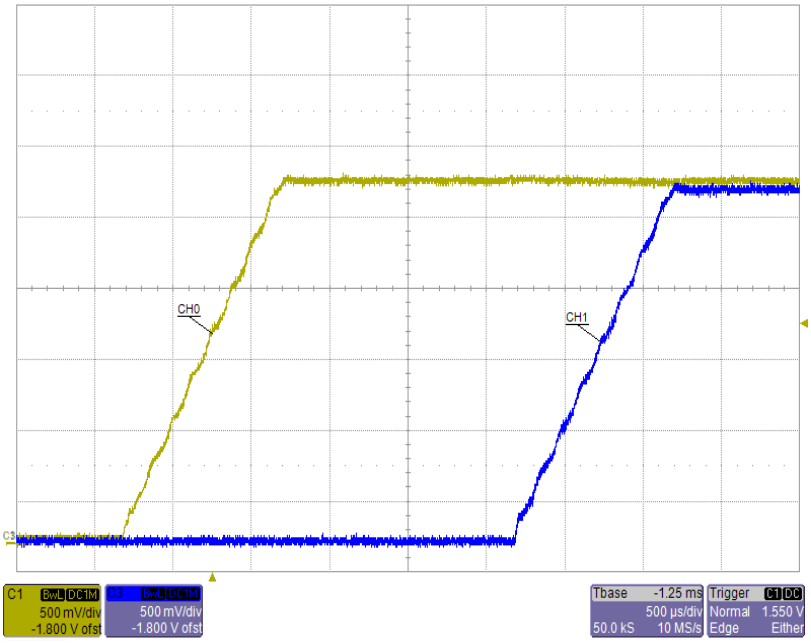


Figure 13: Ch 0 to Ch 1 Sequence on with 1.5mS delay

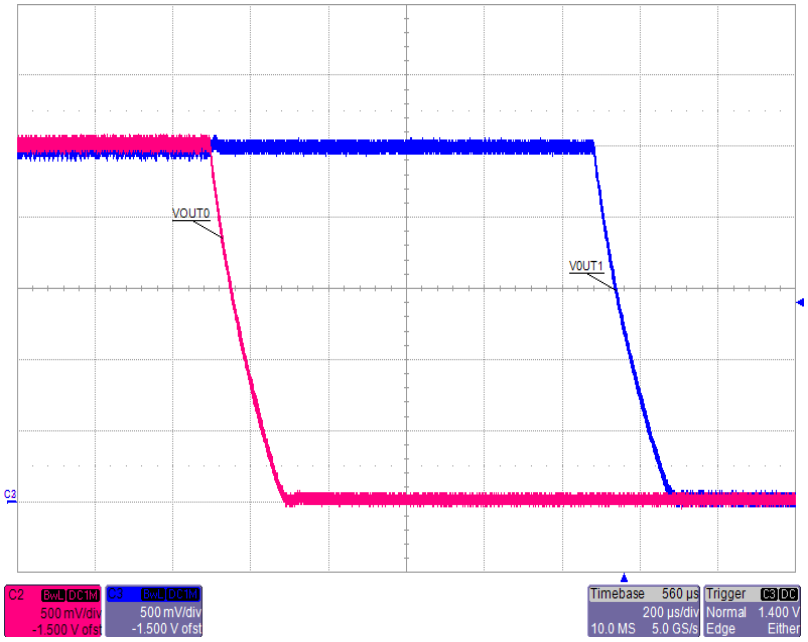


Figure 14: Ch 1 to Ch 0 Sequence off with 1.5mS delay

APPLICATIONS INFORMATION

Cascaded Auto Sequencing Options:
1.) 0,1,2,3
2.) 0,1,3,2
3.) 1,0,2,3
4.) 1,0,3,2

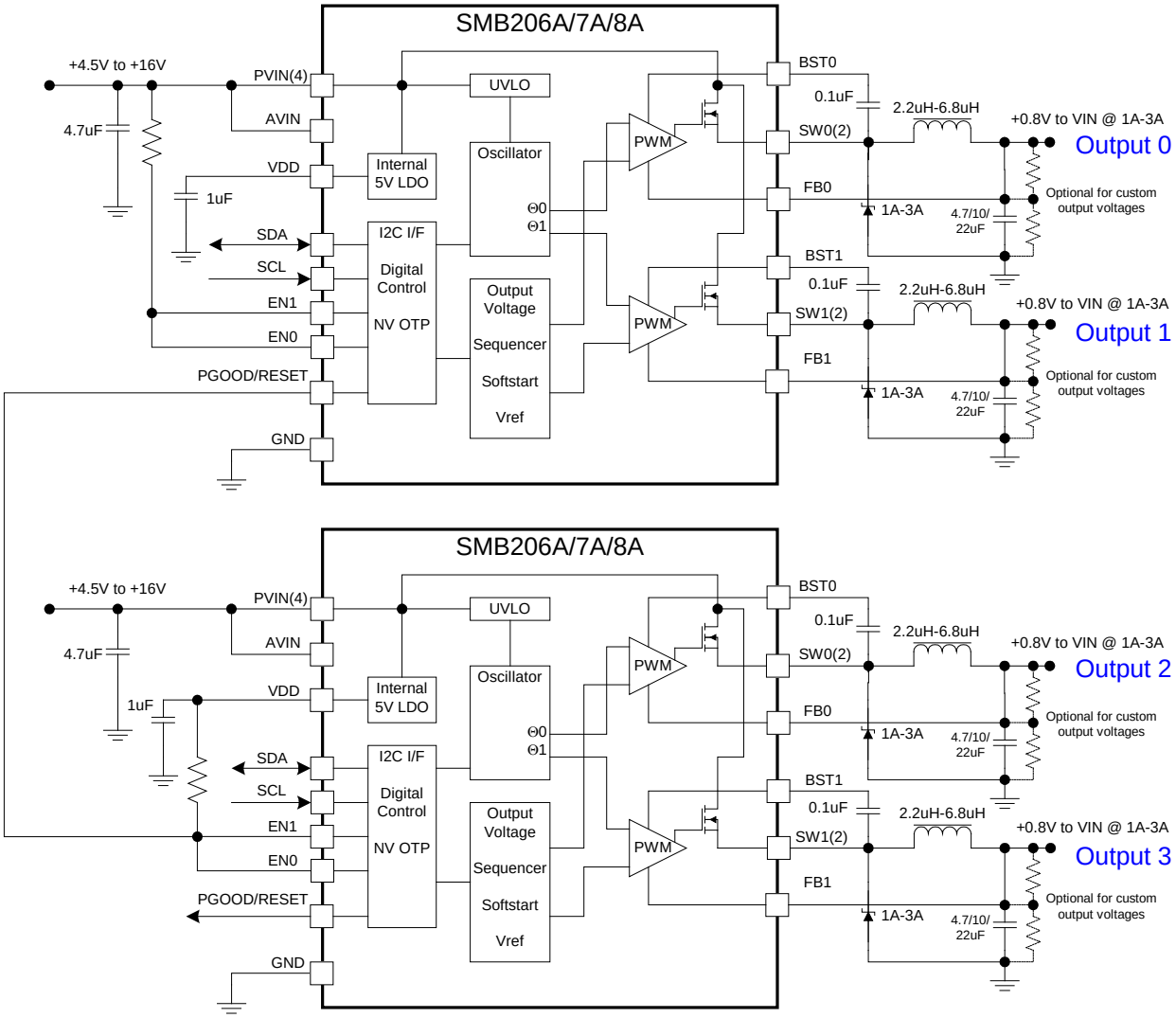


Figure 15: Cascaded Auto Sequencing

APPLICATIONS INFORMATION

EXTERNAL COMPONENT SELECTION

OUTPUT L & C

The inductor and filter capacitor is chosen according to system requirements. These include the minimum to maximum input voltage, nominal output voltage, maximum output current and maximum allowable output ripple. For these criteria we use equations 1-3 to determine the optimal value of L and C. The chosen output capacitor's ESR will impact the system ripple and therefore must be taken into account. For this, we use Equation 3 to determine the maximum allowable ESR.

Eq 1. $$L \geq \frac{V_{OUT}(1-\sigma)}{0.4\, f_{SW} I_{OUT}}$$

Where σ is the duty cycle $\frac{V_{OUT}}{V_{IN}}$

Eq 2. $$ESR_{COUT} \leq \frac{V_{P-P}}{I_{L(P-P)}}$$

Eq 3. $$C \geq \frac{I_{LP-P}}{8\, f_{SW} V_{P-P}}$$

A practical example involves the below system requirements:

V_{IN} = 12V

V_{OUT} = 1.8V

$I_{OUT(Max)}$ = 2.0A (SMB208A), use 50% of this amount to guarantee the inductor current is in CCM for most loads.

P-P Ripple (Max) = 50mV

First, solve for the minimum inductor value:

$$L \geq \frac{1.8 \cdot \left(1 - \frac{1.8}{12}\right)}{0.4 \cdot 5 \cdot 10^5 \cdot 1.0} \geq 7.4 \cdot 10^{-6} : \text{Use } 6.8\text{uH}$$

Now find the inductor ripple current:

$$I_{LP-P} = \frac{V_{OUT}(1-\sigma)}{L \cdot f_{SW}} = \frac{1.8 \cdot 0.85}{6.8 \cdot 10^5 \cdot 5 \cdot 10^5} = 0.45A$$

Next, solve for the maximum allowable ESR for the output capacitor, followed by the minimum capacitor value required to meet the output ripple spec given the ripple current flowing through the inductor.

$$ESR_{COUT} \leq \frac{0.05}{2.1} \leq 24m\Omega$$

$$C \geq \frac{0.45}{8 \cdot 5 \cdot 10^5 \cdot 0.05} \geq 2.25 \cdot 10^{-6}$$

The calculated value of capacitance is much less than the minimum recommended for stable loop operation of the SMB208A (10uF), so choose 2 x 10uF capacitors with each having a maximum ESR at 500kHz of 24milliohms (0.024/2 = 0.012) or less.

APPLICATIONS INFORMATION

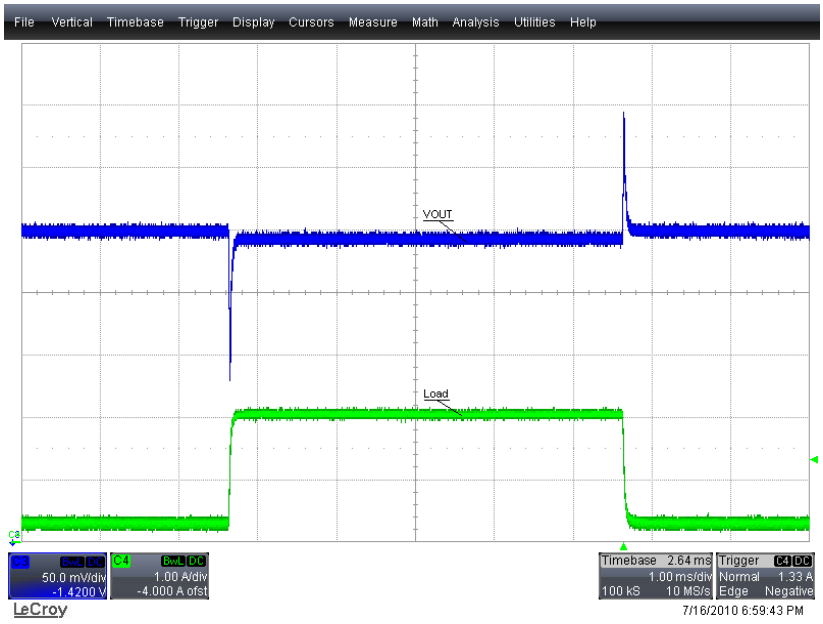


Figure 16: Transient load response: 5VIN, 1.5VOUT 0.2A-2A current Step

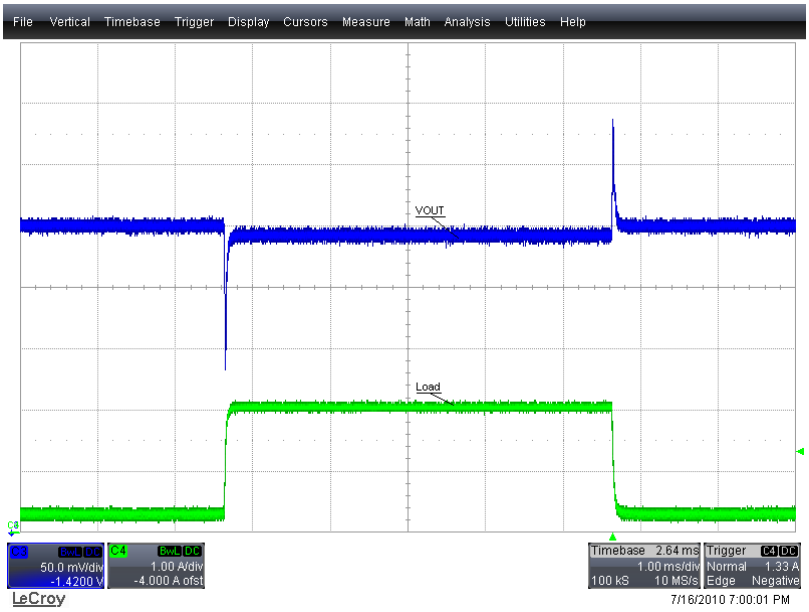


Figure 17: Transient load response: 12VIN, 1.5VOUT 0.2A-2A current Step

APPLICATIONS INFORMATION

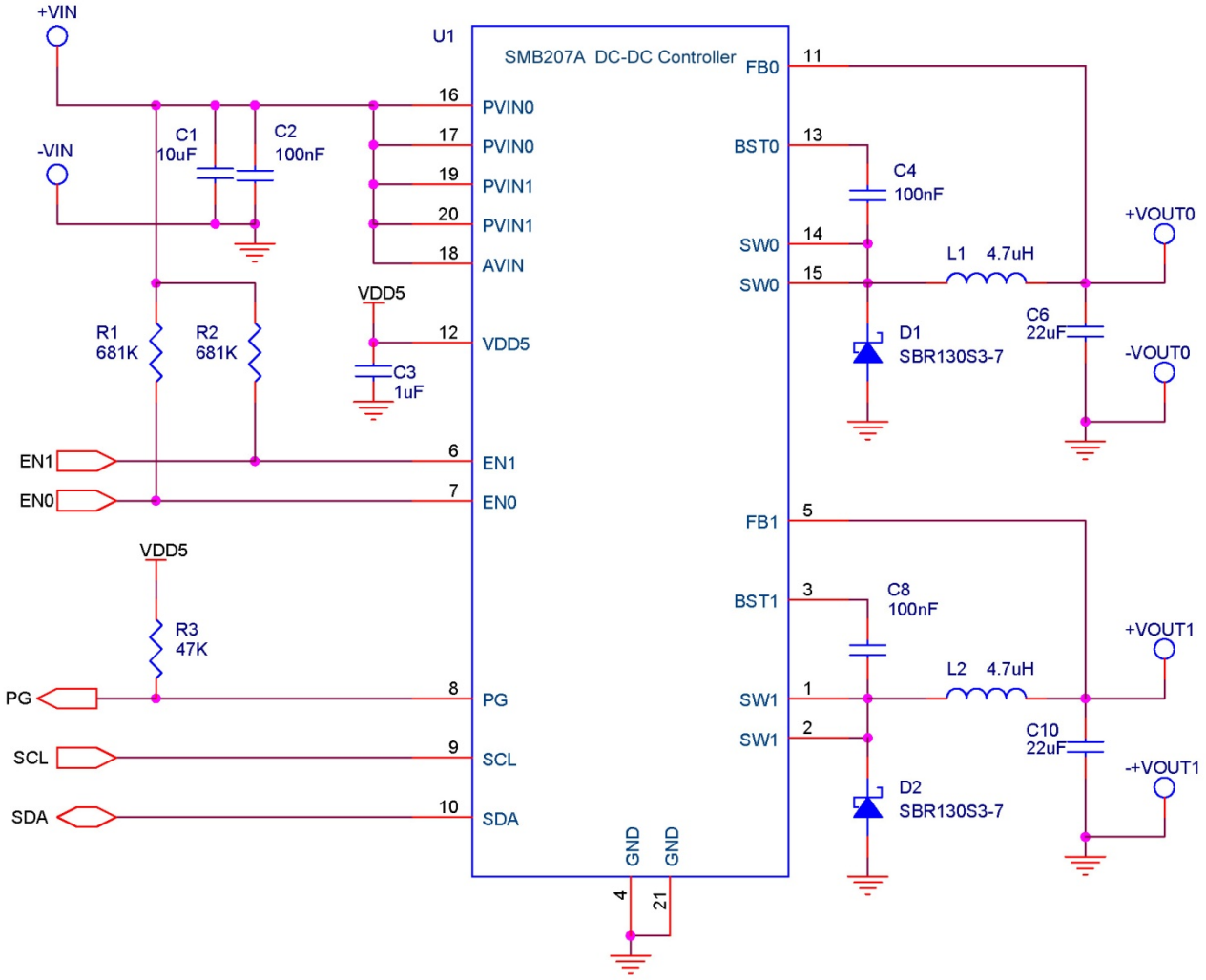
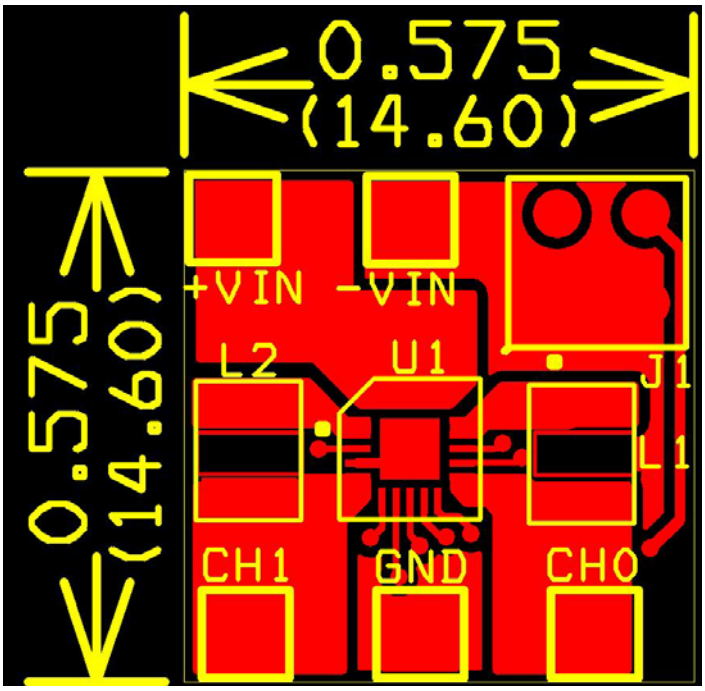


Figure 18: SMB207A Detailed Schematic

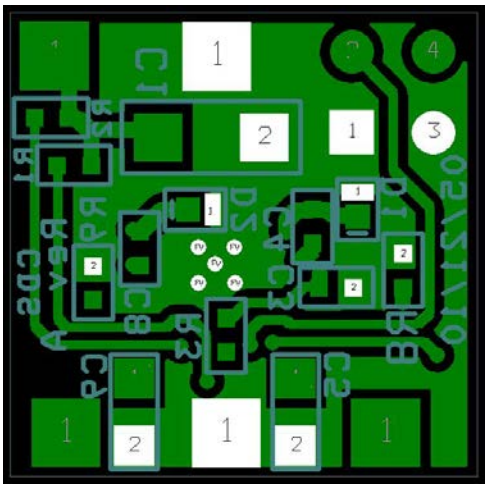
SMB207A BILL OF MATERIALS

Item#	Quantity	Description	Ref Des	Manufacturer	Manufacturer P/N
1	1	10UF 25V CERAMIC X5R 1206	C1	Panasonic	ECJ-3YB1E106K
2	1	CAP CER 4.7UF 6.3V X5R 0402	C3	Panasonic	ECJ-0EB0J475M
3	2	0.1uF 16V 10% X7R 0402	C4, C8	EPCOS Inc	B37921C9104K60
4	2	CAP CER 22UF 10V X5R 0805	C5, C9	Panasonic	ECJ-2FB1A226M
5	2	Schottky diode, 3 pin, common anode	D1, D2	Diode Inc	SBR1U40LP-7
6	2	4.7uH Inductor 1.3A 20% 1210 SMD	L1, L2	Taiyo Yuden	BRL3225T4R7M
7	2	RES 681K OHM 1/16W 1% 0402	R1, R2	Any	
8	1	RES 47K OHM 1/16W 5% 0402	R3	Any	
9	1	DC-DC Controller	U1	Summit Micro	SMB207A

APPLICATIONS INFORMATION



Top Layer



Bottom Layer

Figure 19: Typical SMB207A layout displaying placement of critical components and trace routing

APPLICATIONS INFORMATION

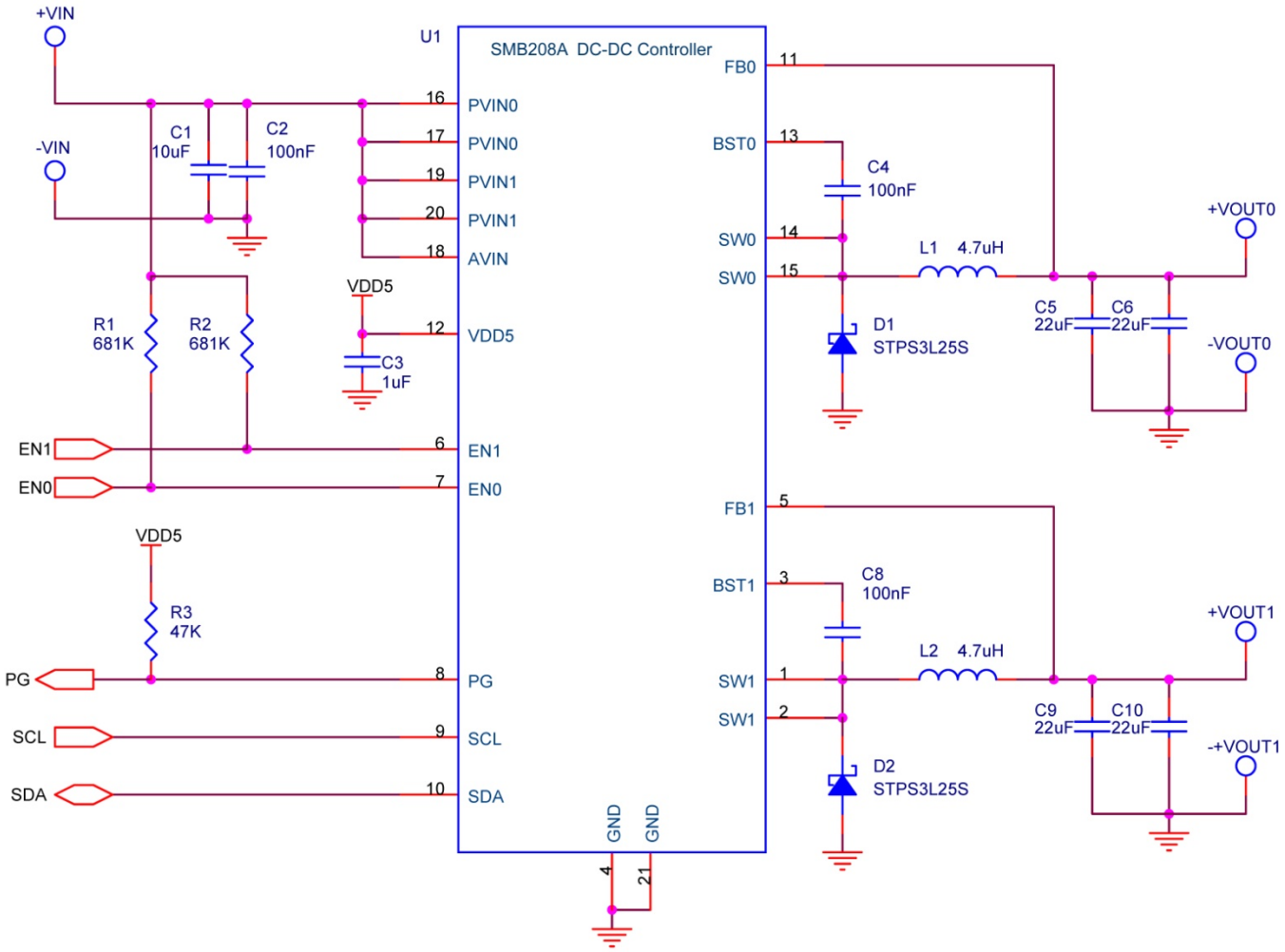
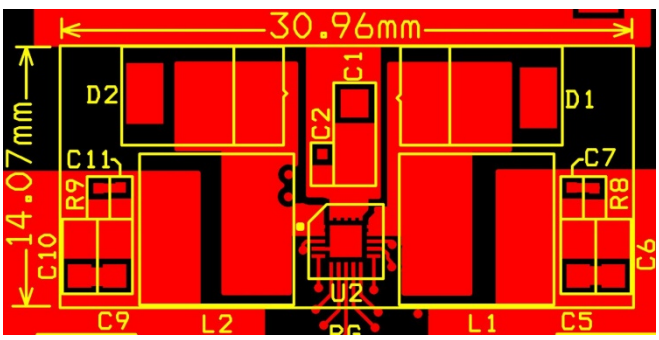


Figure 20: SMB208A Detailed Schematic

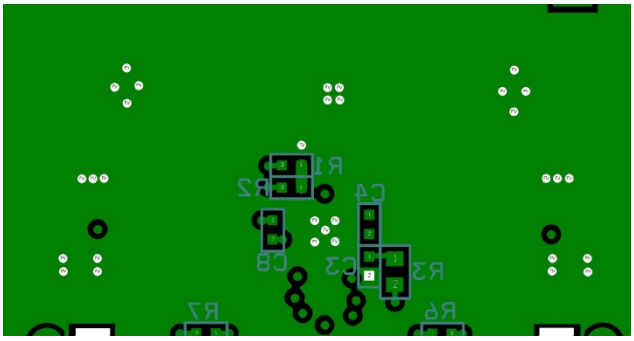
SMB208A BILL OF MATERIALS

Item Number	Qty	Description	Ref Des	Manufacturer	Manufacturer P/N
1	1	10UF 25V CERAMIC X5R 1206	C1	Panasonic	ECJ-3YB1E106K
2	1	CAP CER 4.7UF 6.3V X5R 0402	C3	Panasonic	ECJ-0EB0J475M
3	2	0.1uF 16V 10% X7R 0402	C4 C8	EPCOS Inc	B37921C9104K60
4	2	CAP CER 22UF 10V X5R 0805	C5 C9	Panasonic	ECJ-2FB1A226M
5	2	Schottky diode, 3 pin, common anode	D1, D2	Diode Inc	SBR1U40LP-7
6	2	4.7uH Inductor 1.3A 20% 1210	L1, L2	Taiyo Yuden	BRL3225T4R7M
7	2	RES 681K OHM 1/16W 1% 0402	R1, R2	Any	
8	1	RES 47K OHM 1/16W 5% 0402	R3	Any	
11	1	DC-DC Controller	U1	Summit Micro	SMB208A

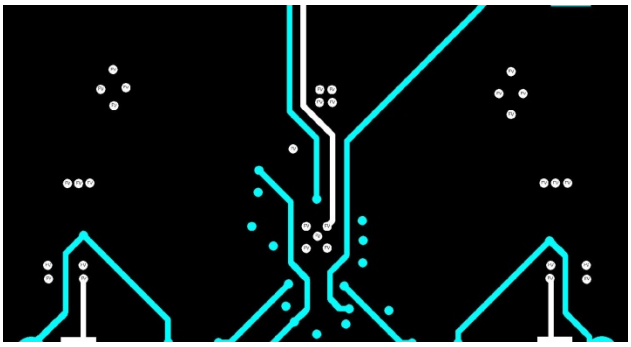
APPLICATIONS INFORMATION



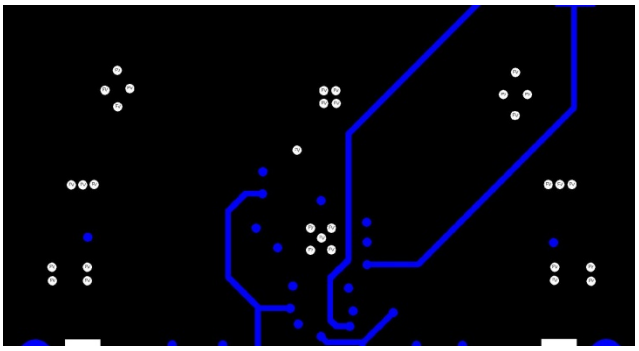
Top Layer



Bottom Layer



Inner Layer 1

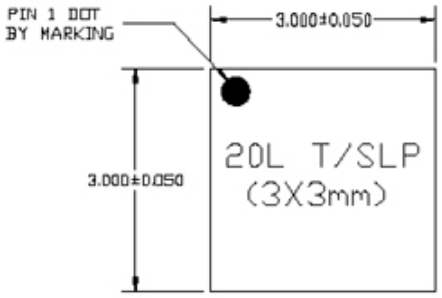


Inner Layer 2

Figure 21: SMB208A typical bottom layer layout displaying placement of critical components and trace routing

PACKAGE DIMENSIONS (QFN-20)

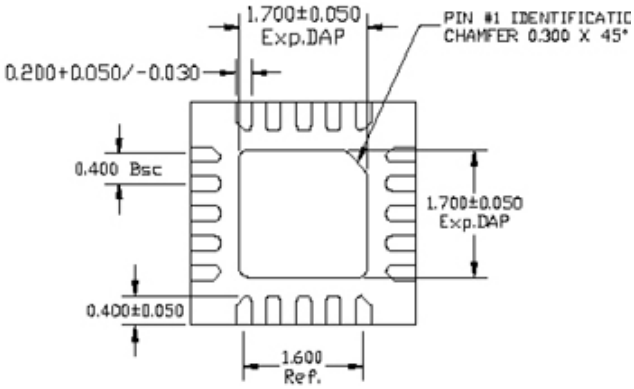
TOP VIEW



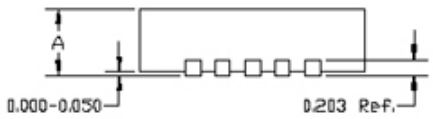
NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS.

		TSLP	SLP
A	MAX.	0.810	0.900
	NOM.	0.750	0.850
	MIN.	0.710	0.800

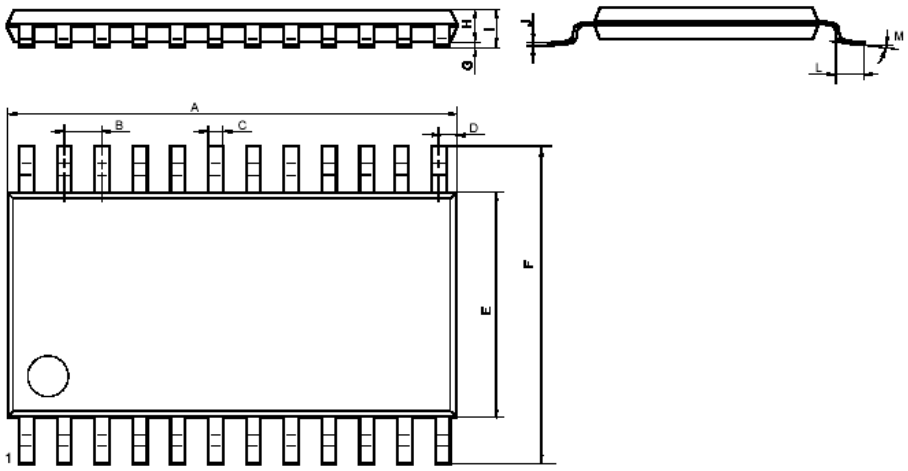
BOTTOM VIEW



SIDE VIEW



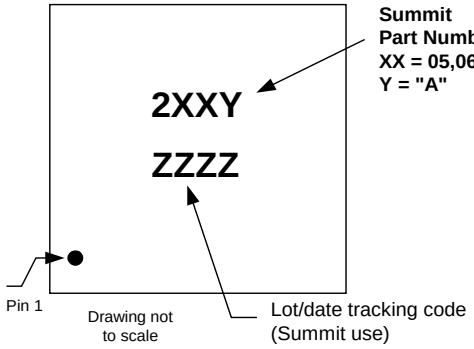
PACKAGE DIMENSIONS (TSSOP-24)



[mm]		
	Min.	Max.
A	7.70	7.90
B	0.65 BSC	
C	0.19	0.30
D	0.275	0.375
E	4.30	4.50
F	6.40 BSC	
G	0.05	0.15
H	0.85	0.95
I	-	1.10
J	0.09	0.20
K	-	
L	0.50	0.60
M	0 DEG	8 DEG

**Contact factory for TSSOP package*

PART MARKING



ORDERING INFORMATION

SMB2XXY Z T nnnn L

Summit Part Number
XX = 05,06,07,08
Y = "A"

Package
N=20 Pad QFN
T=24 Pin TSSOP

T = Tape & Reel

Part Number Suffix
Specific requirements are contained in the suffix

Environmental Attribute
L = 100% Sn Free, RoHS Compliant

**Contact factory for TSSOP package*

NOTICE

NOTE 1 - This is an ***Preliminary*** data sheet that describes a Summit product currently in development. It is meant solely as a product description and should not be used as a design tool.

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