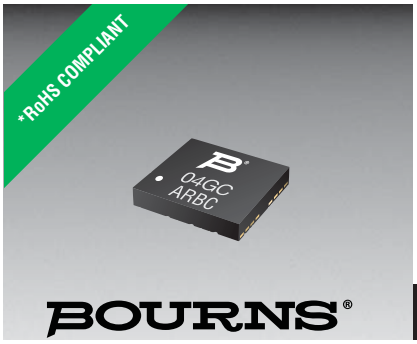


Features

- Formerly FulTec brand
- Extremely high speed performance
- Low impedance
- Two TBU™ protectors in one small package
- Very high bandwidth, GHz compatible
- Simple, superior circuit protection
- RoHS compliant*, UL Recognized

Applications

- xDSL (ADSL, VDSL, VDSL2)
- High Data Rate Interface IC protection (LVDS, HDMI, etc.)
- Industrial sensors and controls
- General electronics

TBU™ P40-G Protectors

Transient Blocking Units - TBU™ Devices

Bourns® Model P40-G products are high speed bidirectional protection components, constructed using MOSFET semiconductor technology, designed to protect against faults caused by short circuits, AC power cross, induction and lightning surges.

The TBU™ high speed protector, triggering as a function of the MOSFET, blocks surges and provides an effective barrier behind which sensitive electronics are not exposed to large voltages or currents during surge events. The TBU™ device is provided in a surface mount DFN package and meets industry standard requirements such as RoHS and Pb Free solder reflow profiles.

Agency Approval

UL recognized component File # E315805.

Industry Standards

Description		Model
Telcordia	GR-1089	P40-G
ITU-T	K.20, K.20E, K.21, K.21E, K.45	

Absolute Maximum Ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{imp}	Maximum protection voltage for impulse faults with rise time ≥ 1 µsec	40	V
V_{rms}	Maximum protection voltage for continuous V_{rms} faults	28	V
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-65 to +150	°C

Electrical Characteristics (T_{amb} = 25 °C)

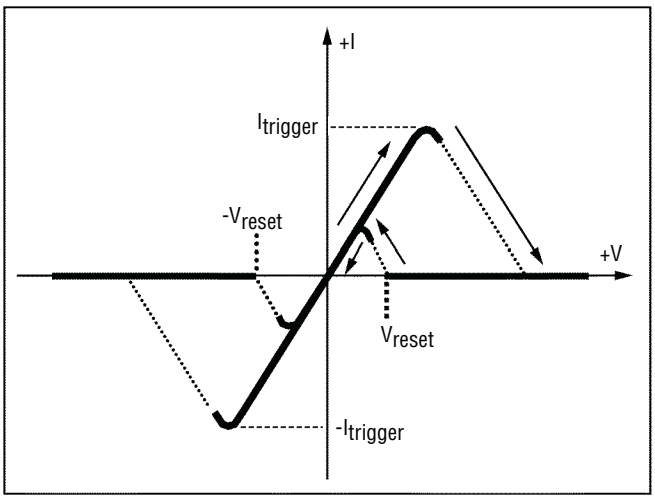
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{op}	Maximum current through the device that will not cause current blocking			240	mA
$I_{trigger}$	Typical current for the device to go from normal operating state to protected state		350		mA
I_{out}	Maximum current through the device			480	mA
R_{TBU}	Series resistance of the TBU™ device		3.6	4.2	Ω
R_{bal}	Line-to line series resistance difference between two TBU™ devices			5	%
t_{block}	Maximum time for the device to go from normal operating state to protected state			0.2	µs
$I_{quiescent}$	Current through the triggered TBU™ device with 40 Vdc circuit voltage		0.7		mA
V_{reset}	Voltage below which the triggered TBU™ device will transition to normal operating state		7		V

The P40-G Series TBU™ device is bidirectional; specifications are valid in both directions.

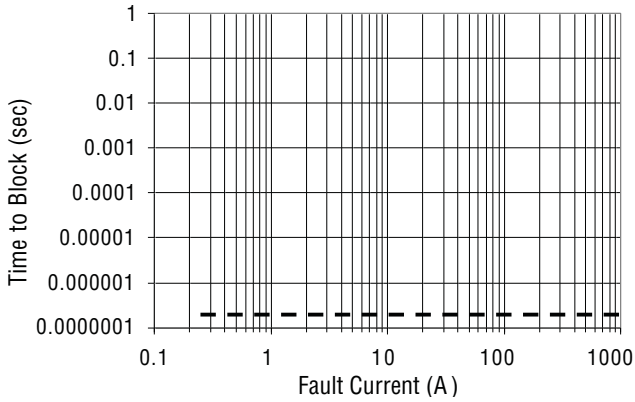
*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Typical Performance Characteristics

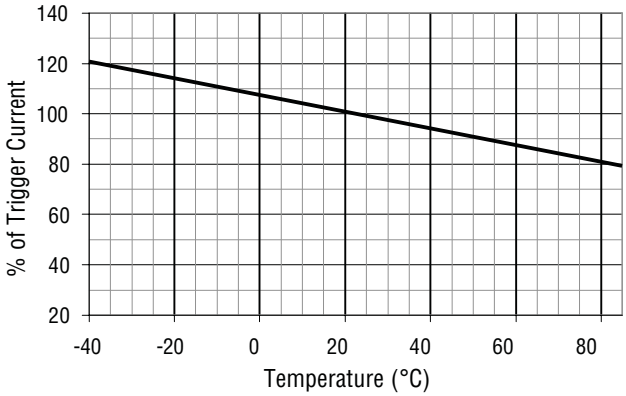
V-I Characteristics



Time to Block vs. Fault Current



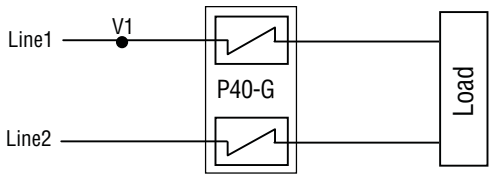
Trigger Current vs. Temperature



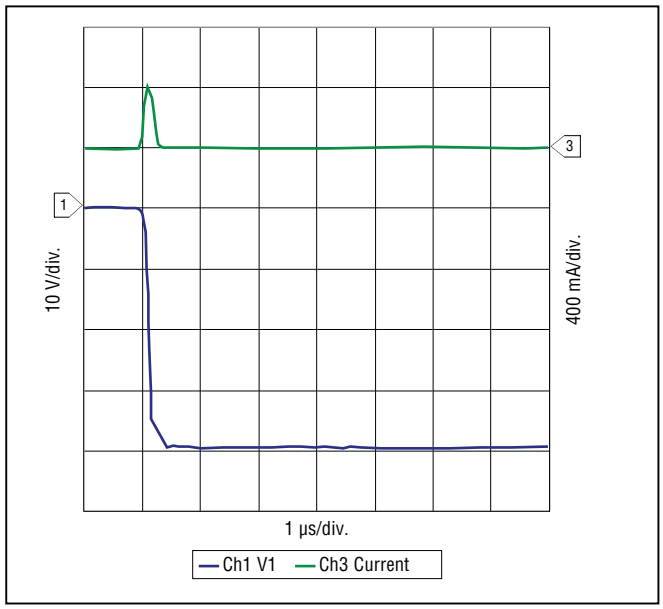
Operational Characteristics

The graph below demonstrates the operational characteristics of the TBU™ device. In the graph below the fault voltage, protected side voltage, and current is presented.

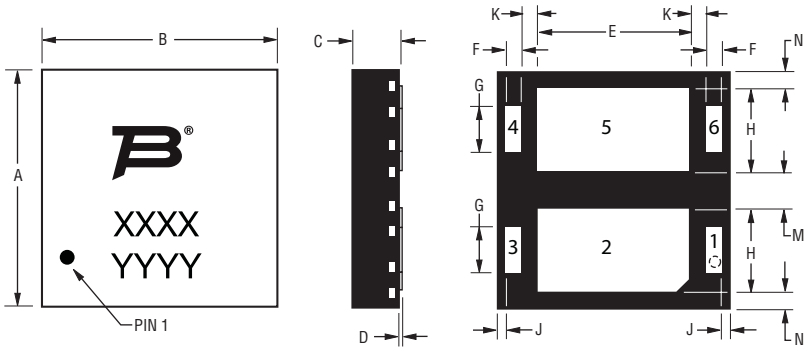
TEST CONFIGURATION DIAGRAM



P40-G Lightning Protection 40 V



Product Dimensions

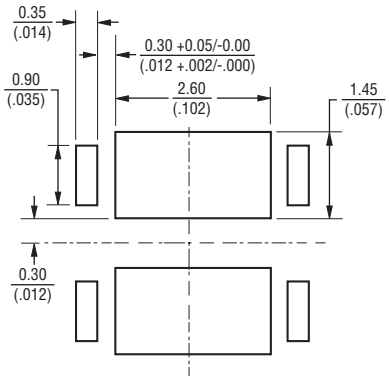


TOP VIEW SIDE VIEW BOTTOM VIEW

Dim.	Min.	Typ.	Max.
A	3.90 (.154)	4.00 (.157)	4.10 (.161)
B	3.90 (.154)	4.00 (.157)	4.10 (.161)
C	0.80 (.031)	0.85 (.033)	0.90 (.035)
D	0.000 (.000)	0.025 (.001)	0.050 (.002)
E	2.55 (.100)	2.60 (.102)	2.65 (.104)
F	0.20 (.008)	0.25 (.010)	0.30 (.012)
G	0.75 (.030)	0.80 (.031)	0.85 (.033)
H	1.40 (.055)	1.45 (.057)	1.50 (.059)
J	0.10 (.004)	0.15 (.006)	0.20 (.008)
K	0.25 (.010)	0.30 (.012)	0.35 (.014)
M	0.55 (.022)	0.60 (.024)	0.65 (.026)
N	0.20 (.008)	0.25 (.010)	0.30 (.012)

DIMENSIONS: MM (INCHES)

Recommended Pad Layout



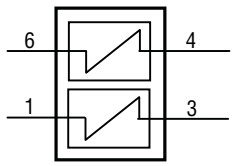
Pad Designation

Pad #	Apply
1	In1
2	NC
3	Out1
4	Out2
5	NC
6	In2

NC = Solder to PCB; do not make electrical connection, do not connect to ground.

TBU™ devices have matte-tin termination finish. Suggested layout should use non-solder mask define (NSMD). Recommended stencil thickness is 0.10-0.12 mm (.004-.005 in.) with stencil opening size 0.025 mm (.0010 in.) less than the device pad size. As when heat sinking any power device, it is recommended that, wherever possible, extra PCB copper area is allowed. For minimum parasitic capacitance, do not allow any signal, ground or power signals beneath any of the pads of the device.

Block Diagram



TBU™ Device

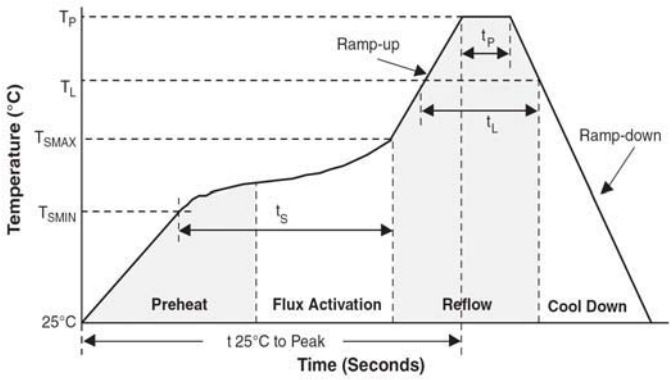
Thermal Resistances

Thermal resistance using minimal pad size, where the power is the total power dissipated in the package. Additional copper pad area to be used for additional heatsinking is also recommended.

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to Package Pads (1 TBU of Pair)	250	°C/W
$R_{th(j-a)}$	Junction to Package Pads (2 TBUs of Equal Power)	180	°C/W

Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp-Up Rate (Tsmax to Tp)	3 °C/sec. max.
Preheat - Temperature Min. (Tsmin) - Temperature Max. (Tsmax) - Time (tsmin to tsmax)	 150 °C 200 °C 60-180 sec.
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 sec.
Peak/Classification Temperature (Tp)	260 °C
Time within 5 °C of Actual Peak Temp. (tp)	20-40 sec.
Ramp-Down Rate	6 °C/sec. max.
Time 25 °C to Peak Temperature	8 min. max.



How to Order

P 40 - G 240 - WH

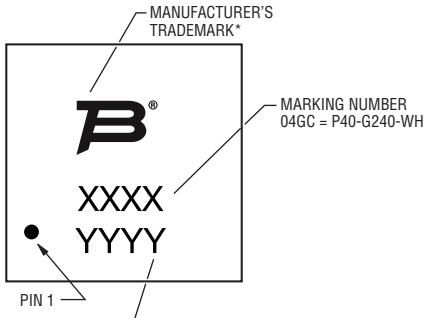
Form Factor
P = Two TBU™ protectors in one device

Impulse Voltage Rating
40 = 40 V

Directional Indication
G = Bidirectional

Iop Indicator
240 = 240 mA

Typical Part Marking



- 1ST DIGIT INDICATES THE YEAR'S 6-MONTH PERIOD.
- 2ND DIGIT INDICATES THE WEEK NUMBER IN THE 6-MONTH PERIOD.
- 3RD & 4TH DIGITS INDICATE SPECIFIC LOT FOR THE WEEK.

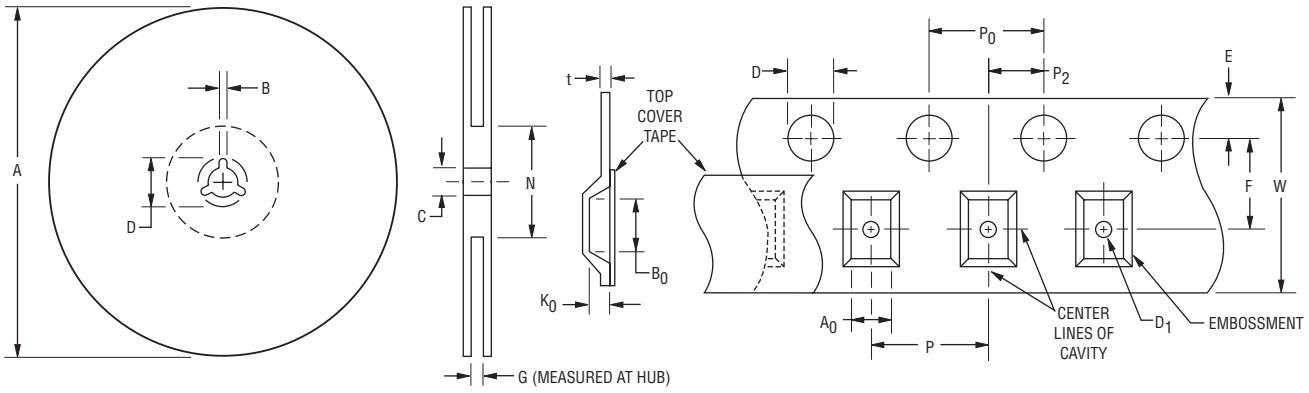
6-MONTH PERIOD CODES:

A = JAN-JUN 2009	C = JAN-JUN 2010	E = JAN-JUN 2011
B = JUL-DEC 2009	D = JUL-DEC 2010	F = JUL-DEC 2011

EXAMPLE: ARBC
- *1ST DIGIT 'A' = JAN-JUN 2009*
- *2ND DIGIT 'R' = WEEK 18; WEEK OF APRIL 27*
- *3RD & 4TH DIGITS 'BC' = LOT SPECIFIC INFORMATION*

*TRANSITION FROM FULTEC TRADEMARK AND LOT CODE TO BOURNS TRADEMARK AND DATE CODE IN 2009.

Packaging Specifications (per EIA468-B)



QUANTITY: 3000 PIECES PER REEL

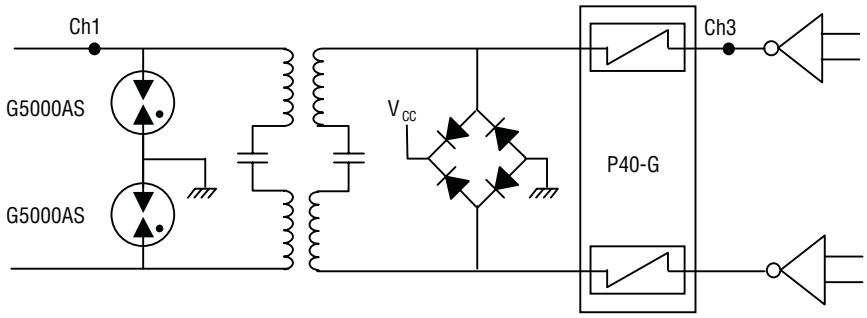
Device	A		B		C		D		G	N
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Ref.	Ref.
P40-G240	326 (12.835)	330.25 (13.002)	1.5 (.059)	2.5 (.098)	12.8 (.504)	13.5 (.531)	20.2 (.795)	-	12.4 (.488)	102 (4.016)

Device	A_0		B_0		D		D_1		E		F	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	max.
P40-G240	4.2 (.165)	4.4 (.173)	4.2 (.165)	4.4 (.173)	1.5 (.059)	1.6 (.063)	1.5 (.059)	-	1.65 (.065)	1.85 (.073)	5.45 (.216)	5.55 (.219)
Device	**K_0**		**P**		**P_0**		**P_2**		**t**		**W**	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
P40-G240	1.05 (.041)	1.25 (.049)	7.9 (.311)	8.1 (.319)	3.9 (.159)	4.1 (.161)	1.9 (.075)	2.1 (.083)	0.25 (.010)	0.35 (.014)	11.7 (.461)	12.3 (.484)

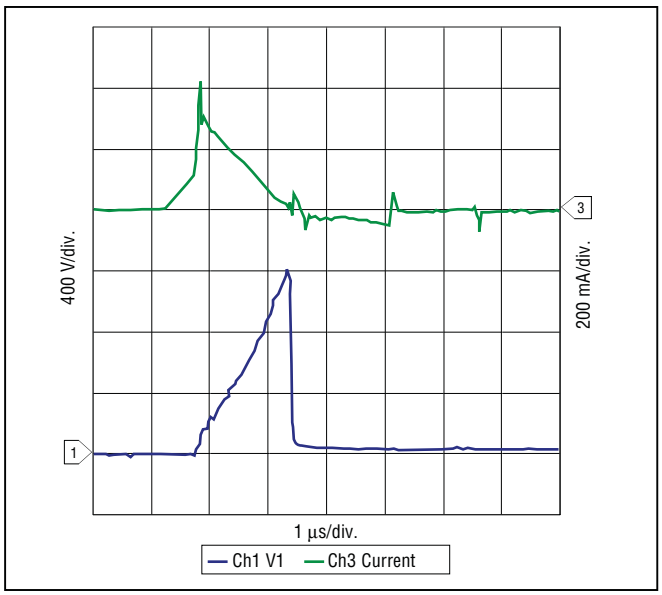
DIMENSIONS: MM (INCHES)

Reference Application

A cost-effective protection solution combines the Bourns® TBU™ protection device with a diode bridge on the driver side of the transformer and Bourns® GDTs on the line side. The diagram below illustrates a common configuration of these components. The graph demonstrates the operational characteristics of the circuit.



Common Configuration Diagram - xDSL Protection



5000 V Lightning 2/10 µsec, 500 A

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