PowerPC™

IBM

PowerPC 401GF
Embedded Controller

Highlights

401 Core
- *Compatible with PowerPC User Instruction Set Architecture*
- *32-bit x 32 general purpose registers*
- *Hardware multiply and divide*
- *Unaligned load/store*

Bus Controller
- *Multiplexed address/data bus*
- *Programmable read/write burst*
- *Target word first capability*
- *Bus clock out*
- *Support for 8-, 16- and 32- bit devices*
- *External bus master support*
- *JTAG port for Test/Debug (IEEE 1149.1)*

Real Mode MMU
- *Programmable cacheability*
- *Programmable copy-back/write-thru*
- *True Little-Endian operation*

Timers
- *64-bit time-base*
- *Programmable interval timer*
- *Fixed interval timer*
- *Watchdog timer*

Cache Controllers
- *Separate I and D cache controllers*
- *Critical data forwarding*
- *Fill first handling of cache misses*
- *Non-blocking flush operations*
- *Store queue*
- *2K I and 1K D cache arrays*
- *Array Built In Self Test (ABIST)*

Power Management
- *Custom circuitry to minimize power*
- *Hardware-based dynamic clocking*
- *On-chip oscillator*
- *Software-controlled sleep modes*

Product Overview

The PowerPC 401GF* is a member of IBM's growing family of 32-bit RISC embedded controllers. The 401GF design, based on the PowerPC 401 Core, provides a high level of value to system developers in communications, consumer and printer markets — especially developers who measure value based on price, performance and power consumption.

Like all PowerPC* embedded controllers, the 401GF supports the PowerPC User Instruction Set Architecture. This means there's a new price/performance leader in our extended family of embedded processors. A family that offers unprecedented processor scalability, as well as portability across the product line to protect your investment in code.

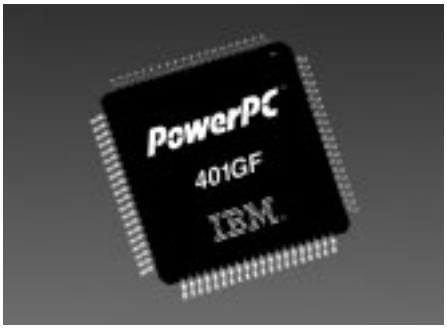
IBM's leading edge embedded controller technology allows us to pack a lot of functionality into this tiny package. And your implementation of this technology will prove that cost effectiveness does not come at the expense of performance or power.

A three-stage execution pipeline, combined with barrel rotator, operand forwarding and branch prediction logic, allows the 401GF to maintain the high level of performance inherent in all PowerPC processors. At 50 MHz, the 401 benchmarks at 92 K Dhrystones/sec (53 Dhrystone MIPS).

Additionally, the 401GF I/O bus provides an easy interface to system peripherals. The simple bus interface enables the best performance from the CPU while allowing you to design peripherals and memory control logic.

If low power consumption is important in your application, consider having 401GF performance powered by an operating voltage of 3.3 volts. With IBM's unique power management logic, active power consumption is 200 mW at 50 MHz and 3.3 V. Sleep-mode power is as low as 520 µW.

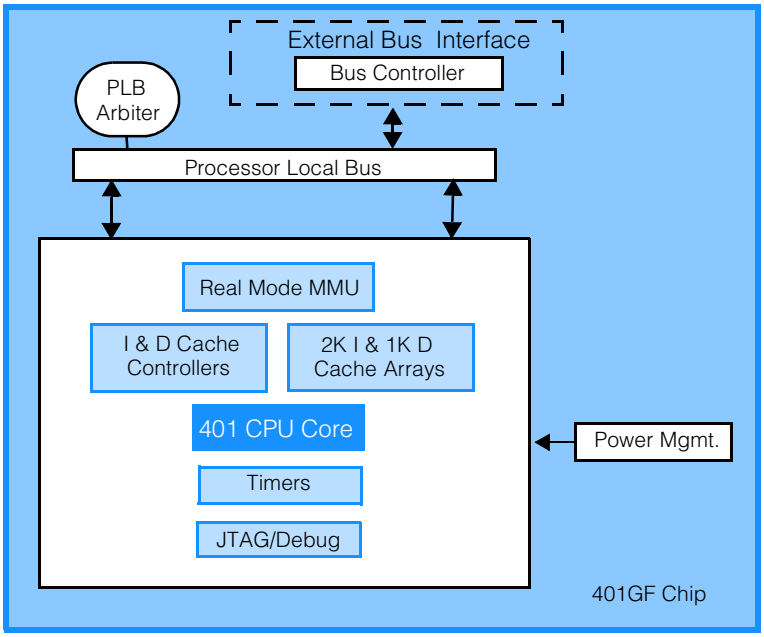
Choosing the PowerPC 401GF as your processor platform ensures the support of IBM and over 75 select third-party vendors in the PowerPC Embedded Tools* Program. This program offers a full range of embedded development tools, including compilers, debuggers, real-time operating systems, emulators, logic analyzers, and evaluation boards.



PowerPC 401GF Specifications

Technology	0.5 µm CMOS, three levels of metal
Core Size	4.5 mm^2
Frequency (CPU : I/O)	2:1
Performance:	
50 MHz	92 K Dhrystones/sec., 53 DMIPS
Voltage Requirements	
50 MHz	3.3 V ±5% (supports 5V I/Os)
Power Dissipation (Est.)	
50 MHz at 3.3V	
Average Power	200 mW
Wait	40 mW
Doze	30 mW
Nap	5 mW
Deep Sleep	520 µW
Max Case Temp. Range	0° C to +85° C
Packaging	80-Pin TQFP, 63 signal I/Os

To see why more and more engineers and integrators are choosing IBM for their processor platform solutions, call your nearest IBM Microelectronics office, or contact us on the World-Wide Web.



PowerPC 401GF Block Diagram

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