

深圳思玛自动化控制有限公司

*SHenzhen SMAR Industrial Automation*

## SM HT2015 Hart 调制解调器 (Modem)

# 中英文技术资料说明书

[SM HT2015 (32 脚 LQFP 和 28 脚 PLCC) 都满足 RoHS 环保标准。该芯片管脚与 HT2015/SYM20C15 或 A5191HRT 完全兼容,可直接替代无需修改外围电路,也无需改动 PCB 板。当替代 HT2015/SYM20C15 时无需修改任何参数,替代 A5191HRT 时只需修改一个电阻值。]

## 1.0 特点(Features)

- ★ 符合 HART 通信协议物理层要求。
- ★ 可与 HT2015、A5191HRT SYM20C15 完全兼容。
- ★ 功耗低。
- ★ 误码率典型值小于百万分之一。
- ★ 工作电压 3.0V~5.5V。
- ★ 单芯片、半双工 1200b/s 的 FSK 调制解调器。
- ★ 符合 Bell202 标准，载波为 1200Hz 和 2200Hz。
- ★ 内部集成接收滤波器,以及输出 HART 波形整形电路。
- ★ 可外接 460.8kHz 晶体或陶瓷谐振器或使用外部时钟源。
- ★ 工业级工作温度:-40℃~+85℃
- ★ 32 脚 LQFP 封装和 28PLCC 封装。
- ★ 满足 RoHS 环保要求。



SM HT2015 使用相位连续的频移键控 (FSK) 调制解调技术，传输速率为 1200 位/秒，采用半双工通信，符合 HART 协议物理层要求。芯片的典型电流值在 5V 电压时 150  $\mu$  A，3.3V 时 110  $\mu$  A，低于现有的其他 HART 芯片。误码率典型值小于百万分之一，是 HART 协议要求的百分之一。

SM HT2015 (32 脚 LQFP) 都满足 RoHS 环保标准。该芯片管脚与 HT2015/SYM20C15 或 A5191HRT 完全兼容，可直接替代无需修改外围电路，也无需改动 PCB 板。当替代 HT2015/SYM20C15 时无需修改任何参数，替代 A5191HRT 时只需修改一个电阻值 (图 8 的 R6)。

## 2.0 产品描述 (General Description)

SM HT2015 是专为实现 HART 协议而设计的 CMOS 单芯片调制解调器，用于支持 HART 协议的现场仪表和控制器中。芯片只需外加少量无源元件，即可满足 HART 物理层规范功能要求，包括调制与解调，输入信号滤波，载波检测和发送信号波形整形等。详细资料请看管脚描述与功能描述。

## 3.0 订购信息

SM HT2015 是 32 脚 LQFP 封装和 28 脚 PLCC 封装，请根据表 1 进行订购。

表 1:订购信息

封装形式	订货名称	品牌
LQFP-32P	HT2015-LQ	SM (思玛)
PLCC-28P	HT2015-PL	SM (思玛)

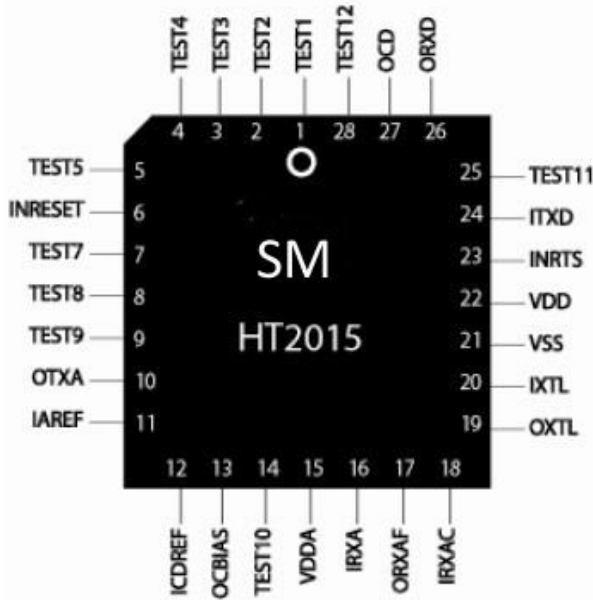


Fig. 1 - 28 pin PLCC Pinout Package

图 1. LQFP32 封装管脚图

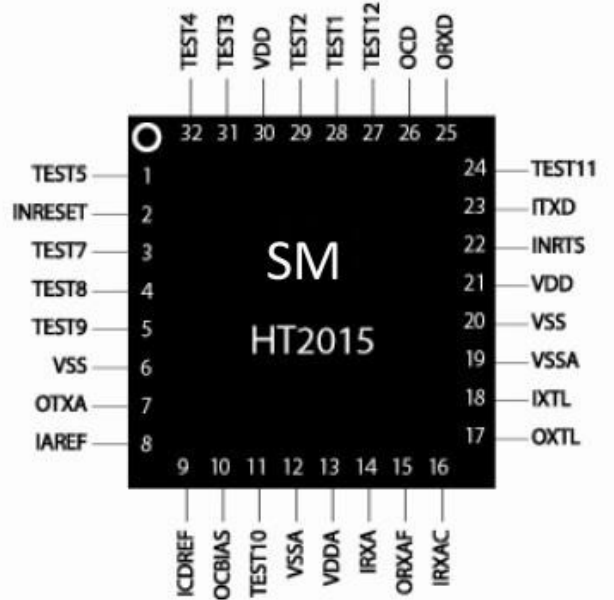


Fig. 2 - 32 pin LQFP Pinout Package

PLCC28 封装管脚图

4.0 管脚描述 表 2:端口描述 (Pin Descriptions)

管脚名称 Signal	属性 Type	管脚号		描述 Description
		LQFP	PLCC	
TEST5	—	1	5	悬空或连接到 VSS (Connect to Vss.)
INRESET	输入 (Input)	2	6	低电平有效, 复位所有数字逻辑 (Reset all digital logic when low)
TEST7	输入 (Input)	3	7	连接到 VSS (Connect to Vss.)
TEST8	输入 (Input)	4	8	连接到 VSS (Connect to Vss.)
TEST9	输入 (Input)	5	9	连接到 VSS (Connect to Vss.)
VSS	地 (Ground.)	6		接地 (Ground.)
OTXA	输出 (Output)	7	10	模拟输出脚, 发送符合 HART 规范的 FSK 调制信号, 信号发送到 4-20 毫安电流回路接口 (Modulated output transmit analog. FSK modulated HART transmit signal to 4-20mA loop interface circuit.)
IAREF	输入 (Input)	8	11	模拟参考电压 (Analog reference voltage.)
ICDREF	输入 (Input)	9	12	载波检测参考电压 (Carrier detect reference voltage.)
OCBIAS	输出 (Output)	10	13	输出脚, 设置偏置电流 (Comparator bias current.)

TEST10	— (Input)	11	14	悬空或连接到 VSS (Connect to Vss.)
VSSA	地	12		模拟地 (Analog ground.)
VDDA	电源 (Power)	13	15	模拟电源 (Analog supply voltage.)
IRXA	输入 (Input)	14	16	模拟输入脚, 接收符合 HART 规范的 FSK 调制信号, 信号来自 4-20 毫安电流环回路端口 (FSK modulated HART receive signal from 4-20mA loop interface circuit. .)
ORXAF	输出 (Output)	15	17	模拟端口, 接收滤波器输出 (Analog receiver filter input.)
IRXAC	输入 (Input)	16	18	模拟端口, 接收比较器输入 (Analog receive comparator input.)
OXTL	输出 (Output)	17	19	晶体振荡器输出 (Crystal oscillator output.)
IXTL	输入 (Input)	18	20	晶体振荡器输入 (Crystal oscillator input.)
VSSA	地	19		模拟地 (Analog ground.)
VSS	地	20	21	接地 (Ground.)
VDD	电源	21	22	数字电源 (Digital supply voltage.)
INRTS	输入 (Input)	22	23	发送请求, 低电平有效 (Request to send.)
ITXD	输入 (Input)	23	24	输入来自 UART 的待发送数据串, 经 OTXA 调制发送 (Input transmit data. Transmitted HART data stream from UART.)
TEST11	—	24	25	悬空 (No connect.)
ORXD	输出 (Output)	25	26	接收解调后的 HART 数据, 送到 UART 口 (Received demodulated HART data to UART.)
OCD	输出 (Output)	26	27	载波检测输出, IRXA 有效时高电平 (Carrier detect output.)
TEST12	— (Input)	27	28	悬空 (No connect.)
TEST1	— (Input)	28	1	悬空或连接到 VSS (Connect to Vss.)
TEST2	— (Input)	29	2	悬空 (No connect.)
VDD	电源 (Power)	30		数字电源 (Digital supply voltage.)
TEST3	— (Input)	31	3	悬空 (No connect.)
TEST4	— (Input)	32	4	悬空 (No connect.)

## 端口描述

- IAREF: 模拟参考电压  
设置电路内部放大器和比较器的静态直流工作点, 根据表 4 选择适当的电压值。
- ICDREF: 载波检测电压 (   
根据 IAREF 与 ICDREF 的差值控制载波检测的阈值, 只有大于该阈值的信号才能使 OCD 使能,  $V^* IAREF - V ICDREF = 80mV$  时, 载波检测阈值为  $100mV_{p-p}$ 。
- INRESET: 数字逻辑复位信号  
低电平时复位数字逻辑, 正常工作下保持高电平。上电过程中, 在 VDD 大于 2.5V 后, INRESET 必须继续保持低电平大于 10ns, 如图 3。

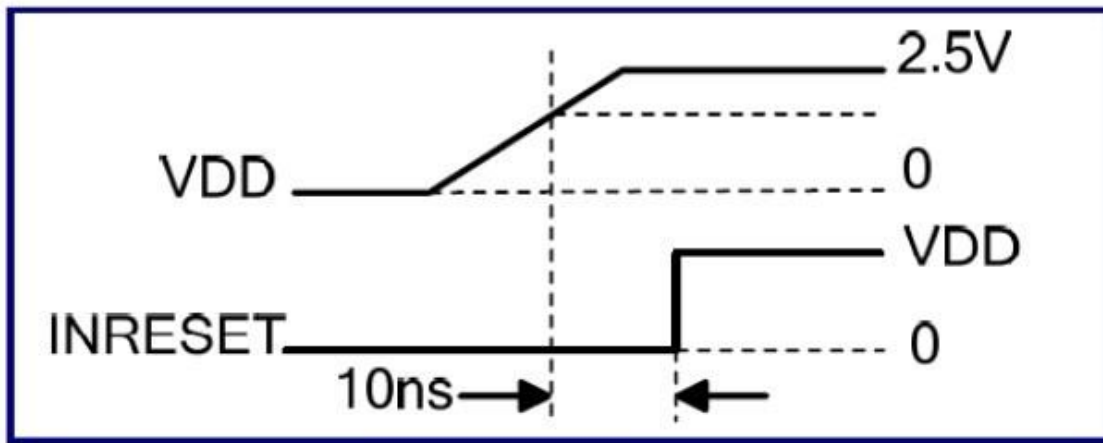


图3 复位时序图

- **INRTS:**发送请求  
低电平有效。高电平时，芯片处于接收解调状态，OTXA 无信号输出并保持在梯形波的中心电平上；当 INRTS 变为低电平时，芯片开始进入调制状态，OTXA 开始输出梯形波信号。在上电时，该管脚应保持高电平。
- **IRXA:** 接收端的模拟信号输入  
接收叠加在 4-20mA 电流回路上的 1200/2200Hz 载波信号，详见图 8。
- **IRXAC:** 模拟接收比较器输入  
连接到载波检测比较器和接收滤波比较器正输入端。
- **ITXD:**发送数据的输入  
调制器输入端，接收输入的不归零制（NRZ）数字信号。当 ITXD 低电平（逻辑 0）时，OTXA 管脚输出 2200Hz 梯形波信号；ITXD 高电平（逻辑 1）时，OTXA 管脚输出 1200Hz 梯形波信号。
- **IXTL:** 振荡器输入  
振荡器的输入端，在使用内部振荡电路时外接 460.8kHz 的晶振或陶瓷谐振器，在外接时钟时该管脚直接接地，如图 9 与图 10 所示。
- **OCBIAS:** 电路偏置电流  
经过该管脚的电流用于设定内部模块的参数。  
通常情况下，OCBIAS 电流（记为  $I_{OCBIAS}$ ）设定为  $2.5 \mu A$ 。
- **OCD:** 载波检测输出  
接收滤波器输入端接收到一个有效输入并保持连续四个周期后，OCD 变高。有效输入指其电平峰值大于由 IAREF 和 ICDREF 设定的阈值。
- **ORXAF:** 模拟接收滤波器输出  
接收端的高通滤波器的放大输出，见图 8。

- ORXD: 数字接收输出 (CMOS)

输出解调后的数字信号。当接收信号是 1200Hz 正弦波时, ORXD 输出高电平, 当接收信号是 2200Hz 正弦波时, ORXD 输出低电平。ORXD 有效与否取决于 OCD; 当 OCD 是低电平时, ORXD 保持高电平 (此时为无效信号)。

- OTXA: 模拟传输输出

该管脚输出调制后的梯形波, 在 INRTS 为低电平且 ITXD 为低电平时, 输出信号频率 2200Hz; 在 INRTS 为低电平且 ITXD 为高电平时, 输出信号频率为 1200Hz。

- OXTL: 振荡器输出

管脚接到外部 460.8kHz 时钟源或者 460.8 kHz 晶振或陶瓷谐振器。

- TEST(1: 12): 测试接口

- VDD: 数字电源

- VDDA: 模拟电源

- VSS: 接地

32 管脚 LQFP 数字地, 28 管脚 PLCC 的模拟和数字地

- VSSA: 模拟地

VIAREF 指 IAREF 管脚的电压值; VICDREF 指 ICDREF 管脚的电压值

## 5.0 功能描述

SM HT2015 与 HT2015、SYM20C15、A5191HRT 的功能完全相同。该芯片包含一个发送数据的调制器和波形整形器、模拟接收滤波器和解调器、载波检测电路、振荡器, 功能框图如图 4 所示。

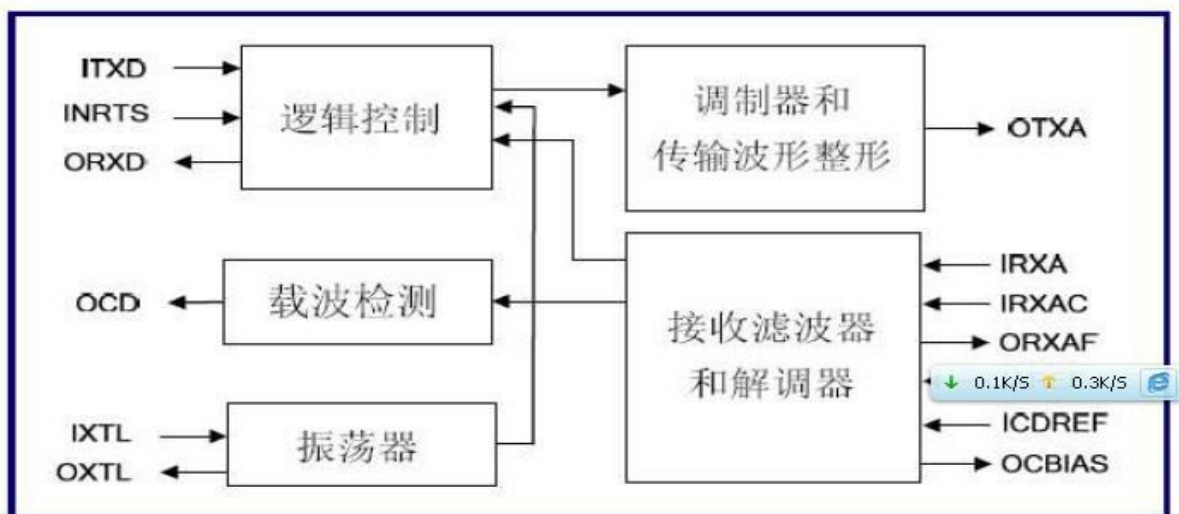


图 4 HT2015 内部结构图



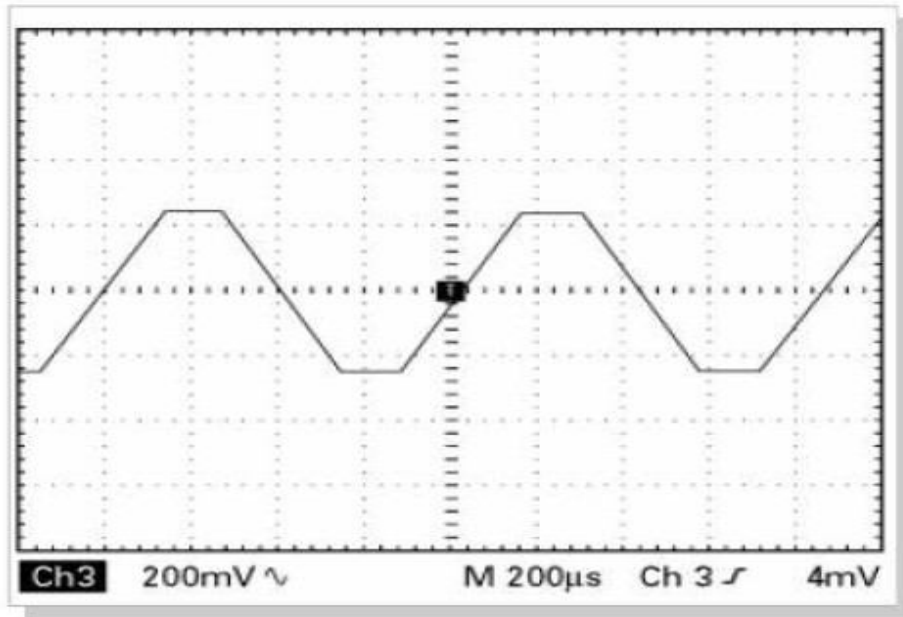


图5 OTXA 波形逻辑1 (1200HZ)

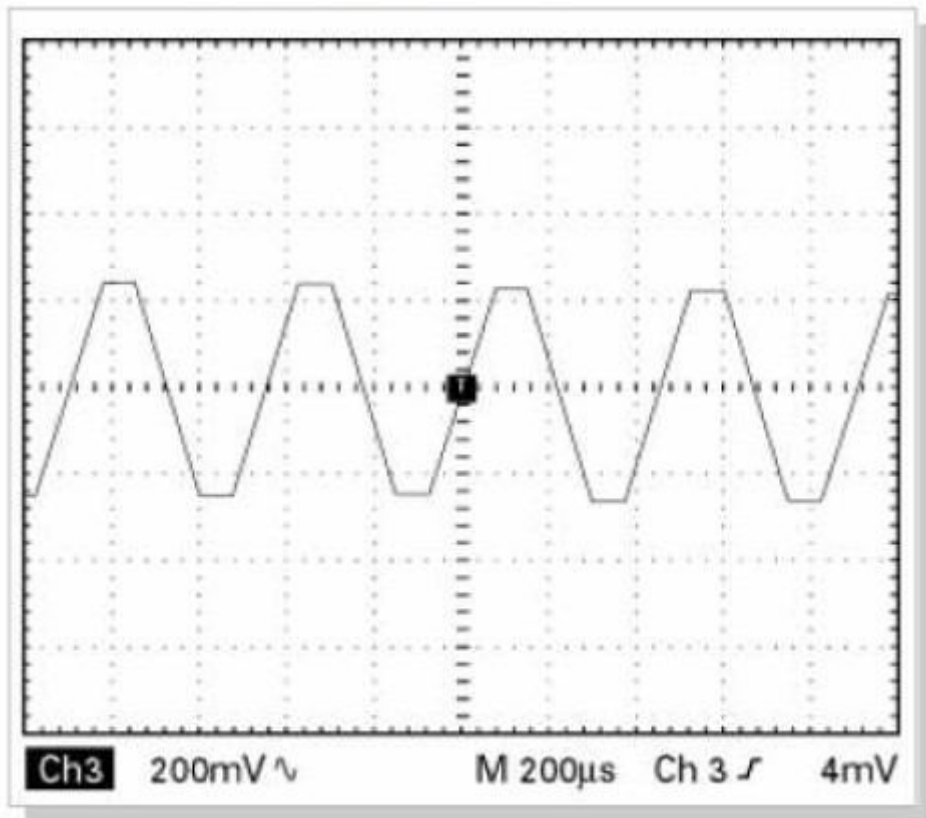


图6 OTXA波形逻辑0 (2200HZ)

调制解调器调制发送信号、解调接收信号，信号波形整形电路对发送信号进行波形整形，使之符合 HART 规范。载波检测电路将把接收滤波器输出和两个外部参考电压  $V_{IAREF}$  与  $V_{ICDREF}$  之间的差值进行比较，以确定载波是否出现。模拟接收电路对接收信号进行带通滤波，然后输入解调电路和载波检测电路。振荡电路通过外接一个谐振器或时钟源，给整个该电路提供时钟基准。

该调制电路使用 FSK 调制方式（1200Hz 为 1，2200Hz 为 0），比特率 1200 位/秒。

### 5.1 调制器和传输波形整形

调制器在 ITXD 管脚接收非归零制 (NRZ) 的数字信号，进行调制并经波形整形电路整形后在 OTXA 管脚输出符合 HART 协议要求的 FSK 调制信号，如图 5 与图 6 所示。INRTS 管脚必须保持低电平才能保证调制器的正常工作。

当  $V_{IAREF}=1.235V$  DC 时,OTXA 将有一个 0.25~0.75 V 的电压摆幅,  $V_{IAREF}=2.5VDC$  OTXA 将有一个 0.5~1.5V 的电压摆幅。

解调器输出受控于载波检测输出(OCD)

### 5.2 解调器和载波检测

解调器在 IRXA 接收 FSK 信号，经解调后在 ORXD 脚输出基带数字信号，比特率为 1200bps，解调器的解调过程如图 7 所示。

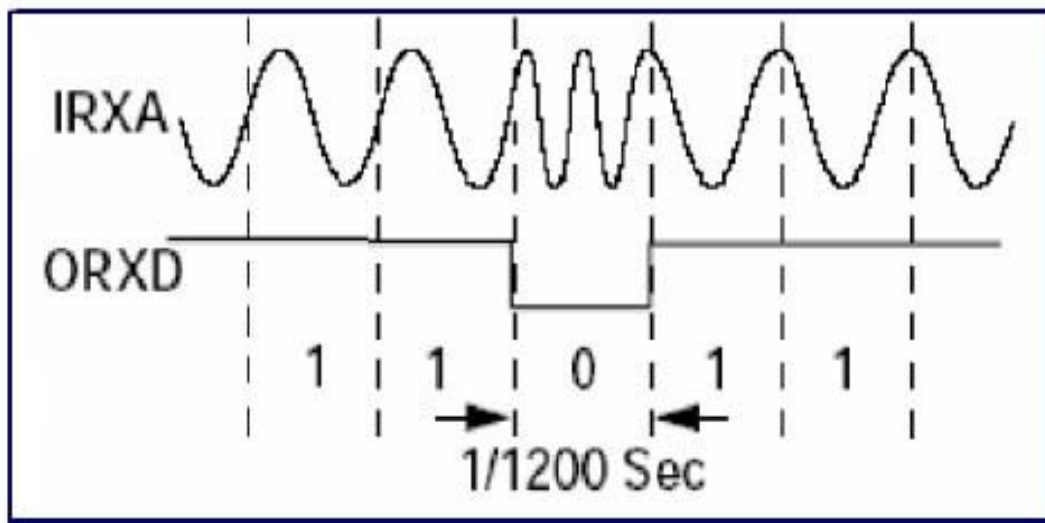


图 7 信号解调时序图

解调器输出受控于载波检测输出 (OCD)，只有当接收滤波器输入信号大于一定值(典型值为 100mV<sub>p-p</sub>)，被载波检测电路判定为有效后，才会在 ORXD 口输出接收到的数据。根据 HART 协议，在时钟频率为 460.8kHz(±1.0%)，IRXA 输入波形对称的条件下，最大解调抖动不会超过 ORXD 输出码率一个位元宽度的 12%\*

信号经过载波检测比较器和载波检测模块，在 OCD 脚输出载波检测结果（见图 4 和图 8）。当 INRTS 高电平并且载波检测比较器输出四个连续的脉冲后，OCD 变成高电平。只有 INRTS 保持在高





在 HT2015 的内部，有一个截止频率为 35Hz 高通滤波器，一个截止频率为 109Hz 的低通滤波器，低通滤波极点有  $\pm 30\%$  的摆幅。滤波器的输入阻抗在频率低于 50Hz 时大于  $6.7\text{M}\Omega$ 。

## 5.4 振荡器

HT2015 在 OXTL 上需要一个 460.8kHz 的时钟信号，可以通过外接外部时钟或振荡器获得。

### 5.4.1 内部振荡器

内部振荡器单元可以外接 460.8kHz 的晶体或陶瓷谐振器，见图 9。

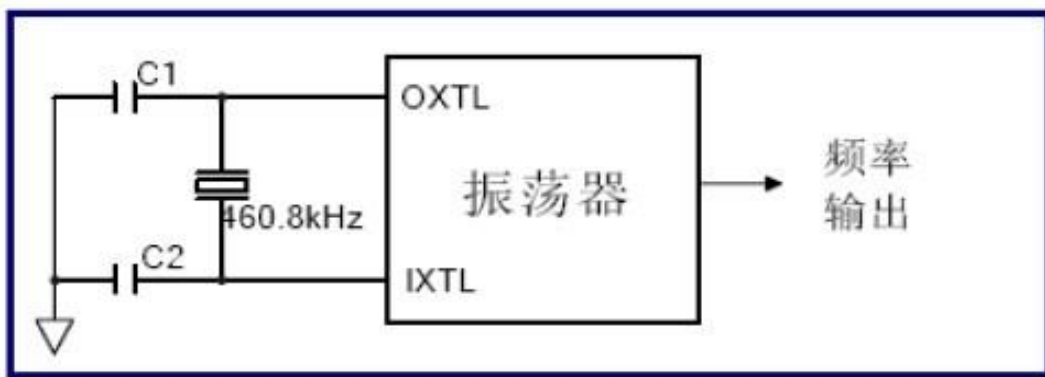


图 9 晶体振荡器

谐振器频率为 460.8kHz ( $\pm 1\%$  误差范围)。电容器 C1、C2 值的选择取决于谐振器制造商的建议，但 C1、C2 值应该相同，通常在 33pF 到 470pF 之间。

### 5.4.2 外部时钟

图 10 为一个选用 460.8kHz 外部时钟的电路示意图，此时 IXTL 必须接地。

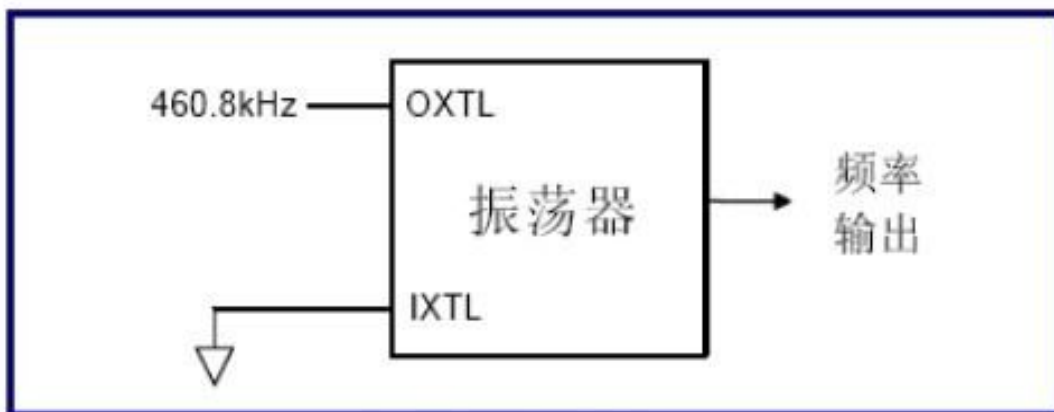


图 10 外部时钟输入

## 6.0 电气特性

表3. 最大绝对值

标识	参数	最小值	最大值	单位
$T_A$	环境温度	-40	+85	°C
$T_S$	储存温度	-55	+150	°C
$V_{DD}$	供电电压	-0.3	+6.0	V
$V_{IN}, V_{OUT}$	直流输入、输出	-0.3	$V_{DD}+0.3$	V
$T_L$	回流焊温度曲线		Per IPC/JEDECJ-STD-020C	°C

表4. 直流特性

( $V_{DD}$  = 3.0V到5.5V,  $V_{SS}$  = 0V,  $T_A$  = -40°C到+85°C)

标识	参数	VDD	最小值	典型值	最大值	单位
$V_{IL}$	输入低电平, 逻辑0	3.0-5.5			$0.3*V_{DD}$	V
$V_{IH}$	输入高电平, 逻辑1	3.0-5.5	$0.7*V_{DD}$			V
$V_{OL}$	输出数字低电平 ( $I_{OL}=0.67mA$ )	3.0-5.5			0.4	V
$V_{OH}$	输出数字高电平 ( $I_{OH}=0.67mA$ )	3.0-5.5	$V_{DD}-0.6$			V
$C_{IN}$	输入管脚电容					pF
	模拟输入管脚			2.9		
	IRXA			25		
	数字输入管脚			3.5		
$I_{IL/IH}$	输入管脚的漏电流				$\pm 500$	nA
$I_{OLL}$	输出管脚的漏电流				$\pm 10$	$\mu A$
$I_{DD}$	电源电流	3.3	--	110	120	$\mu A$
		5.0	--	150	170	
$V_{IAREF}$	模拟参考电压	3.3	1.2	1.235	1.26	V
		5.0		2.5		
$V_{ICDREF}^*$	载波检测参考电压 ( $V_{IAREF}-0.08V$ )	3.3		1.155		V
		5.0		2.420		
$I_{OCBIAS}$	偏置电流 ( $R_{BIAS}=500k\Omega$ , $I_{AREF} = 1.235V$ 或 $R_{BIAS}=1M\Omega$ , $I_{AREF} = 2.5V$ )			2.5		$\mu A$

表5. 交流特性

( $V_{DD}$  = 3.0V到5.5V,  $V_{SS}$  = 0V,  $T_A$  = -40°C到+85°C)

管脚名称	描述	最小值	典型值	最大值	单位
IRXA	模拟接收器输入				
	漏电流			±150	nA
	频率-逻辑1	1190	1200	1210	Hz
	频率-逻辑0	2180	2200	2220	Hz
ORXAF	模拟接收滤波器的高通滤波器输出				
	转换速率 (SR)		0.025		V/μs
	增益带宽 (GBW)	500			kHz
	电压范围	0.1		V <sub>DD</sub> -0.15	V
IRXAC	模拟接收滤波器与载波检测比较器输入				
	漏电流			±500	nA
OTXA*	模拟调制器输出				
	频率-逻辑1		1200		Hz
	频率-逻辑0		2200		Hz
	振幅 (IAREF 1.235V)		500		mV <sub>P-P</sub>
	振幅 (IAREF 2.5V)		1000		mV <sub>P-P</sub>
	上升/下降速率 负载	30	2.79		mV/μs kΩ
	输出管脚非有效状态电平(INRTS高电平) VDD=3.3V		0.5		V
	输出管脚非有效状态电平(INRTS高电平) VDD=5V		1		V
ORXD	数字接收输出				
	上升/下降时间	20			ns
OCD	载波检测输出				
	上升/下降时间	20			ns

表6. 调制解调器特性

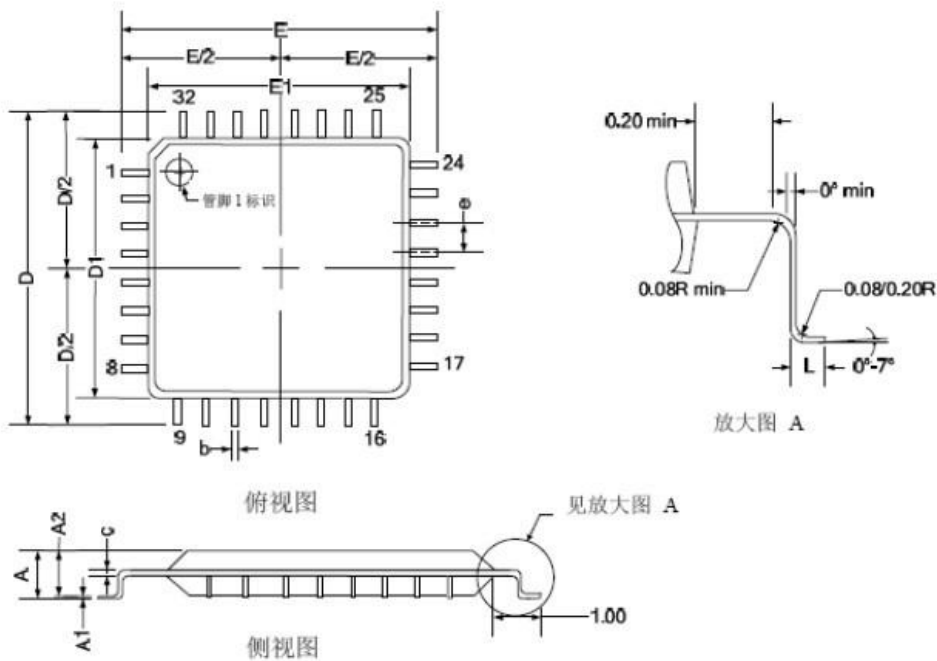
(V<sub>DD</sub> = 3.0V到5.5V, VSS = 0V, T<sub>A</sub> = -40°C到+85°C)

参数	最大值	单位
解调抖动	12	% of 1 bit*
条件:		
1. 输入频率在1200Hz ± 10Hz, 2200Hz ± 20Hz		
2. 时钟频率460.8kHz ± 0.1%		
3. IRXA输入信号对称		
*1bit是指ORXD输出码率的一个位元, 在时钟频率为460.8kHz时, 1bit为1/1200秒。		

( $V_{DD} = 3.0V$ 到 $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$ 到 $+85^{\circ}C$ )

参数	最小值	典型值	最大值	单位
谐振器				
容差			$\pm 1.0$	%
频率	460.8			kHz
外部时钟				
时钟频率	456.2	460.8	465.4	kHz
占空比	40	50	60	%
振幅		$V_{OH}-V_{OL}$		V

### 7.0 封装规格

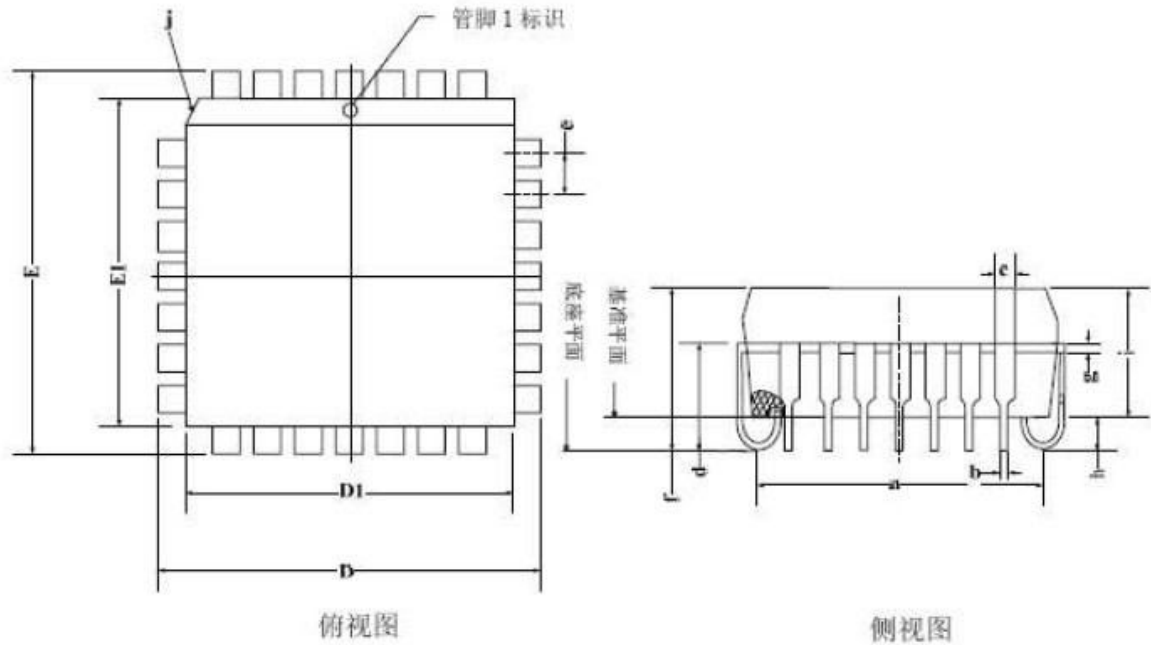


尺寸: 毫米

标记	最小值	典型值	最大值
A	-	-	1.6
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D		9.00	
D/2		4.50	
D1		7.00	
E		9.00	
E/2		4.50	
E1		7.00	
L	0.45	0.60	0.75
e		0.80	
b	0.30	0.37	0.45







尺寸: 英寸(毫米)

标记	最小值	典型值	最大值
E	0.4850 (12.320)	-	0.4950 (12.574)
E1	0.4500 (11.430)	-	0.4560 (11.582)
D	0.4850 (12.320)	-	0.4950 (12.574)
D1	0.4500 (11.430)	-	0.4560 (11.582)
a	0.3900(9.906)	-	0.4300 (10.922)
b	0.0130 (0.330)	-	0.0210 (0.533)
c	0.0260 (0.660)	-	0.0320 (0.813)
d	0.0900 (2.286)	-	0.1200 (3.048)
e	-	0.0500 (1.270)	-
f	0.1650 (4.191)	-	0.1800 (4.572)
g	0.0075 (0.191)	-	0.0125 (0.318)
h	0.0200 (0.508)	-	-
i	0.1480 (3.760)	-	0.1540 (3.912)
j	0.0420 (1.067) *45°	-	0.048 (1.219)*45°

PLCC28封装外形尺寸

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类型	型号	封装	备注	均可提供 17%增值票
HART 协议芯片	SM HT2015PL	PLCC28P	国产封装进口芯片	优势产品 性能稳定 价格优
HART 协议芯片	SM HT2015LQ	LQFP32P	国产封装进口芯片	优势产品 性能稳定 价格优
HART 协议芯片	HT20C12PL	PLCC28P	进口原装	全新
HART 协议芯片	HT2012PL	PLCC28P	进口原装	全新
HART 协议芯片	HT2015PL	PLCC28P	进口原装	全新
HART 协议芯片	HT20C15PL	PLCC28P	进口原装	全新
HART 协议芯片	HT2015LQ	LQFP32P	进口原装	全新
HART 协议芯片	HT20C15LQ	LQFP32P	进口原装	全新
HART 协议芯片	SYM2015	PLCC28P	进口原装	全新
HART 协议芯片	A5191HRTPG	PLCC28P	进口原装	全新
HART 协议芯片	A5191HRTL	LQFP32P	进口原装	全新
基金会现场总线	FB3050TQ	QFP	进口原装	全新

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# Hart Modem HT2015 Datasheet



## Features

- Can be used in designs presently using the HT2015、A5191HRT SYM20C15 or equivalent type chip
- Single-chip, half-duplex 1200 bits per second FSK modem
- Bell 202 shift frequencies of 1200 Hz and 2200 Hz
- 2.7V-5.0V power supply
- Transmit-signal wave shaping
- Receive band-pass filter
- Low power: optimal for intrinsically safe applications
- CMOS compatible
- Internal oscillator requires 460.8 kHz crystal or ceramic resonator
- Meets HART physical layer requirements
- Industrial temperature range of -40 °C to +85 °C
- Available in a 28-pin PLCC and 32-pin LQFP packages (LQFP pictured)

### General Description

The HT2015 is a single-chip, CMOS modem for use in Highway Addressable Remote Transducer (HART) field instruments and masters. The modem and a few external passive components provide all of the functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect and transmit-signal shaping. The HT2015 is pin-compatible with the HT2015、A5191HRT SYM20C15. See the Pin Description and Functional Description sections for details on pin compatibility with the HT2015、A5191HRT SYM20C15.

The HT2015 uses Phase Continuous Frequency Shift Keying (FSK) at 1200 bits per second. To conserve power the receive circuits are disabled during transmit operations and vice versa. This provides the half-duplex operation used in HART communications.

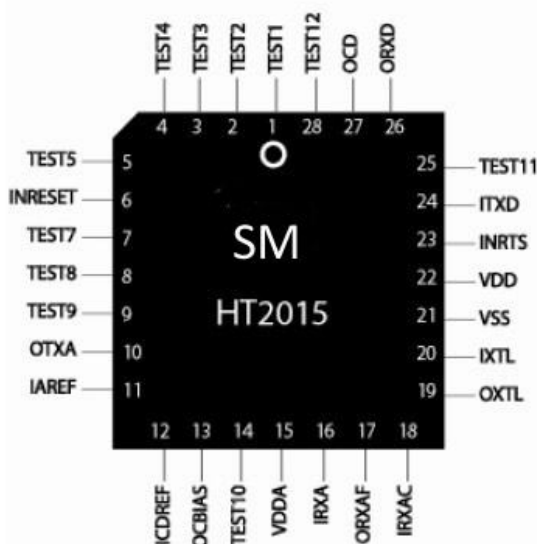


Fig. 1 - 28 pin PLCC Pinout Package

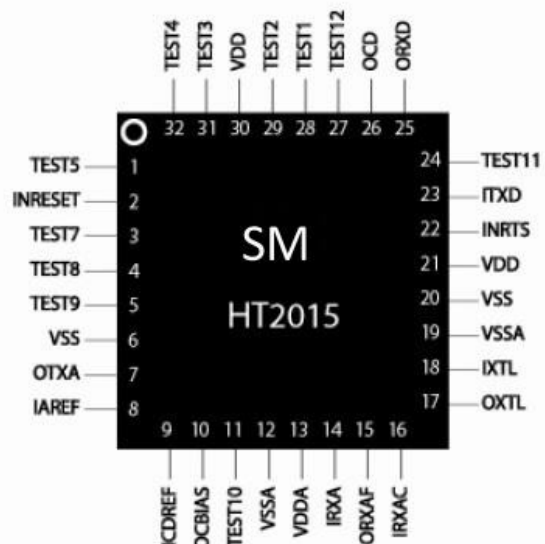


Fig. 2 - 32 pin LQFP Pinout Package

Table 1 - Pin Descriptions

<b>Signal</b>	<b>Type</b>	<b>PLCC</b>	<b>LQFP</b>	<b>Description</b>
TEST1	Input	1	28	Connect to Vss.
TEST2	*	2	29	No connect.
TEST3	*	3	31	No connect.
TEST4	*	4	32	No connect.
TEST5	Input	5	1	Connect to Vss.
INRESET	Input	6	2	Reset all digital logic when low.
TEST7	Input	7	3	Connect to Vss.
TEST8	Input	8	4	Connect to Vss.
TEST9	Input	9	5	Connect to Vss.
OTXA	Output	10	7	Modulated output transmit analog. FSK modulated HART transmit signal to 4-20mA loop interface circuit.
IAREF	Input	11	8	Analog reference voltage.
ICDREF	Input	12	9	Carrier detect reference voltage.
OCBIAS	Output	13	10	Comparator bias current.
TEST10	Input	14	11	Connect to Vss.
VDDA	Power	15	13	Analog supply voltage.
IRXA	Input	16	14	FSK modulated HART receive signal from 4-20mA loop interface circuit.
ORXAF	Output	17	15	Analog receiver filter input.
IRXAC	Input	18	16	Analog receive comparator input.
OXTL	Output	19	17	Crystal oscillator output.
IXTL	Input	20	18	Crystal oscillator input.
VSS	Ground	21	6,20	Ground.
VDD	Power	22	21,30	Digital supply voltage.
INRTS	Input	23	22	Request to send.
ITXD	Input	24	23	Input transmit data. Transmitted HART data stream from UART.
TEST11	*	25	24	No connect.
ORXD	Output	26	25	Received demodulated HART data to UART.
OCD	Output	27	26	Carrier detect output.
TEST12	*	28	27	No connect.
VSSA	Ground	*	12,19	Analog ground.



## **Pin Descriptions:**

### **IAREF: Analog Reference Voltage**

This analog input sets the dc operating point of the operational amplifiers and comparators and is usually selected to split the dc potential between  $V_{DD}$  and  $V_{SS}$ . See IAREF in DC Characteristics on page 11.

### **ICDREF: Carrier Detect Reference Voltage**

This analog input controls at which level the carrier detect (OCD) becomes active. This is determined by the dc voltage difference between ICDREF and IAREF. Selecting ICDREF - IAREF equal to  $0.08V_{DC}$  will set the carrier detect to a nominal 100 mV<sub>p-p</sub>.

### **INRESET: Reset Digital Logic**

When at logic low ( $V_{SS}$ ) this input holds all the digital logic in Reset. During normal operation INRESET should be at  $V_{DD}$ . INRESET should be held low for a minimum of 10nS after  $V_{DD} = 2.5 V$  as shown in Figure 3.

### **INRTS: Request To Send**

This active-low input selects the operation of the modulator. OTXA is enabled when this signal is low. This signal must be held high during power-up.

### **IRXA\*: Analog Receive Input**

This input accepts the 1200/2200 Hz signals from the external filter

### **IRXAC: Analog Receive Comparator Input**

This is the positive input of the carrier detect comparator and the receiver filter comparator.

### **ITXD: Digital Transmit Input (CMOS)**

This input to the modulator accepts digital data in NRZ form. When ITXD is low, the modulator output frequency is 2200 Hz. When ITXD is high, the modulator output frequency is 1200 Hz.

### **IXTL: Oscillator Input**

This input to the internal oscillator must be connected to a parallel mode 460.8 kHz ceramic resonator when using the internal oscillator or grounded when using an external



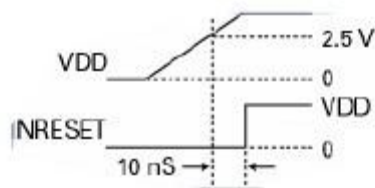
460.8 kHz clock signal.

### **OCBIAS: Comparator Bias Current**

The current through this output controls the operating parameters of the internal operational amplifiers and comparators. For normal operation, OCBIAS current is set to 2.5  $\mu$ A

### **OCD: Carrier Detect Output**

This output goes high when a valid input is recognized on IRXA. If the received signal is greater than the threshold specified on ICDREF for four cycles of the IRXA signal, the valid input is recognized.



**Figure 3 - Reset Timing**

### **ORXAF\*: Analog Receive Filter Output**

This signal is the square wave output of the receiver high-pass filter.

### **ORXD: Digital Receive Output (CMOS)**

This signal outputs the digital receive data. When the received signal (IRXA) is 1200 Hz, ORXD outputs logic high. When the received signal (IRXA) is 2200 Hz, ORXD outputs logic low. ORXD is qualified internally with OCD and is logic high when OCD is low.

### **OTXA: Analog Transmit Output**

This output provides the trapezoidal signal controlled by ITXD. When ITXD is low, the output frequency is 2200 Hz. When ITXD is high, the output frequency is 1200 Hz. This output is active when INRTS is low and 0.5  $V_{DC}$  when INRTS is high.

### **OXTL: Oscillator Output**

This output from the internal oscillator must be connected to an external 460.8kHz clock signal or to a parallel mode 460.8 kHz ceramic resonator when using the internal oscillator.

### **TEST(12:1): Factory Test**

These are factory test pins. For normal operation, tie these signals as per Table 1.

### **VDD: Digital Power**

This is the power for the digital modem circuitry.

**VDDA: Analog Supply Voltage**

This is the power for the analog modem circuitry.

**VSS: Ground**

This is ground.

**VSSA: Analog Ground**

This is the analog ground.

**Functional Description**

The HT2015 is a functional equivalent of the HT2015、A5191HRT SYM20C15 HART Modem. It contains a transmit data modulator and signal shaper, carrier detect circuitry, analog receiver and demodulator circuitry and an oscillator, as shown in Figure 4.

The internal HART modem modulates the transmit-signal and demodulates the receive signal. The transmit-signal shaper enables the HT2015 to transmit a HART compliant signal.

The carrier is detected by comparing the receiver filter output with the difference between two external voltage references. The analog receive circuitry band-pass filters the received signal for input to the modem and the carrier detect circuitry. The oscillator provides the modem with a stable time base using either a simple external resonator or an external clock source.

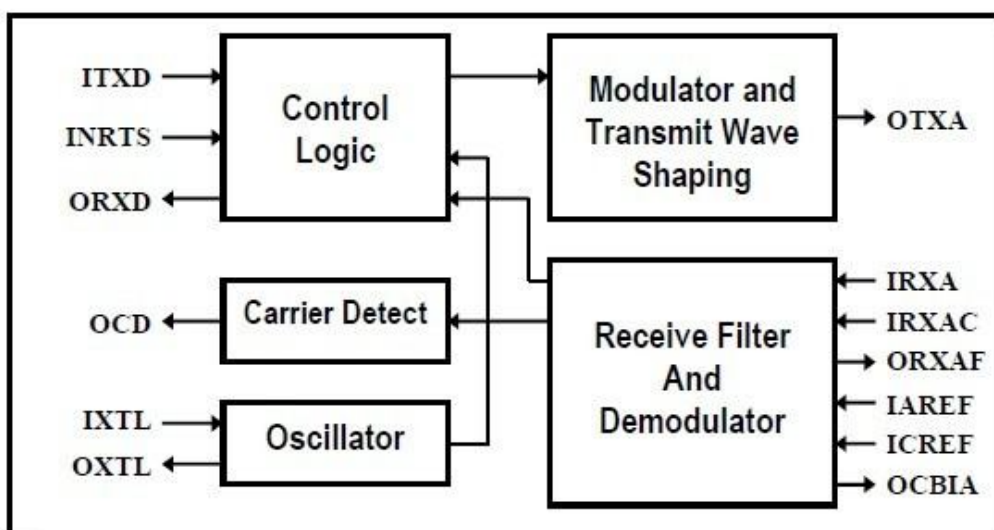


Figure 4 - HT2015 Block Diagram

## Modem Characteristics

### HT2015 LOGIC

The modem consists of a modulator and demodulator. The modem uses shift frequencies of nominally 1200 Hz (for a 1) and 2200 Hz (for a 0). The bit rate is 1200 bits/second.

#### Modulator

The modulator accepts digital data in NRZ form at the ITXD input and generates the FSK modulated signal at the OTXA output. INRTS must be a logic low for the modulator to be active.

#### Demodulator

The demodulator accepts an FSK signal at the IRXA input and reproduces the original modulating signal at the ORXD output. The nominal bit rate is 1200 bits per second. Figure 5 illustrates the demodulation process.

The output of the demodulator is qualified with the carrier detect signal (OCD), therefore, only IRXA signals large enough to be detected (100 mVp-p typically) by the carrier detect circuit produce received serial data at ORXD. Maximum demodulator jitter is 12 percent of one bit given input frequencies within HART specifications, a clock frequency of 460.8 kHz ( $\pm 1.0$  percent) and zero input (IRXA) asymmetry.

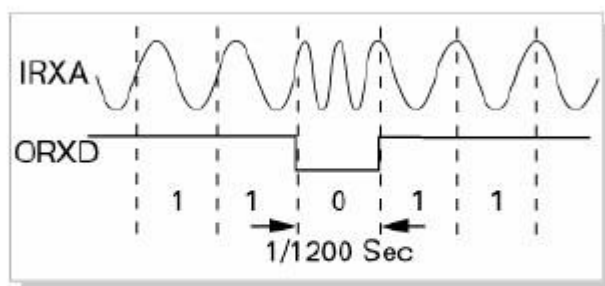


Figure 5: Demodulator Signal Timing

### TRANSMIT-SIGNAL SHAPER

The transmit-signal shaper generates a HART compliant FSK modulated signal at OTXA. Figure 6 and Figure 7 show the transmit-signal forms of the HT2015.

For  $IAREF = 1.235 V_{DC}$ , OTXA will have a voltage swing from approximately 0.25 to 0.75  $V_{DC}$ .

### CARRIER DETECT CIRCUITRY

The Carrier Detect Comparator shown in Figure 8 generates logic low output if the IRXAC voltage is below  $ICDREF$ . The comparator output is fed into a carrier detect block (see Figure 4 on page 6). The carrier detect block drives the carrier detect output pin OCD

high if INRTS is high and four consecutive pulses out of the comparator have arrived. OCD stays high as long as INRTS is high and the next comparator pulse is received in less than 2.5 ms. Once OCD goes inactive, it takes four consecutive pulses out of the comparator to assert OCD again. Four consecutive pulses amount to 3.33 ms when the received signal is 1200 Hz and to 1.82 ms when the received signal is 2200 Hz.

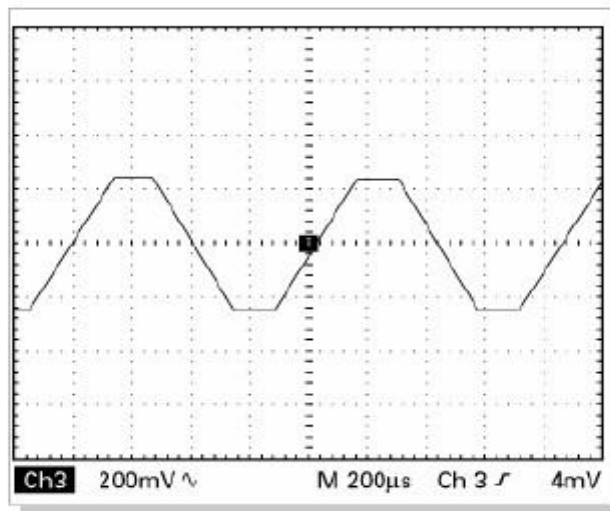
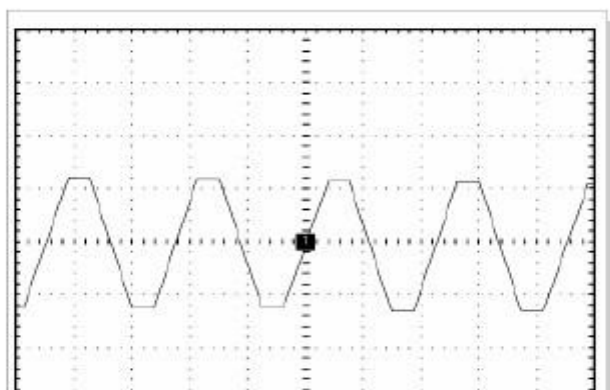


Figure 6 - OTXA Waveform (1200 Hz)



## ANALOG RECEIVER CIRCUITRY

### Voltage References

The HT2015 requires two voltage references, IAREF and ICDREF.

IAREF sets the dc operating point of the internal operational amplifiers and comparators. A 1.235 V<sub>DC</sub> reference (Analog Devices AD589) is suitable as IAREF.

The level at which OCD (carrier detect) becomes active is determined by the dc voltage difference (ICDREF - IAREF). Selecting a voltage difference of 0.08 V<sub>DC</sub> will set the carrier detect to a nominal 100 mV<sub>p-p</sub>.

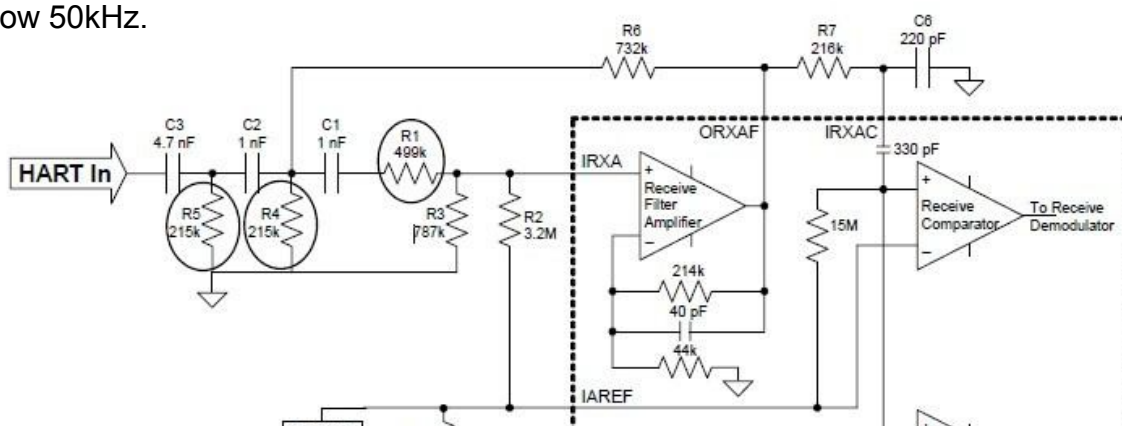
### Bias Current Resistor

The HT2015 requires a bias current resistor to be connected between OCBIAS and V<sub>SS</sub>. The bias current controls the operating parameters of the internal operational amplifiers and comparators.

The value of the bias current resistor is determined by the reference voltage IAREF and the following formula:

$$R_{BIAS} = \left( \frac{IAREF}{2.5 \mu A} \right)$$

The recommended bias current resistor is 499 Kohm; when IAREF is equal to 1.235 V<sub>DC</sub>. In Figure 8 all external capacitor values have a tolerance of ±5 percent and the resistors have a tolerance of ±1 percent, except the 3 ohm; which has a tolerance of ±5 percent. External to the HT2015, the filter exhibits a three-pole, high-pass filter at 624 Hz and a onepole, low-pass filter at 2500 Hz. Internally, the HT2015 has a high-pass pole at 35 Hz and a low-pass pole at 90 kHz. The low-pass pole can vary as much as ±30 percent. The input impedance of the entire filter is greater than 150 Kohm; at frequencies below 50kHz.



## OSCILLATOR

The HT2015 requires a 460.8kHz clock signal on OXTL. This can be provided by an external clock or external components may be connected to the HT2015 internal oscillator.

### Internal Oscillator Option

The oscillator cell will function with either a 460.8 kHz crystal or ceramic resonator. A parallel resonant ceramic resonator can be connected between OXTL and IXTL. Figure 9 illustrates the crystal option for clock generation using a 460.8 kHz ( $\pm 1$  percent tolerance) parallel resonant crystal and two tuning capacitors. The actual values of the capacitors may depend on the recommendations of the manufacturer of the resonator. Typically, capacitors in the range of 100 pF to 470pF are used.

### External Clock Option

It may be desirable to use an external 460.8 kHz clock as shown in Figure 10 rather than the internal oscillator because of the high cost and low availability of ceramic resonators. In addition, the HT2015 consumes less current when an external clock is used. Minimum current consumption occurs with the clock connected to OXTL and IXTL connected to V<sub>SS</sub>.

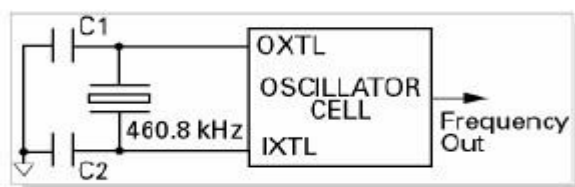
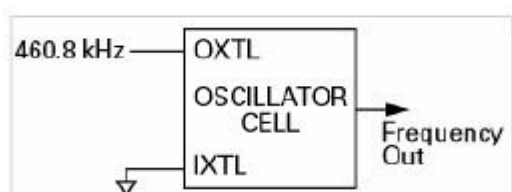


Figure 9 - Crystal Oscillator





## Electrical Characteristics

ABSOLUTE MAXIMUMS				
Symbol	Parameter	Min.	Max.	Units
T <sub>A</sub>	Ambient	-40	+85	C
T <sub>s</sub>	Storage Temperature	-55	150	C
V <sub>DD</sub>	Supply Voltage	2.7	6.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input, Output	2.7	V <sub>DD</sub> + .3	V
T <sub>L</sub>	Lead Temperature (soldering)		250	C

**Cautions:**

1. CMOS devices are damaged by high-energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted. Precautions should be taken to avoid application of voltages higher than the maximum rating. Stresses above absolute maximum ratings may result in damage to the device.
2. Remove power before insertion or removal of this device.

DC CHARACTERISTICS						
(V <sub>DD</sub> = 3.0V to 5.5V, V <sub>SS</sub> = 0V, T <sub>A</sub> = -40C to +85C)						
Symbol	Parameter	V <sub>DD</sub>	Min.	Typical	Max.	Units
V <sub>IL</sub>	Input Voltage, Low	3.0 - 5.5			.3 * V <sub>DD</sub>	V
V <sub>IH</sub>	Input Voltage	3.0 - 5.5	.7 * V <sub>DD</sub>			V
V <sub>OL</sub>	Output Voltage, Low (I <sub>OL</sub> = .67mA)	3.0 - 5.5			.4	V
V <sub>OH</sub>	Output Voltage, High (I <sub>OH</sub> = .67mA)	3.0 - 5.5	2.4			V
C <sub>IN</sub>	Input Capacitance Analog Input IRXA Digital Input			2.9 25 3.5		pF
I <sub>I<sub>LH</sub></sub>	Input Leakage Current				+/-500	nA
I <sub>O<sub>LL</sub></sub>	Output Leakage Current				+/-10	μA
I <sub>DD</sub>	Power Supply Current (R <sub>BIAS</sub> = 500kΩ, I <sub>A<sub>REF</sub></sub> = 1.235V)	3.3 5.0		150 170	180 200	μA
I <sub>A<sub>REF</sub></sub>	Analog Reference	3.3 5.0	1.2	1.235 2.5	2.6	V
I <sub>C<sub>D<sub>REF</sub></sub></sub> *	Carrier Detect Reference			1.15		V



<b>AC CHARACTERISTICS</b>					
(V <sub>DD</sub> = 3.0V to 5.5V, V <sub>SS</sub> = 0V, T <sub>A</sub> = -40C to +85C)					
Pin Name	Description	Min.	Typical	Max.	Units
IRXA	Receive Analog Input Leakage Current			+/-150	nA
	Frequency - Mark (Logic 1)	1190	1200	1210	Hz
	Frequency - Space (Logic 0)	2180	2200	2220	Hz
ORXAF	Output of the High-pass Filter Slew Rate		.025		V/ $\mu$ s
	Gain Bandwidth (GBW)	150			kHz
	Voltage Range	.15		V <sub>DD</sub> - .15	V/ $\mu$ s
IRXAC	Carrier Detect & Receive Filter Input Leakage Current			+/-500	nA
OTXA	Modulator Output Frequency * - Mark (Logic 1)		1196.9		Hz
	Frequency - Space (Logic 0)		2194.3		Hz
	Amplitude (IAREF 1.235 V)		500		mV p-p
	Slope		2.79		mV/ $\mu$ s
	Loading (IAREF = 1.235 V)	30			k $\Omega$
ORXD	Receive Digital Output Rise/Fall Time	20			ns
OCD	Carrier Detect Output Rise/Fall Time	20			ns

\* The modular output frequencies are proportional to the input clock frequency (460.8 kHz)

<b>MODEM CHARACTERISTIC</b>				
(V <sub>DD</sub> = 2.7V to 5.5V, V <sub>SS</sub> = 0V, T <sub>A</sub> = -40 C to +85 C)				
Parameter	Min.	Typical	Max	Units
Demodulator Jitter Conditions 1. Input frequencies at 1200 Hz +/-10 Hz, 2200 Hz +/-20 Hz 2. Clock frequency of 460.8 kHz +/-0.1% 3. Input (HLXA) asymmetry, 0			12	% of 1 bit

<b>CERAMIC RESONATOR - EXTERNAL CLOCK SPECIFICATIONS</b>				
(V <sub>DD</sub> = 2.7V to 5.5V, V <sub>SS</sub> = 0V, T <sub>A</sub> = -40 C to +85 C)				
Parameter	Min.	Typical	Max	Units
Resonator Tolerance			1.0	%
Frequency	460.8			kHz
External Clock Frequency	456.2	460.8	465.4	kHz
	40	50	60	%
		V <sub>OH</sub> - V <sub>OL</sub>		V

Mechanical Specification

Symbol	Min	Nom	Max
A	.165	.172	.180
A1	.099	.101	.110
D	.485	.490	.495
D1	.450	.452	.455
D2	.390	.420	.430
D3	.300 REF		
E	.485	.490	.495
E1	.450	.452	.455
E2	.390	.420	.430
E3	.300 REF		
e	.050 BSC		

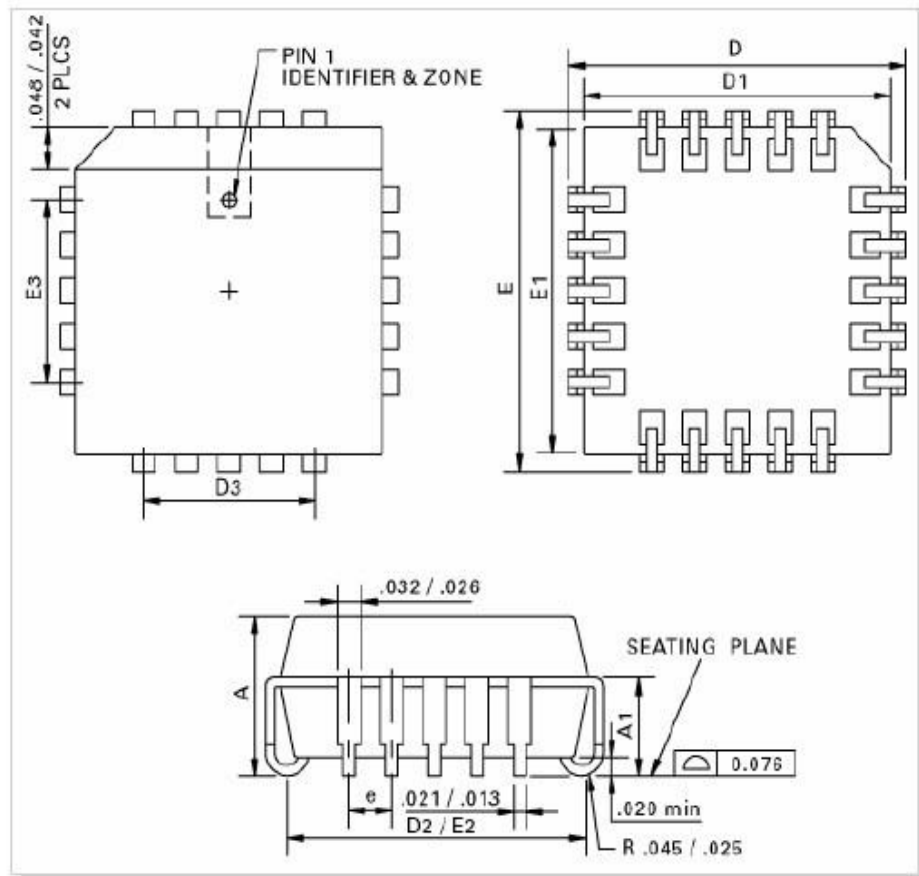


Figure 11 - 28-pin PLCC Mechanical Specification

Symbol	Min	Nom	Max
A	-	-	1.60
A1	.05	.01	.15
A2	1.35	1.40	1.45
D	9.00 BSC		
D/2	4.50 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E/2	4.50 BSC		
E1	7.00 BSC		
L	.45	.60	.75
e	.80 BSC		
b	.30	.37	.45
c	.09	-	.20
ccc	-	-	.10
ddd	-	-	.20

