Zero standby power universal PAL® devices

PLC18V8Z Series

FEATURES

- 20-pin Universal Programmable Array Logic
- Virtually Zero-Standby-power
- Functional replacement for Series 20 PAL devices
  - I_{OL} = 24mA
- High-performance CMOS EPROM cell technology
  - Erasable
  - Reconfigurable
  - 100% testable
- 40ns Max propagation delay.
- Up to 18 inputs and 8 input/output macro cells
- Programmable output polarity
- Power-up reset on all registers
- Register Preload capability
- Synchronous Preset/Asynchronous Reset
- Security fuse to prevent duplication of proprietary designs
- Design support provided using AMAZE software development package and other CAD tools for PLDs
- Available in 300mil-wide DIP with quartz window, ceramic DIP (OTP)

APPLICATIONS

- Battery powered instruments
- Laptop and pocket computers
- Industrial control
- Medical Instruments
- Portable communications equipment

DESCRIPTION

The PLC18V8Z is a universal PAL® device featuring high performance and virtually zero-standby power for power sensitive applications. It is a reliable, user-configurable substitute for discrete TTL/CMOS logic. While compatible with TTL and HCT it can also replace HC logic over the V_{CC} range of 4.5 to 5.5V.

The PLC18V8Z is a two-level logic element comprised of 10 inputs, 74 AND gates (product terms) and 8 output Macro cells.

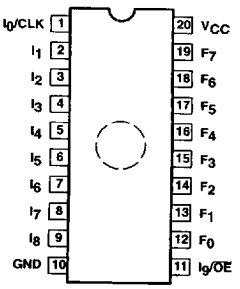
Each output features an "Output Macro Cell" which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the it is capable of emulating all common 20-pin PAL devices to reduce documentation, inventory, and manufacturing costs.

A power-up reset function and a Register Preload function have been incorporated in the architecture to facilitate state machine design and testing.

With a standby current of less than 250µA and active power consumption of 2mA/MHz, the device is ideally suited for power sensitive applications in battery operated/backed portable instruments and computers.

The PLC18V8Z is also processed to industrial requirements for operation over an extended temperature range of -55°C to +125°C and supply voltage of 4.5V to 5.5V.

PIN CONFIGURATIONS



PIN LABEL DESCRIPTIONS

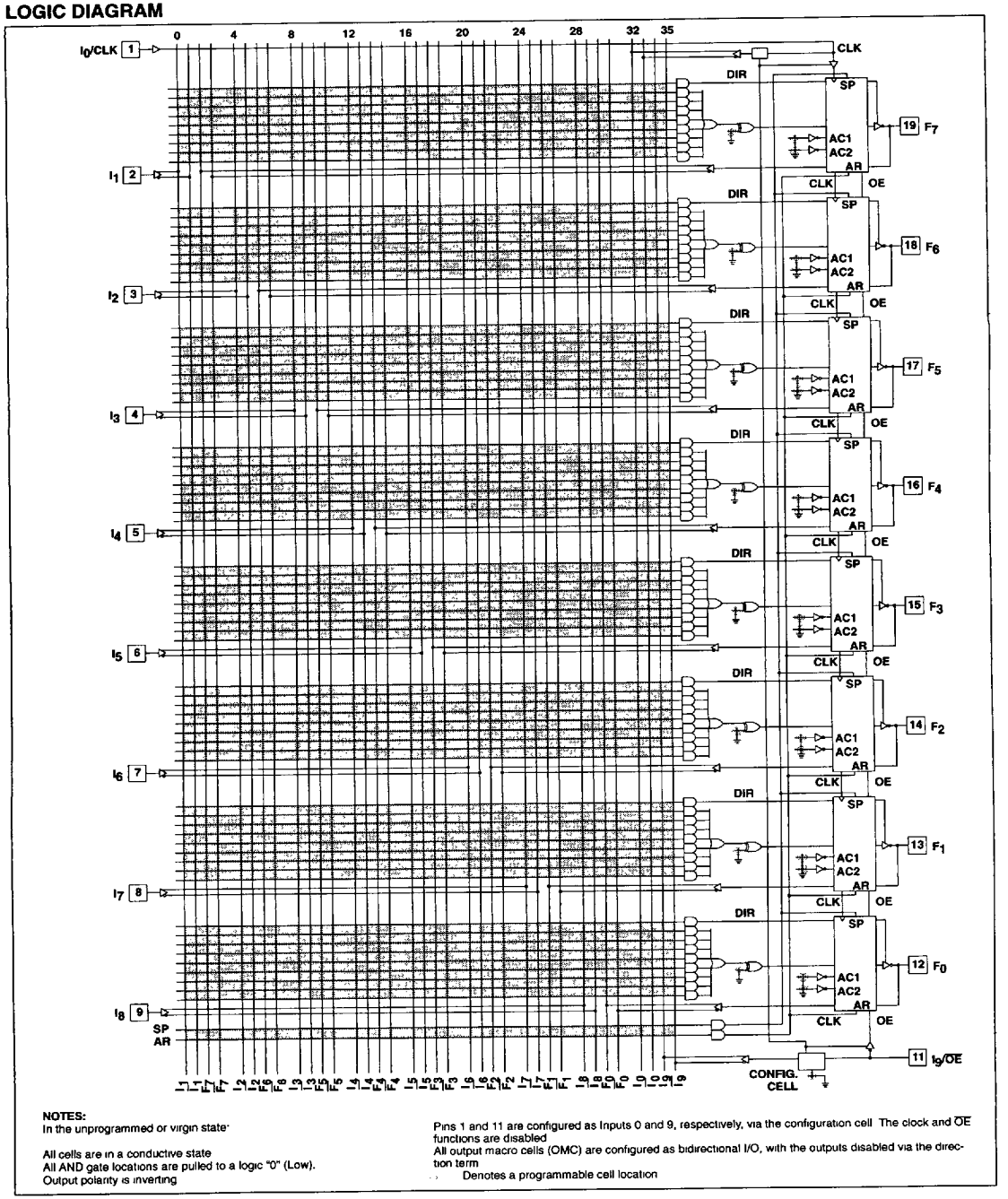
I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)
F	Macrocell Input/Output
CLK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic Dual In-Line Package 300mil-wide	PLC18V8Z/ BRA (OT)	GDIP1-T20
20-Pin Ceramic Dual In-Line Package 300mil-wide w/ quartz window	PLC18V8Z/ BRA	GDIP1-T20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

LOGIC DIAGRAM



NOTES:
In the unprogrammed or virgin state:

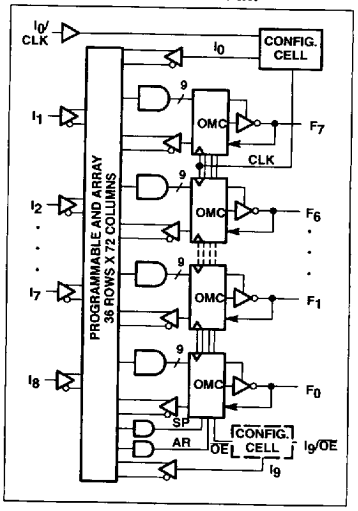
All cells are in a conductive state
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
. . Denotes a programmable cell location

PAL DEVICE TO PLC18V8Z OUTPUT PIN CONFIGURATION CROSS REFERENCE

PIN NO.	PLC 18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	I_9/$\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

FUNCTIONAL DIAGRAM



The Philips Semiconductors state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Philips Semiconductors to functionally test the devices prior to shipment to the customer.

Additionally, this allows Philips Semiconductors to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

THE OUTPUT MACRO CELL (OMC)

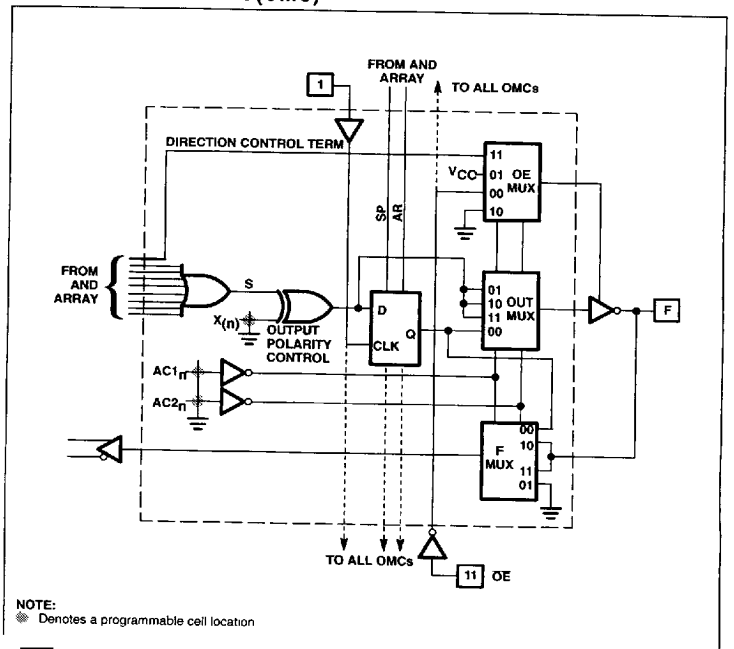
The PLC18V8Z series devices have 8 individually programmable Output Macro Cells The 74 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the configuration cell table, 4 different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

DESIGN SECURITY

The PLC18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

OUTPUT MACRO CELL (OMC)



NOTE:
▒ Denotes a programmable cell location

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

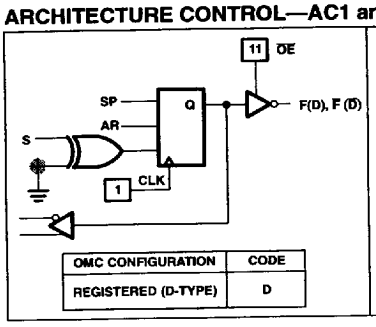
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

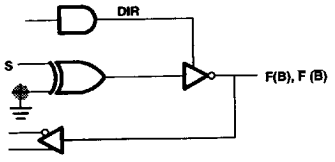
FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_1$	$AC2_N$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registerd OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

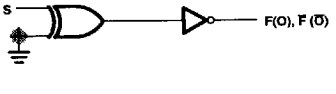
ARCHITECTURE CONTROL—AC1 and AC2



OMC CONFIGURATION	CODE
REGISTERED (D-TYPE)	D

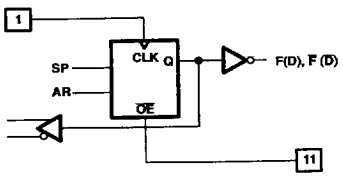


OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B

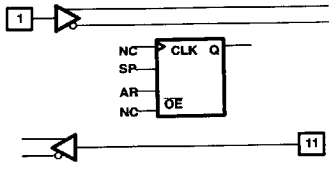


OMC CONFIGURATION	CODE
FIXED OUTPUT	O

OMC CONFIGURATION	CODE
FIXED INPUT	I



CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L



CONFIGURATION CELL	CODE
PIN 1 = INPUT PIN 11 = INPUT	H[6]

NOTE:
A factory shipped unprogrammed device is configured such that:
1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V_{DC}
V_{CC}	Operating supply voltage	4.5 to 5.5	V_{DC}
V_{IN}	Input voltage	-0.5 to V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	-0.5 to V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	-10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$-55°C \leq T_{amb} \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Input voltage						
V_{IL}	Low	V_{CC} = MIN	-0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[3]						
V_{OL}	Low	V_{CC} = MAX, I_{OL} = 24mA			0.500	V
V_{OH}	High	V_{CC} = MAX, I_{OH} = -3.2mA	2.4			V
Input current						
I_{IL}	Low[6]	V_{IN} = GND			-10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 -10	µA µA
I_{OS}	Short-circuit[4]	V_{CC} = MAX, V_{OUT} = GND			-130	mA
I_{CC}	V_{CC} supply current (Standby)	V_{CC} = MAX, V_{IN} = 0 or V_{CC}[7]			250	µA
I_{CC}/f	V_{CC} supply current (Active)[5]	V_{CC} = MAX			2.0	mA/MHz
Capacitance						
C_I[12]	Input	V_{CC} = 5V V_{IN} = 2.0V		12	17	pF
C_B[12]	I/O	V_B = 2.0V		15	20	pF

AC ELECTRICAL CHARACTERISTICS

$-55°C \le T_{amb} \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[8]		LIMITS		UNIT
				R_1 (W)	C_L (pF)	MIN	MAX	
Pulse width								
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)[13]	CLK +	CLK +	200	50	40		ns
t_{CKH}	Clock width High	CLK +	CLK -	200	50	15		ns
t_{CKL}	Clock width Low	CLK -	CLK +	200	50	15		ns
t_{ARW}[11]	Async reset pulse width	I ±, F±	I $\overline{+}$, F $\overline{+}$			40	ns	
Hold time								
t_{IH}	Input or feedback data hold time	CLK +	Input ±	200	50	0		ns
Setup time								
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	200	50	22		ns
Propagation delay								
t_{PD}	Delay from input to active output	I ±, F±	F±	200	50		30	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	200	50		18	ns
t_{OE1}[10]	Product term enable to outputs off	I ±, F±	F±	Active-High R = 1.5k Active-Low R = 550	50		30	ns
t_{OD1}[9]	Product term disable to outputs off	I ±, F±	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		30	ns
t_{OD2}[9]	Pin 11 output disable High to outputs off	OE -	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		25	ns
t_{OE2}[10]	Pin 11 output enable to active output	OE +	F±	Active-High R = 1.5k Active-Low R = 550	50		25	ns
t_{ARD}[11]	Async reset delay	I ±, F±	F +				40	ns
t_{ARR}[11]	Async reset recovery time	I ±, F±	CLK +			30		ns
t_{SPR}[11]	Sync preset recovery time	I ±, F±	CLK +			30		ns
t_{PPR}[11]	Power-up reset	V_{CC} +	F +				40	ns
Frequency of operation								
f_{MAX}	Maximum frequency	$1/(t_{IS} + t_{CKO})$[13]		200	50		25	MHz

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Duration of short-circuit should not exceed one second. Test one at a time.
5. Measured with all outputs switching.
6. I_{IL} for Pin 1 (I_O/CLK) is ± 10µA with V_{IN} = 0.4V.
7. V_{IN} includes CLK and $\overline{OE}$ if applicable.
8. Refer also to AC Test Conditions. (Test Load Circuit)
9. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the V_T (V_{OL} +0.5V) with S_1 closed.
10. Resistor values of 1.5k and 550ohm provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.
11. Not tested, guaranteed by design/characterization.
12. Only tested for initial qualification, or after any design changes which may effect this parameter.
13. This parameter is guaranteed by testing the individual parameters specified in this equation.

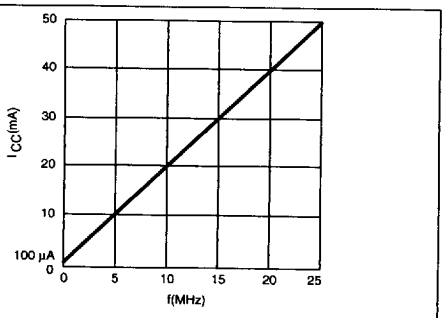


Figure 1. I_{CC} vs Frequency (Worst Case)

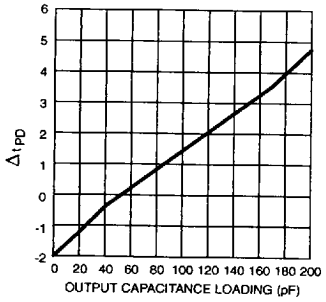
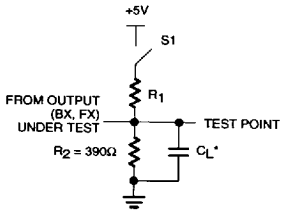


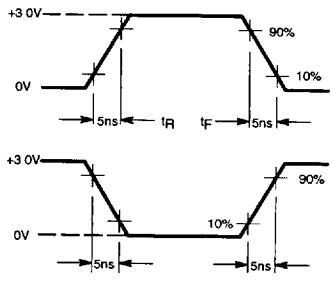
Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC TEST CONDITIONS



Test Load Circuit

VOLTAGE WAVEFORMS



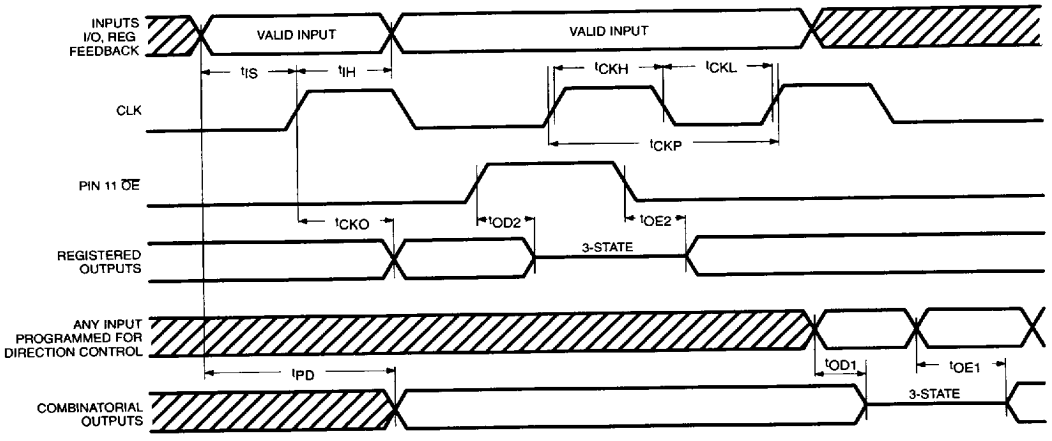
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified

Input Pulses

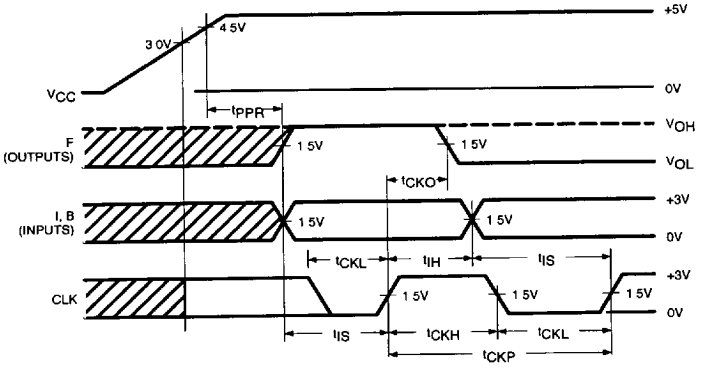
POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC18V8Z. All internal registers will reset to active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the active-High output condition during a system power-up condition.

TIMING DIAGRAMS



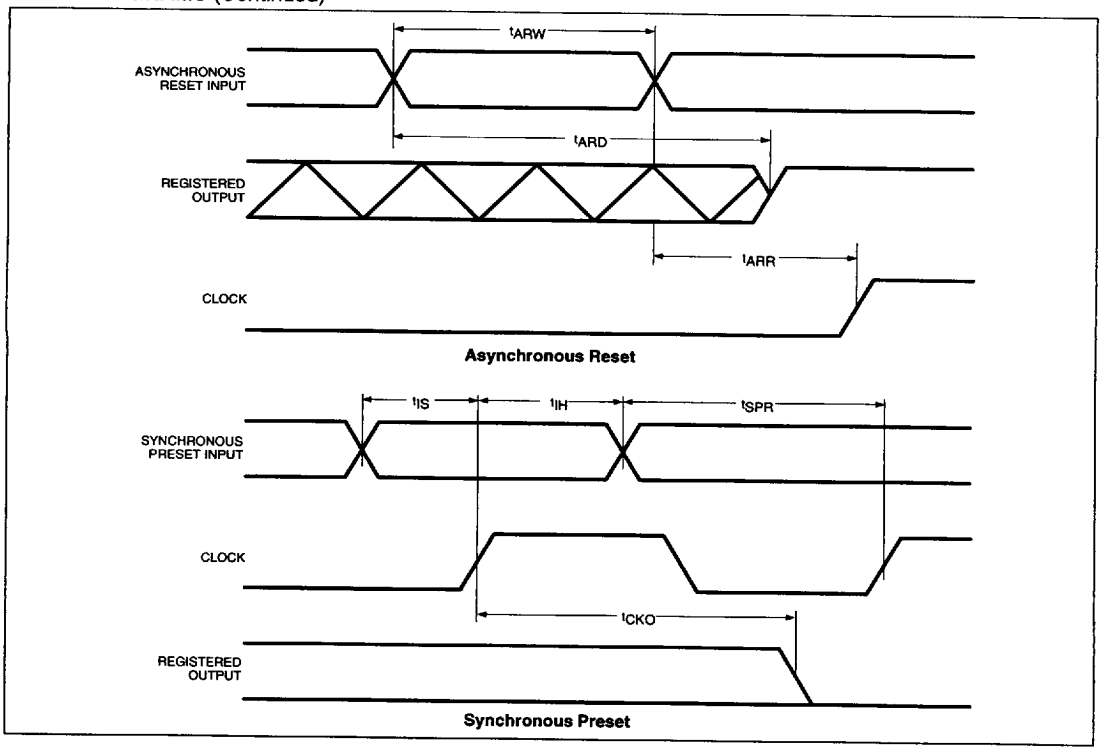
Switching Waveforms



NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Power-Up Reset

TIMING DIAGRAMS (Continued)



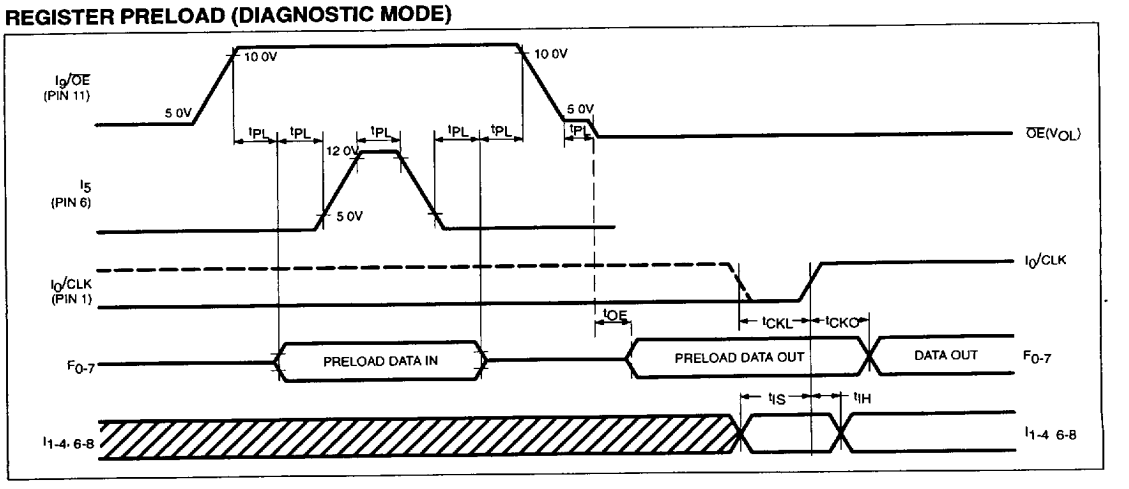
REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_9/\overline{OE}$ and I_5). (See diagram for timing and sequence.)

To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F0-F7 during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F0-F7.

Refer to the voltage waveform for timing and voltage references. t_{PL} = 10µsec.

REGISTER PRELOAD (DIAGNOSTIC MODE)



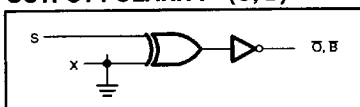
LOGIC PROGRAMMING

The PLC18V8Z can be programmed by means of Logic Programming equipment.

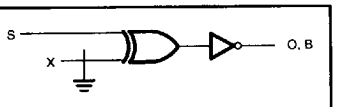
With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY - (O, B)

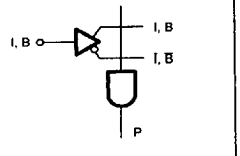


ACTIVE LEVEL	CODE
INVERTING[1]	L

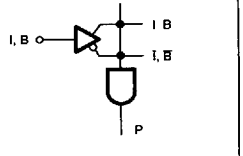


ACTIVE LEVEL	CODE
NON-INVERTING	H

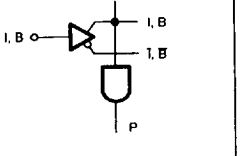
"AND" ARRAY - (I, B)



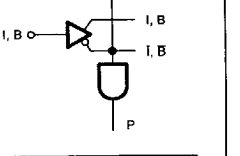
STATE	CODE
DON'T CARE	-



STATE	CODE
INACTIVE[1]	O



STATE	CODE
I, B	H



STATE	CODE
I, B	L

NOTE:
1. A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical PLC18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

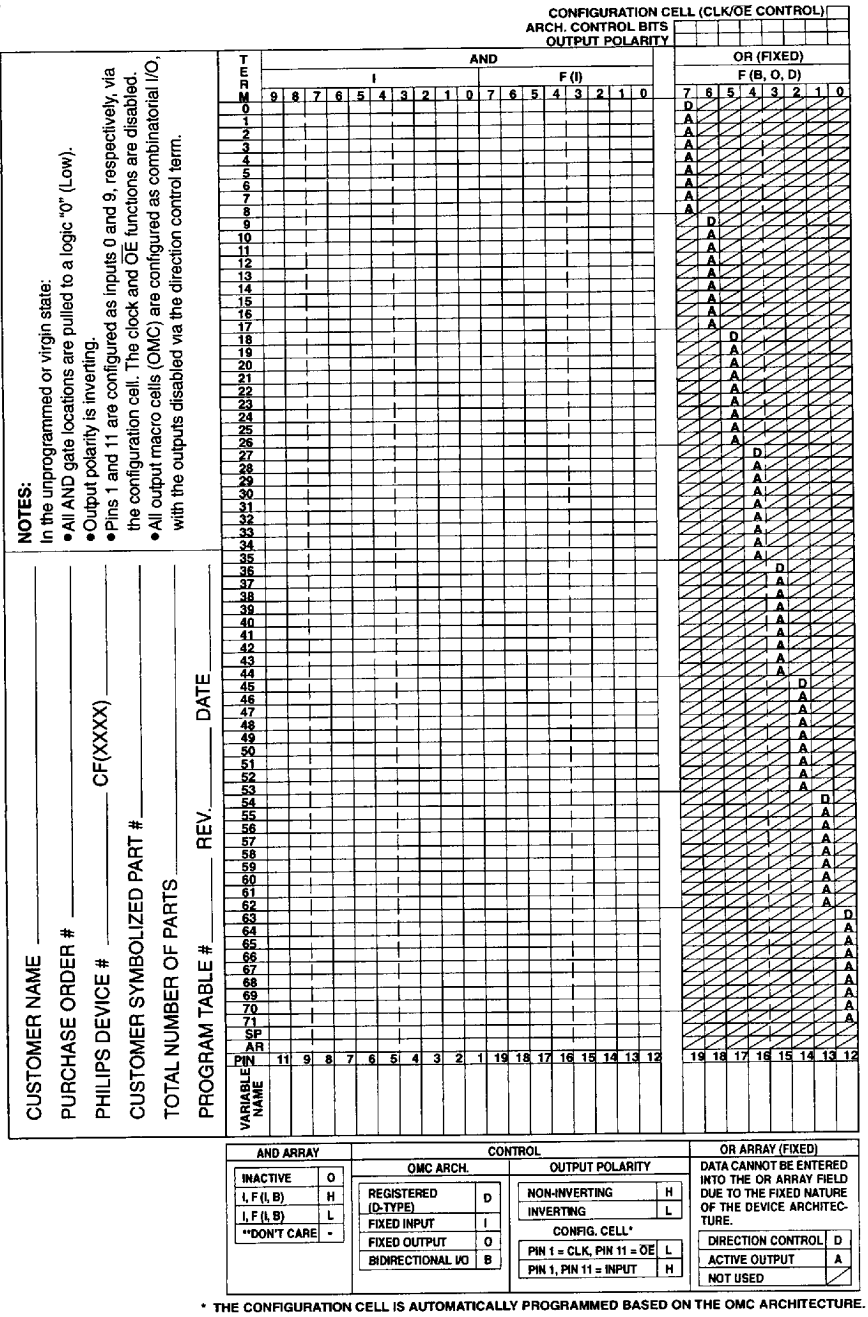
PROGRAMMING

The PLC18V8Z35/I is programmable on conventional programmers for 20-pin PAL devices. Refer to the following charts for qualified manufacturers of programmers and software tools:

PROGRAMMER MANUFACTURER	PROGRAMMER MODEL	FAMILY/PINOUT CODES
DATA I/O CORPORATION 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073-9746 (800) 247-5700	System 29B, LogicPak™ 303A-011A; V09 (DIL) 303A-011B; V04 (PLCC) UNISITE 40/48 V2.5 (DIL) Chipsite (PLCC) - TBA MODEL 60 TBA	86/4F
STAG MICROSYSTEMS, INC. 1600 WYATT DRIVE, SUITE 3 SANTA CLARA, CALIFORNIA 95054 (408) 988-1118	ZL30/30A PROGRAMMER REV. 30A34 (DIL) 30A001 Adaptor (PLCC) PPZ PROGRAMMER TBA	12/205

SOFTWARE MANUFACTURER	DEVELOPMENT SYSTEM
PHILIPS SEMICONDUCTORS COMPANY 811 EAST ARQUES AVENUE P.O. BOX 3409 SUNNYVALE, CALIFORNIA 94088-3409 (408) 991-2000	AMAZE SOFTWARE REV. 1.8 and LATER
DATA I/O 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073-9746 (800) 247-5700	ABEL™ SOFTWARE
LOGICAL DEVICES, INC. 1201 NORTHWEST 65TH PLACE FORT LAUDERDALE, FLORIDA 33309 (800) 331-7766	CUPL™ SOFTWARE

PROGRAM TABLE



* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.
** FOR SP, AR: "-" IS NOT ALLOWED.