

LH52256AS

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time: 500 ns (MAX.)
- Supply current:
 - Operating: 36 mW (MAX.)
 - 18 mW (t_{RC} , $t_{WC} = 1 \mu s$ (TYP.))
 - Standby: 72 μW (MAX.)
- Low voltage operation: 2.5 V to 3.6 V
- Fully-static operation
- Three-state outputs
- Packages:
 - 28-pin, 450-mil SOP
 - 28-pin, 8 × 13 mm² TSOP (Type I)

DESCRIPTION

The LH52256AS is a static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

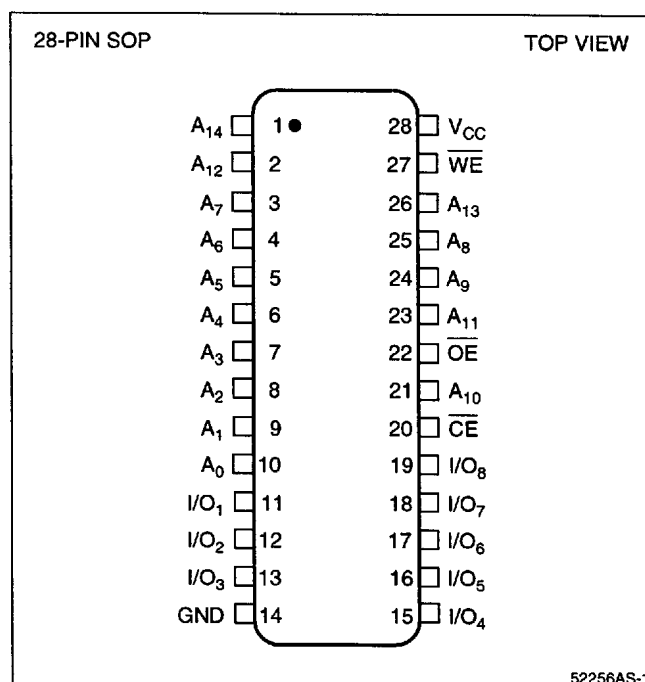


Figure 1. Pin Connections for SOP Package

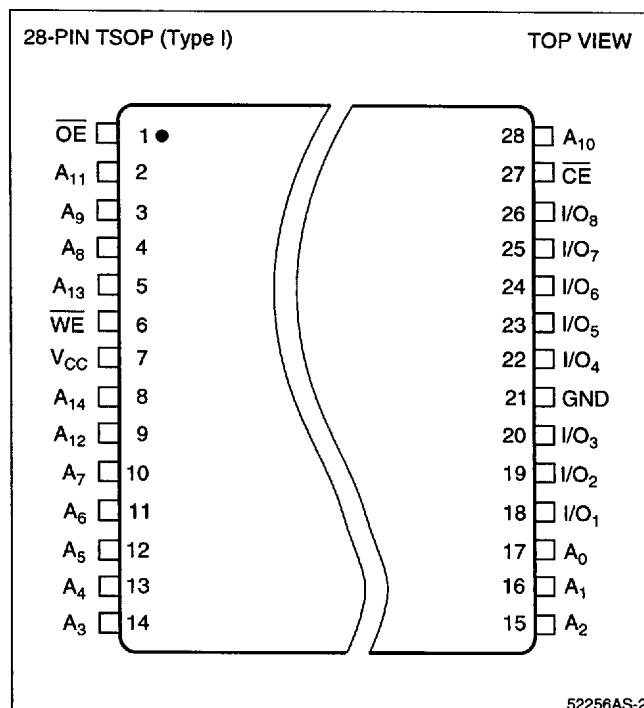


Figure 2. Pin Connections for TSOP Package

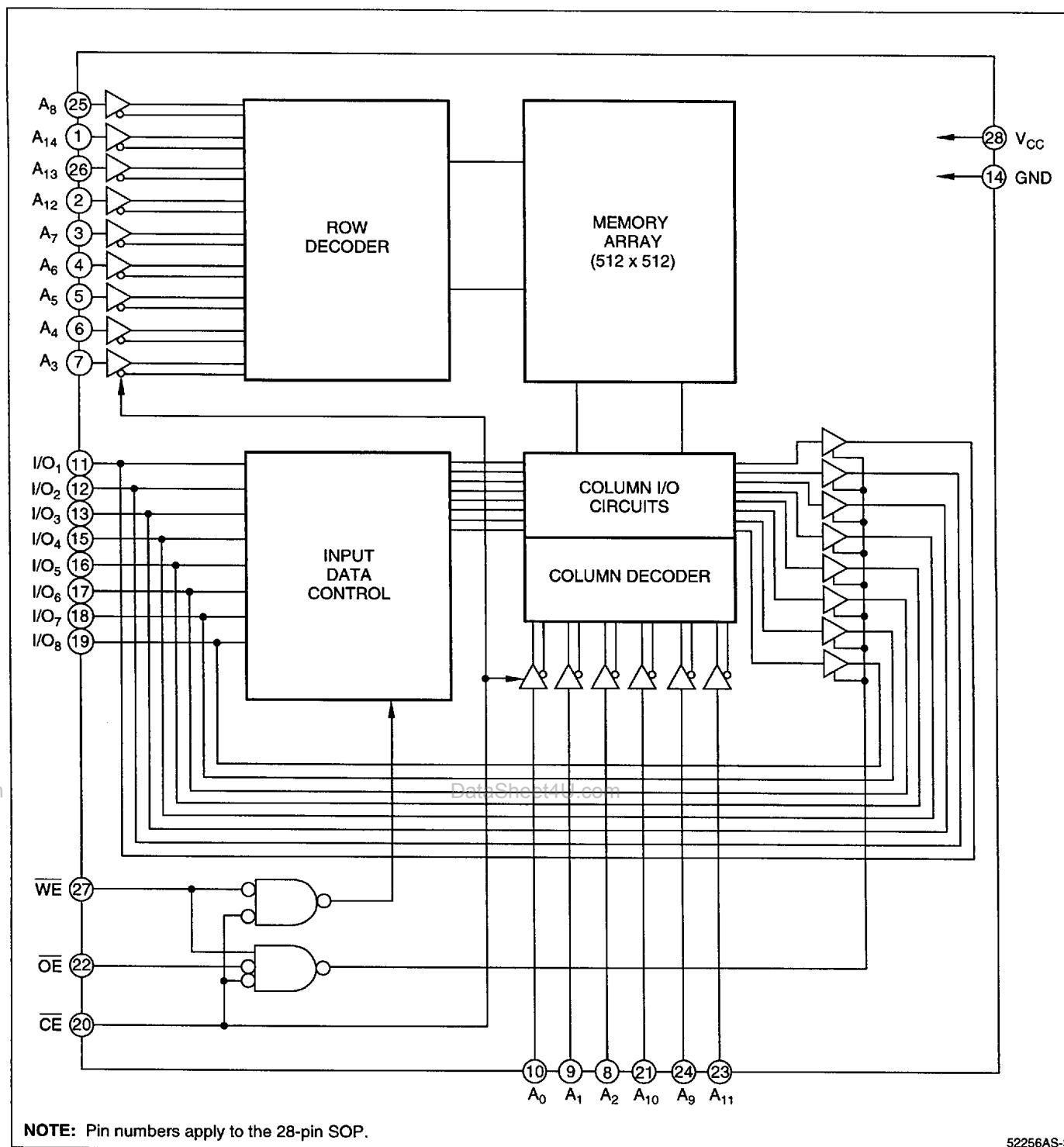


Figure 3. LH52256AS Block Diagram

PIN DESCRIPTION

| SIGNAL | PIN NAME |
|----------------------------------|---------------------|
| A ₀ - A ₁₄ | Address inputs |
| \overline{CE} | Chip Enable input |
| \overline{WE} | Write Enable input |
| \overline{OE} | Output Enable input |

| SIGNAL | PIN NAME |
|-------------------------------------|-------------------------|
| I/O ₁ - I/O ₈ | Data inputs and outputs |
| V _{CC} | Power supply |
| GND | Ground |

TRUTH TABLE

| \overline{CE} | \overline{WE} | \overline{OE} | MODE | I/O ₁ - I/O ₈ | SUPPLY CURRENT | NOTE |
|-----------------|-----------------|-----------------|----------------|-------------------------------------|------------------------------|------|
| H | X | X | Standby | High-Z | Standby (I _{SB}) | 1 |
| L | L | X | Write | D _{IN} | Operating (I _{CC}) | 1 |
| L | H | L | Read | D _{OUT} | Operating (I _{CC}) | |
| L | H | H | Output disable | High-Z | Operating (I _{CC}) | |

NOTE:

- X = H or L.

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT | NOTE |
|-----------------------|------------------|-------------------------------|------|------|
| Supply voltage | V _{CC} | -0.3 to +7.0 | V | 1 |
| Input voltage | V _{IN} | -0.3 to V _{CC} + 0.3 | V | 1, 2 |
| Operating temperature | T _{opr} | -10 to +70 | °C | |
| Storage temperature | T _{stg} | -65 to +150 | °C | |

NOTES:

- The maximum applicable voltage on any pin with respect to GND.
- V_{IN} (MIN.) = -3.0 V for pulse width ≤ 50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = -10°C to +70°C)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|----------------|-----------------|-----------------------|------|-----------------------|------|------|
| Supply voltage | V _{CC} | 2.5 | | 3.6 | V | |
| Input voltage | V _{IH} | V _{CC} - 0.5 | | V _{CC} + 0.3 | V | |
| | V _{IL} | -0.3 | | 0.2 | V | 1 |

NOTE:

- V_{IN} (MIN.) = -3.0 V for pulse width ≤ 50 ns.

DC CHARACTERISTICS ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 2.5\text{ V}$ to 3.6 V)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | MAX. | UNIT |
|--------------------------|-----------|---|----------------|------|---------------|
| Input leakage current | I_{LI} | $V_{IN} = 0\text{ V}$ to V_{CC} | -1.0 | 1.0 | μA |
| Output leakage current | I_{LO} | $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{IO} = 0\text{ V}$ to V_{CC} | -1.0 | 1.0 | μA |
| Operating supply current | I_{CC} | Minimum cycle, $V_{IN} = V_{IL}$ or V_{IH} $I_{IO} = 0\text{ mA}$, $\overline{CE} = V_{IL}$ | | 10 | mA |
| | | t_{RC} , $t_{WC} = 1\ \mu\text{s}$, $V_{IN} = V_{IL}$ or V_{IH} , $I_{IO} = 0\text{ mA}$, $\overline{CE} = V_{IL}$ | | 5 | |
| Standby supply current | I_{SB} | $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ | | 20 | μA |
| | I_{SB1} | $\overline{CE} = V_{IH}$ | | 0.4 | mA |
| Output voltage | V_{OL} | $I_{OL} = 0.5\text{ mA}$ | | 0.5 | V |
| | V_{OH} | $I_{OH} = -0.5\text{ mA}$ | $V_{CC} - 0.5$ | | |

READ CYCLE ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 2.5\text{ V}$ to 3.6 V)

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | NOTE |
|--|-----------|------|------|------|------|
| Read cycle time | t_{RC} | 500 | | ns | |
| Address access time | t_{AA} | | 500 | ns | |
| Chip enable access time | t_{ACE} | | 500 | ns | |
| Output enable access time | t_{OE} | | 250 | ns | |
| Output hold time | t_{OH} | 20 | | ns | |
| \overline{CE} Low to output in Low-Z | t_{LZ} | 10 | | ns | 1 |
| \overline{OE} Low to output in Low-Z | t_{OLZ} | 10 | | ns | 1 |
| \overline{CE} High to output in High-Z | t_{HZ} | 0 | 60 | ns | 1 |
| \overline{OE} High to output in High-Z | t_{OHZ} | 0 | 60 | ns | 1 |

NOTES:

- Active output to high-impedance and high-impedance to output active tests specified for a $\pm 200\text{ mV}$ transition from steady state levels into the test load.

WRITE CYCLE ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 2.5\text{ V}$ to 3.6 V)

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | NOTE |
|---|------------------|------|------|------|------|
| Write cycle time | t _{WC} | 500 | | ns | |
| $\overline{\text{CE}}$ Low to end of write | t _{CW} | 350 | | ns | |
| Address valid to end of write | t _{AW} | 350 | | ns | |
| Address setup time | t _{AS} | 0 | | ns | |
| Write pulse width | t _{WP} | 250 | | ns | |
| Write recovery time | t _{WR} | 0 | | ns | |
| Input data setup time | t _{DW} | 150 | | ns | |
| Input data hold time | t _{DH} | 0 | | ns | |
| $\overline{\text{WE}}$ High to output in Low-Z | t _{OW} | 10 | | ns | 1 |
| $\overline{\text{WE}}$ Low to output in High-Z | t _{WZ} | 0 | 60 | ns | 1 |
| $\overline{\text{OE}}$ High to output in High-Z | t _{OHZ} | 0 | 60 | ns | 1 |

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a $\pm 200\text{ mV}$ transition from steady state levels into the test load.

TEST CONDITIONS

| PARAMETER | MODE | NOTE |
|----------------------------|-----------------|------|
| Input pulse levels | 0 V to V_{CC} | |
| Input rise/fall times | 10 ns | |
| Input/output timing levels | 1.5 V | |
| Output load | C_L (100 pF) | 1 |

NOTE:

- Includes scope and jig capacitance.

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|-------------------|-----------|------------------------|------|------|------|------|------|
| Input capacitance | C_{IN} | $V_{IN} = 0\text{ V}$ | | | 7 | pF | 1 |
| I/O capacitance | $C_{I/O}$ | $V_{I/O} = 0\text{ V}$ | | | 10 | pF | 1 |

NOTE:

- This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS ($T_A = -10^\circ\text{C}$ to $+70^\circ\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | MAX. | UNIT | NOTE |
|-------------------------------|------------|---|----------|------|---------------|------|
| Data retention supply voltage | V_{CCDR} | $\overline{CE} \geq V_{CCDR} - 0.2 \text{ V}$ | 2.0 | 3.6 | V | |
| Data retention supply current | I_{CCDR} | $V_{CCDR} = 3.0 \text{ V}$ $\overline{CE} \geq V_{CCDR} - 0.2 \text{ V}$ | | 20 | μA | |
| Chip enable setup time | t_{CDR} | | 0 | | ns | |
| Chip enable hold time | t_R | | t_{RC} | | ns | 1 |

NOTE:

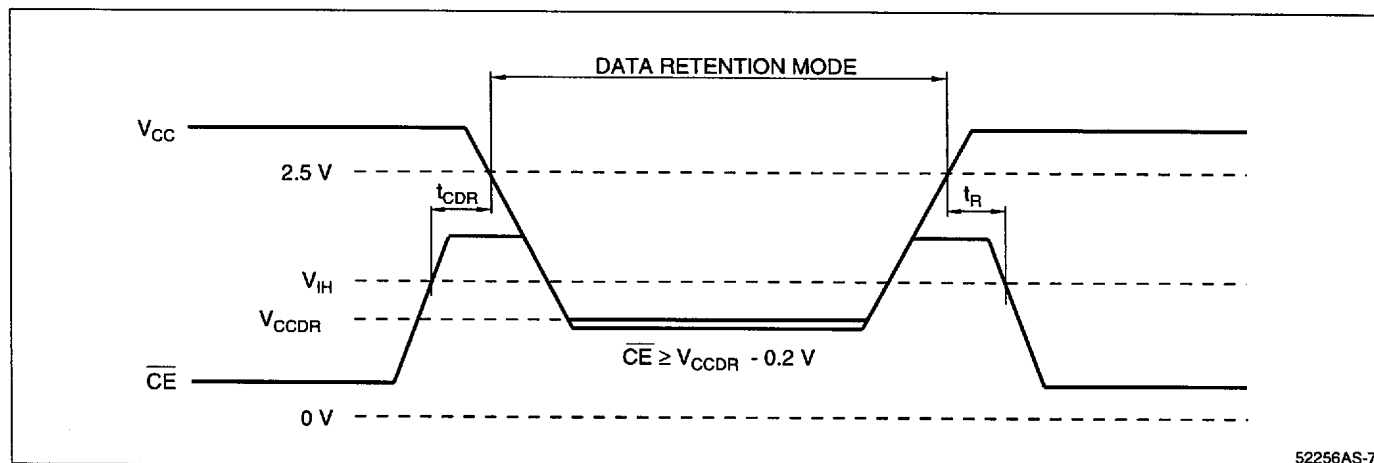
1. t_{RC} = Read cycle time.

Figure 4. Low Voltage Data Retention

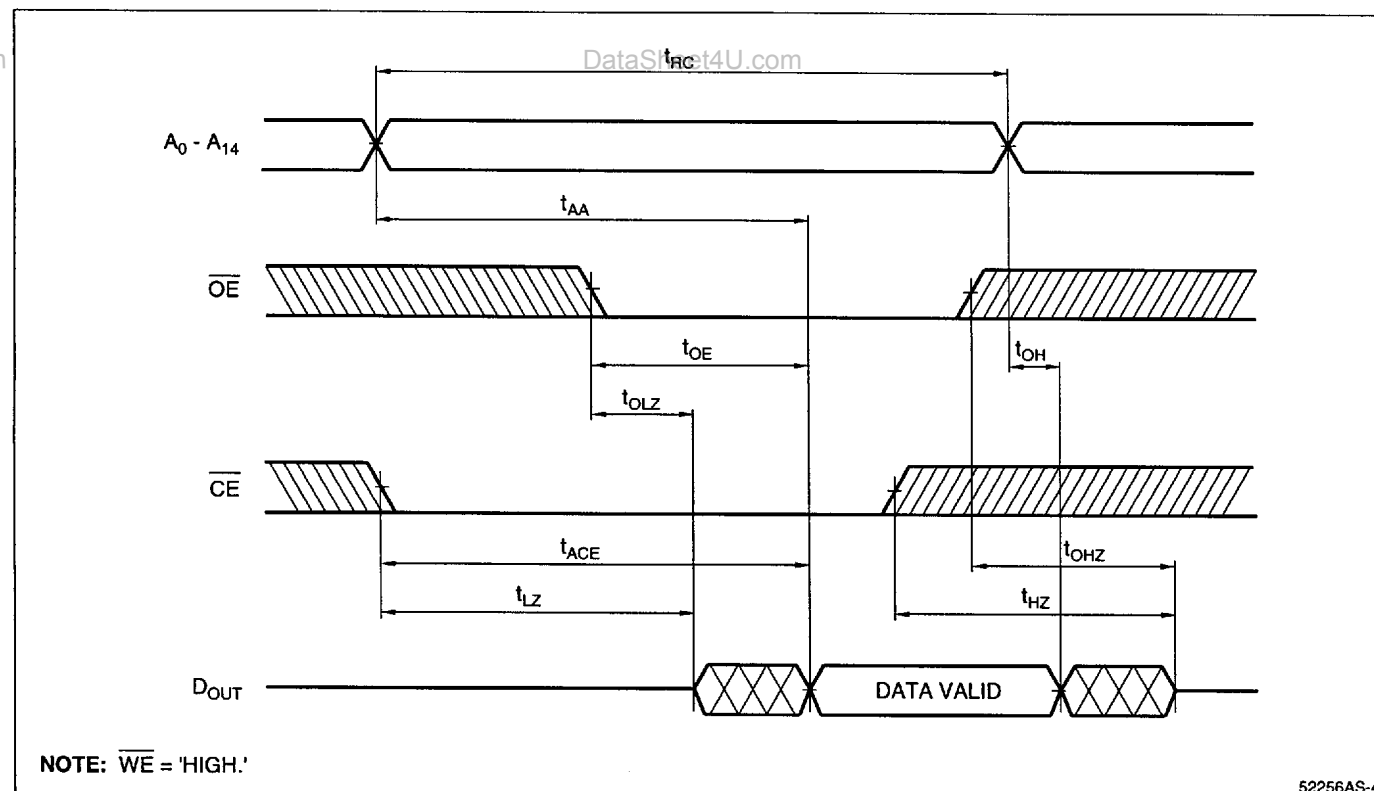
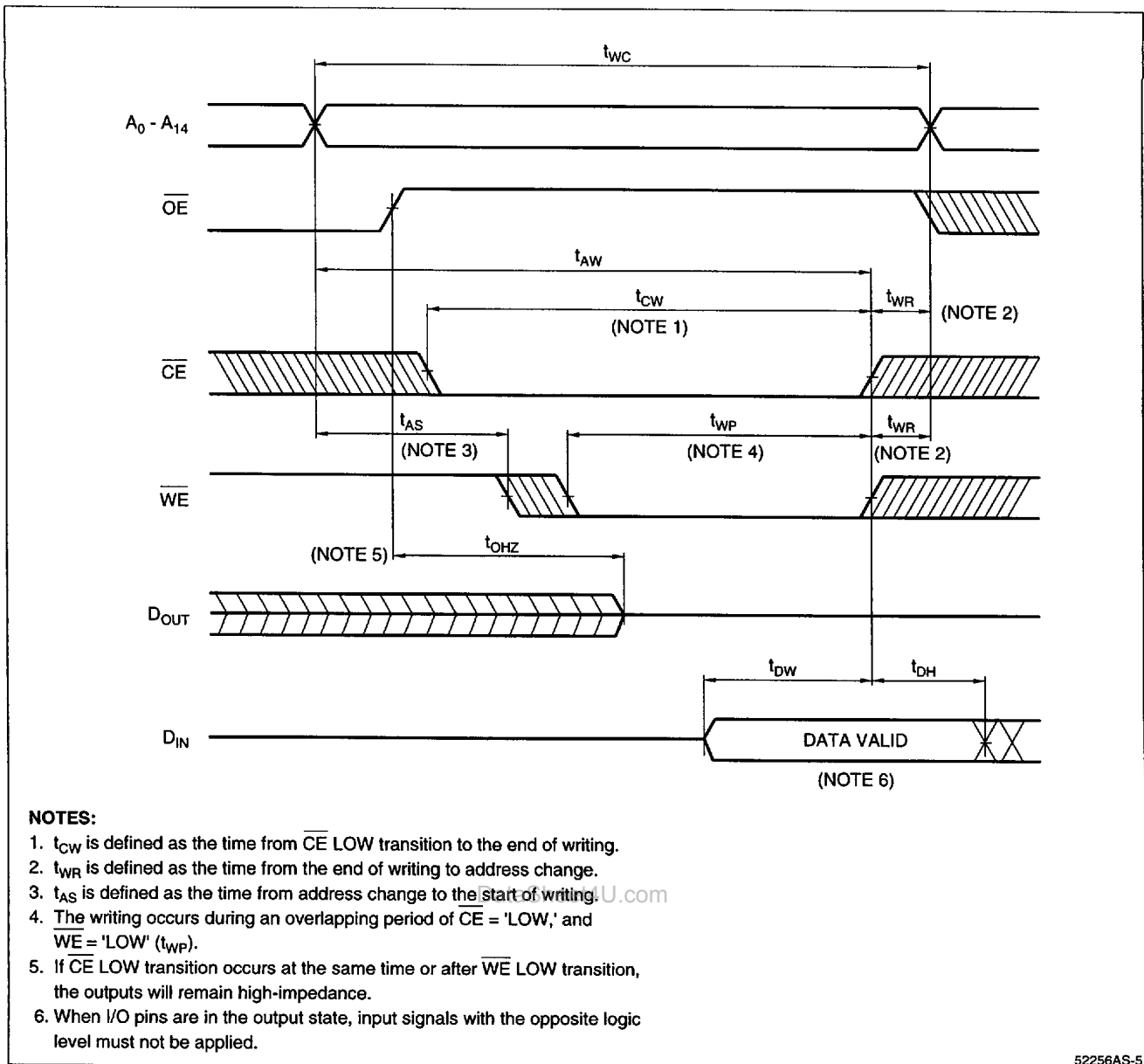
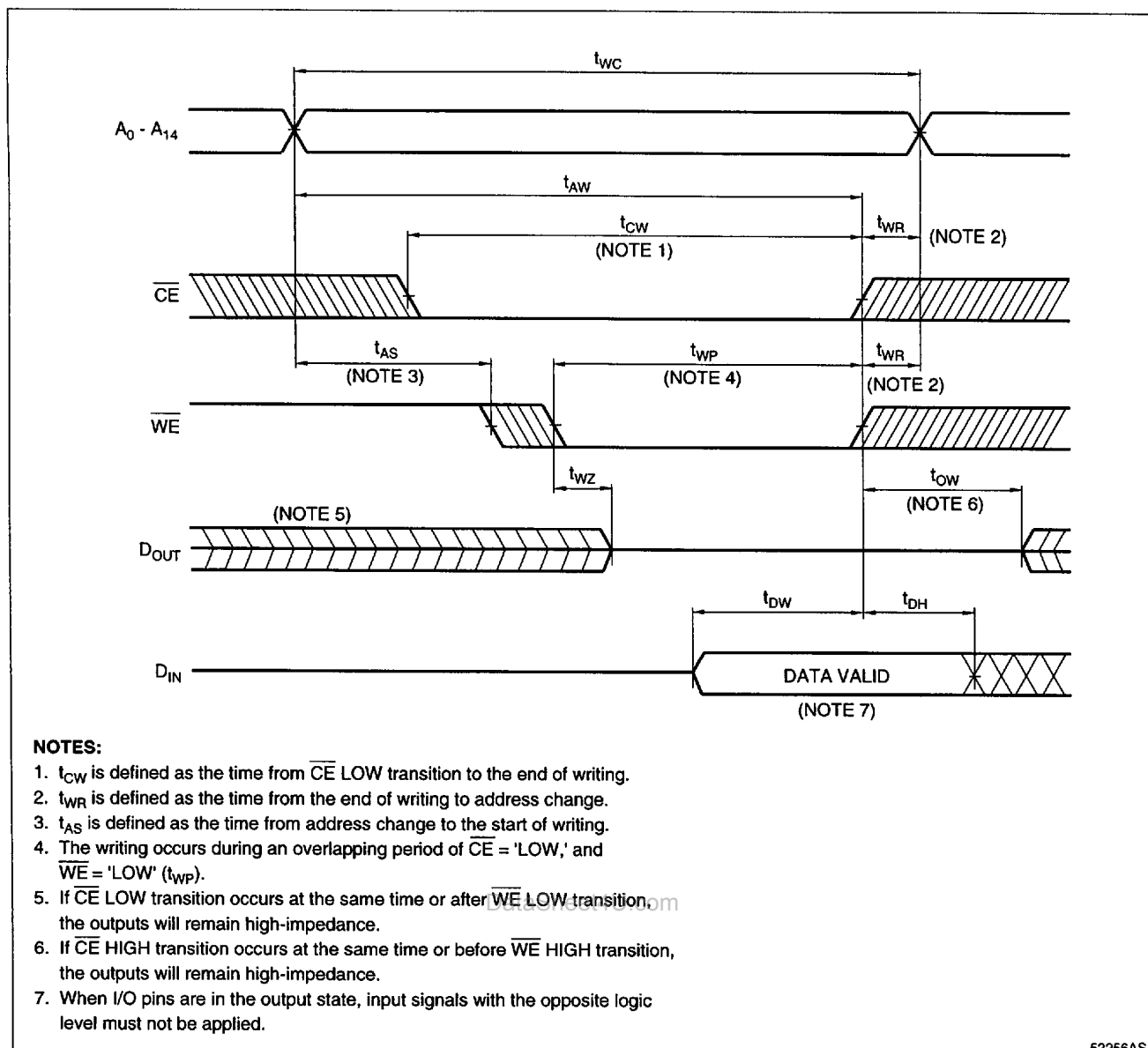
NOTE: \overline{WE} = 'HIGH.'

Figure 5. Read Cycle



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Figure 6. Write Cycle (\overline{OE} Controlled)

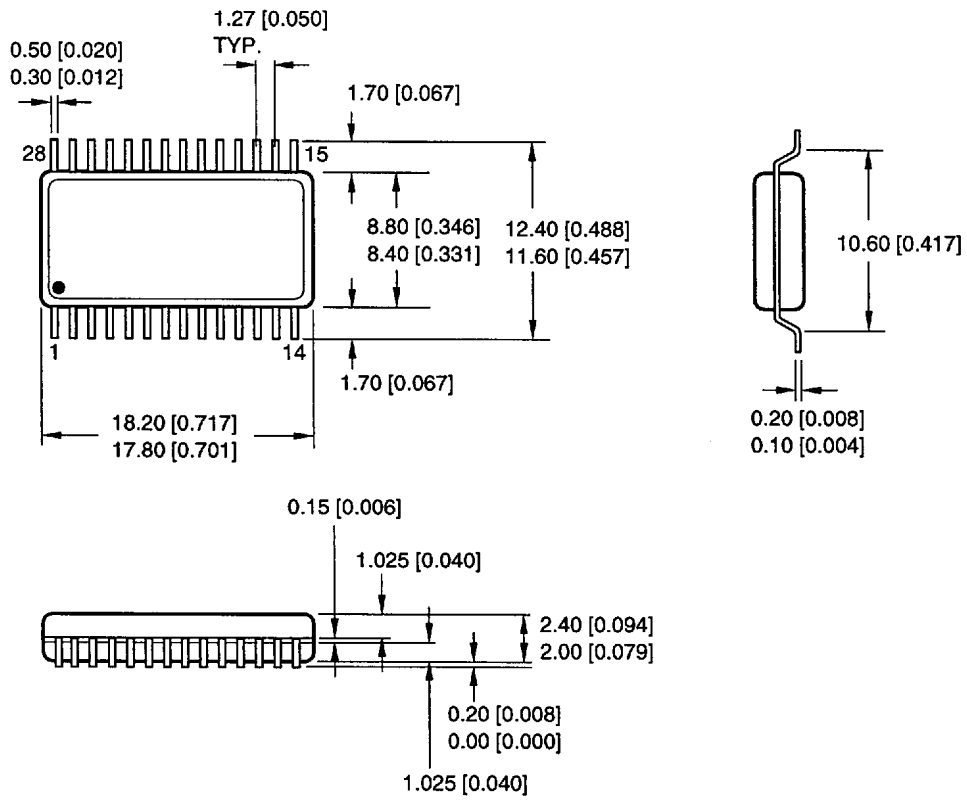


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Figure 7. Write Cycle (\overline{OE} Low Fixed)

PACKAGE DIAGRAMS

28SOP (SOP028-P-0450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

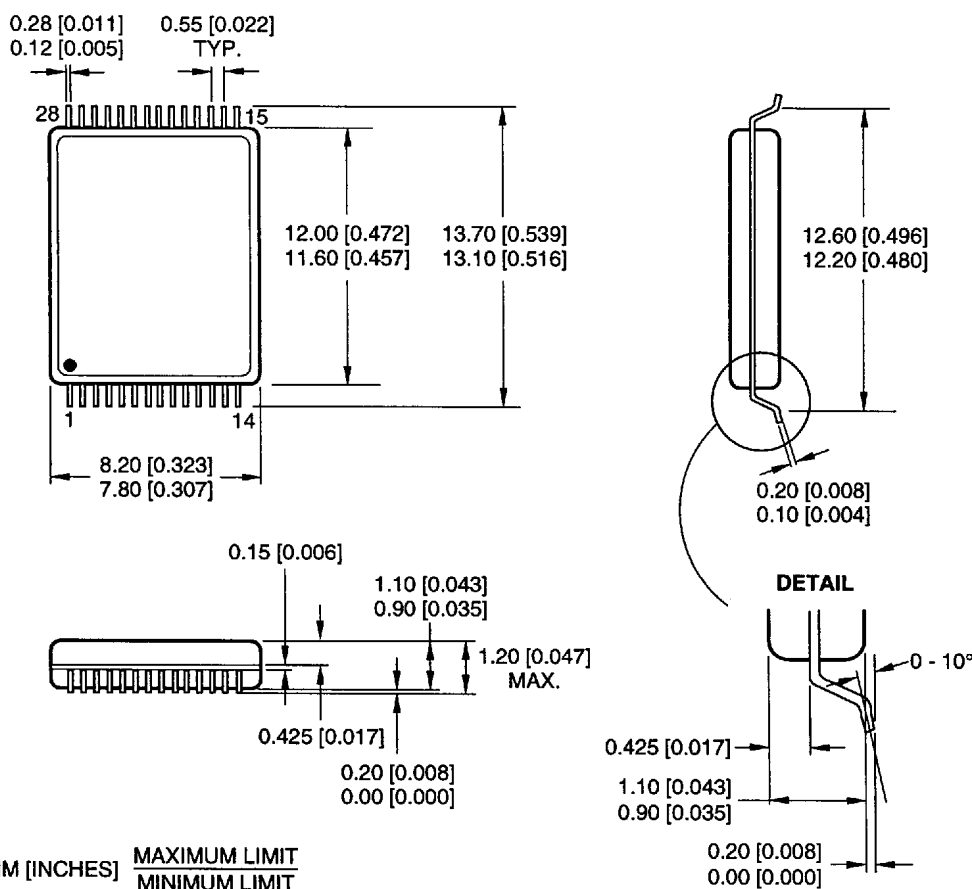
DataSheet4U.com

DataSheet4U.com

28SOP

28-pin, 450-mil SOP

28TSOP (TSOP028-P-0813)



28TSOP

28-pin, 8 × 13 mm² TSOP (Type I)

ORDERING INFORMATION

LH52256AS
Device TypeX
Package

{ N 28-pin, 450-mil SOP (SOP028-P-0450)
T 28-pin, 8 x 13 mm² TSOP (Type I) (TSOP028-P-0813)

CMOS 256K (32K x 8) Static RAM

Example: LH52256ASN (CMOS 256K (32K x 8) Static RAM, 28-pin, 450-mil SOP)

5168V-8