



UM6164 Series

PRELIMINARY

8K × 8 High Speed CMOS SRAM

Features

- Single +5 volt power supply
- Access times: 20/25/30 ns (max.)
- Current:
 - Standard version: Operating: 170 mA (max.)
 - Standby: 2 mA (max.)
 - Low power version: Operating: 170 mA (max.)
 - Standby: 100 μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Output enable and two chip select inputs for easy application
- Data retention voltage: 2V (min.) for low power version
- Available in 28 pin SOP, or Skinny DIP packages (See ordering information)

General Description

The UM6164 is a high speed, low-power 8,192-word by 8-bit CMOS static RAM. It is fabricated using UMC's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques yields access times as fast as 20 ns.

When \overline{CS}_1 is high or CS_2 is low (de-select), the device assumes a standby mode at which the power dissipation

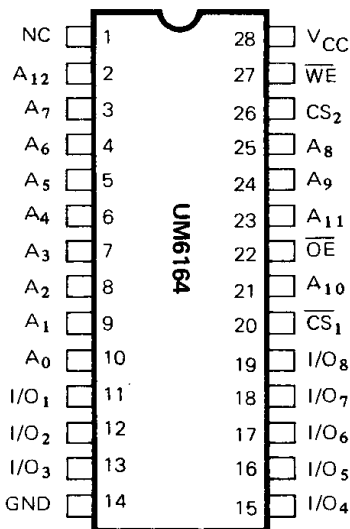
can be reduced to 25 μW (typical) at CMOS input levels.

Easy memory expansion is provided by using two Chip Select inputs \overline{CS}_1 and CS_2 . The active low Write Enable controls both writing and reading of the memory.

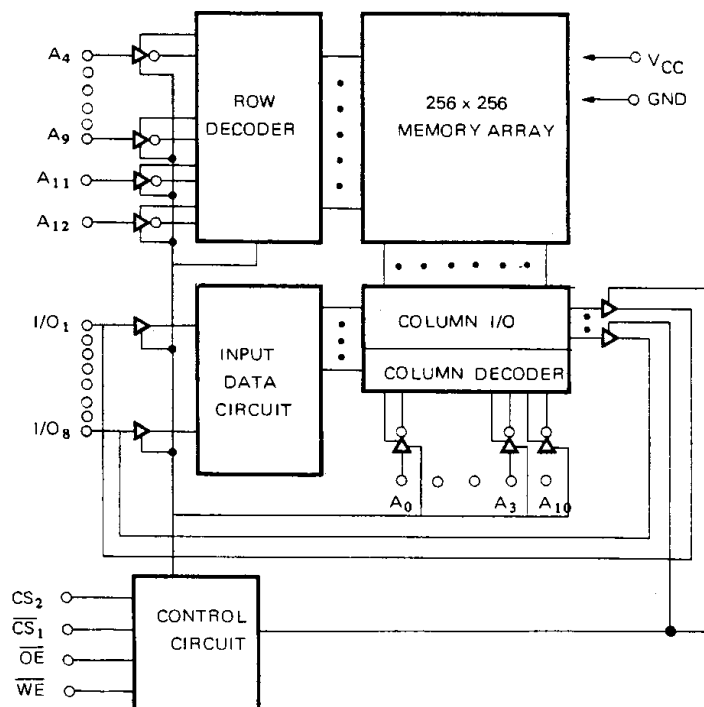
The UM6164 is pin compatible with 2764 type EPROM's and other 8K × 8 SRAM's.

High Speed SRAM

Pin Configuration



Block Diagram



Pin Description

Designation	Description
A ₀ – A ₁₂	Address Input
\overline{WE}	Write Enable
\overline{OE}	Output Enable
CS ₁	Chip Select
CS ₂	Chip Select
NC	No Connection
I/O ₁ – I/O ₈	Data Input/Output
V _{CC}	Power Supply (+5V)
GND	Ground

Recommended DC Operating Conditions

 (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	3.5	V _{CC} + 0.5V	V
V _{IL}	Input Low Voltage	-0.3	0	+0.8	V

Absolute Maximum Ratings *

V_{CC} to GND -0.5V to +7.0V
 IN, IN/OUT Voltage to GND -0.5V to V_{CC}+0.5V
 Operating Temperature, T_{opr} 0°C to +70°C
 Storage Temperature, T_{stg} -55°C to +125°C
 Temperature Under Bias, T_{bias} -10°C to +85°C
 Power Dissipation, P_T 1.0W/SOP 0.7W
 Soldering Temp. & Time 260°C, 10 sec

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Symbol	Parameter	UM6164-20/20L		UM6164-25/25L		UM6164-30/30L		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
I _{LI}	Input Leakage Current	-	2	-	2	-	2	μA	V _{IN} = GND to V _{CC}
I _{LO}	Output Leakage Current	-	2	-	2	-	2	μA	CS ₁ = V _{IH} or CS ₂ = V _{IL} or OE = V _{IH} or WE = V _{IL} V _{I/O} = GND to V _{CC}
I _{CC}	Active Power Supply Current	-	140	-	120	-	105	mA	CS ₁ = V _{IL} , CS ₂ = V _{IH} I _{I/O} = 0 mA
I _{CC1}	Dynamic Operating Current	-	170	-	145	-	125	mA	Min. Cycle, Duty = 100% CS ₁ = V _{IL} , CS ₂ = V _{IH} I _{I/O} = 0 mA
I _{SB}	Standby Power Supply Current	-	30	-	25	-	20	mA	CS ₁ = V _{IH} or CS ₂ = V _{IL}
I _{SB1}		-	2 ⁽¹⁾	-	2 ⁽¹⁾	-	2 ⁽¹⁾	mA	CS ₁ ≥ V _{CC} - 0.2V, CS ₂ ≥ V _{CC} - 0.2V,
		-	100 ⁽²⁾	-	100 ⁽²⁾	-	100 ⁽²⁾	μA	V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V
I _{SB2}		-	2 ⁽¹⁾	-	2 ⁽¹⁾	-	2 ⁽¹⁾	mA	CS ₁ ≤ 0.2V, CS ₂ ≤ 0.2V
		-	100 ⁽²⁾	-	100 ⁽²⁾	-	100 ⁽²⁾	μA	V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V
V _{OL}	Output Low Voltage	-	0.4	-	0.4	-	0.4	V	I _{OL} = 8 mA
V _{OH}	Output High Voltage	2.4	-	2.4	-	2.4	-	V	I _{OH} = -4 mA

Note: 1. Standard Version 2. Low Power Version.

Truth Table

Mode	CS ₁	CS ₂	OE	WE	I/O Operation	V _{CC} Current
Standby	H	X	X	X	High Z	I _{SB} , I _{SB1}
	X	L	X	X	High Z	I _{SB} , I _{SB2}
Output Disabled	L	H	H	H	High Z	I _{CC} , I _{CC1}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: X : H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C _{IN} *	Input Capacitance		5	pF	V _{IN} = 0V
C _{I/O} *	Input/Output Capacitance		7	pF	V _{I/O} = 0V

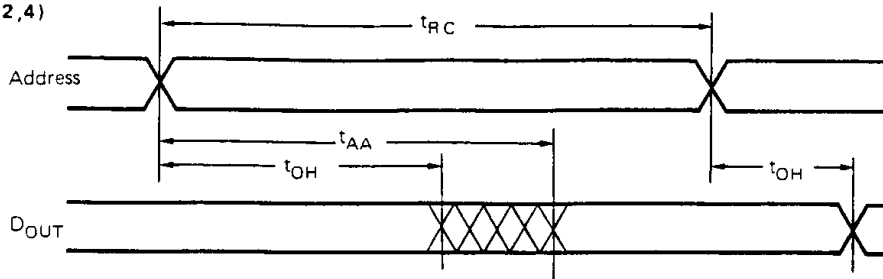
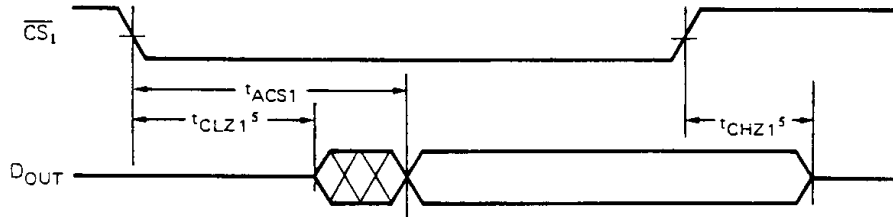
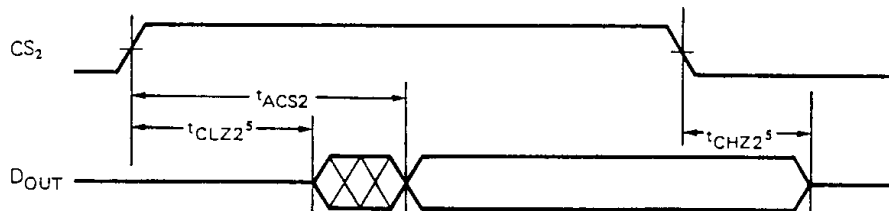
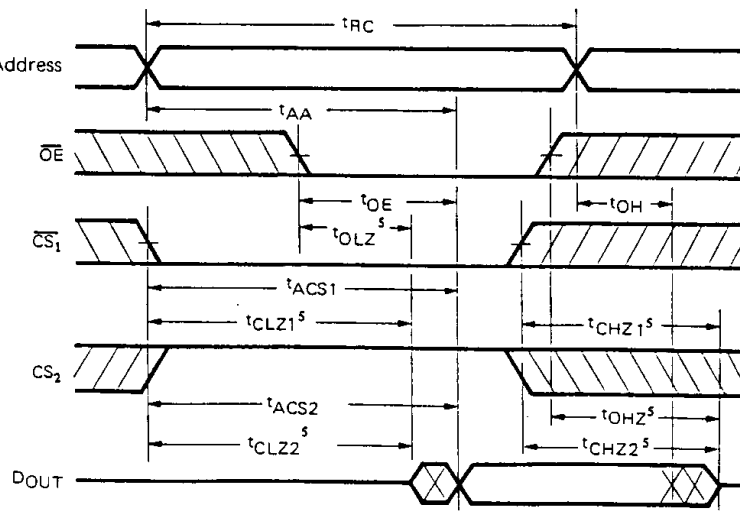
* This parameter is sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

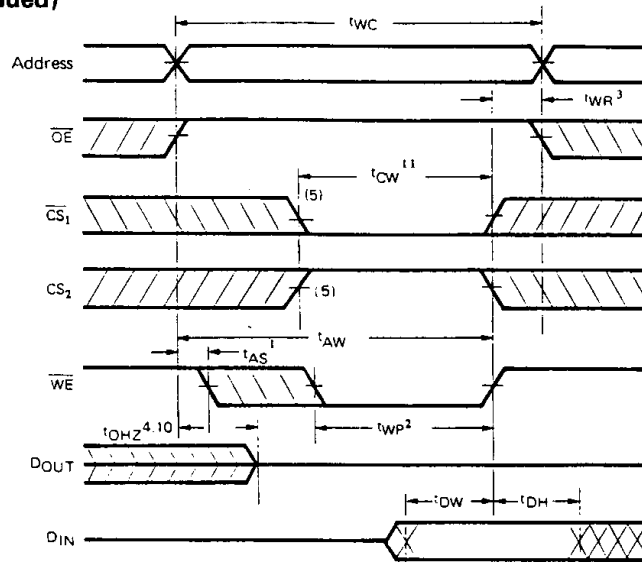
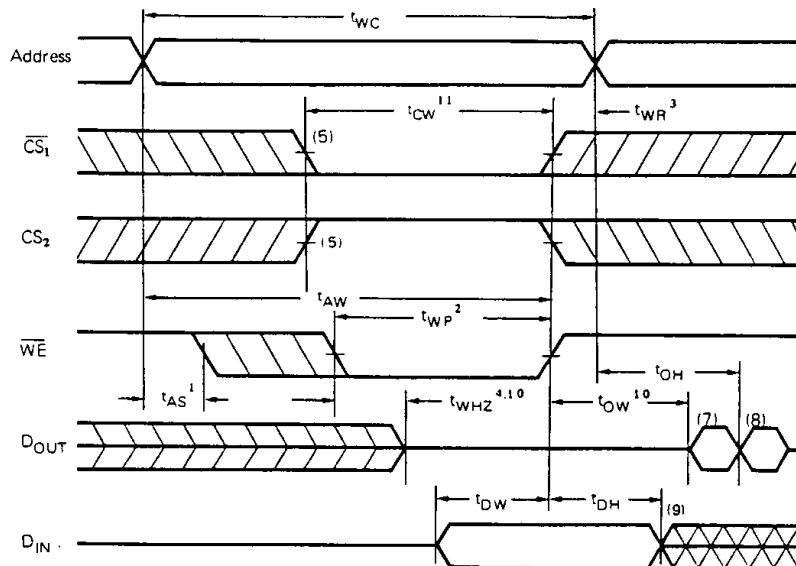
Symbol	Parameter	UM6164-20/20L		UM6164-25/25L		UM6164-30/30L		Unit		
		Min.	Max.	Min.	Max.	Min.	Max.			
Read Cycle										
t _{RC}	Read Cycle Time	20	—	25	—	30	—	ns		
t _{AA}	Address Access Time	—	20	—	25	—	30	ns		
t _{ACS1}	Chip Select Access Time	CS ₁		—	20	—	25	—	30	ns
t _{ACS2}		CS ₂		—	20	—	25	—	30	ns
t _{OE}	Output Enable to Output Valid	—	7	—	9	—	12	ns		
t _{CLZ1}	Chip Selection to Output in Low Z	CS ₁		3	—	3	—	3	—	ns
t _{CLZ2}		CS ₂		3	—	3	—	3	—	ns
t _{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	ns		
t _{CHZ1}	Chip Deselection to Output in High Z	CS ₁		0	10	0	12	0	15	ns
t _{CHZ2}		CS ₂		0	10	0	12	0	15	ns
t _{OHZ}	Output Disable to Output in High Z	0	10	0	12	0	15	ns		
t _{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns		
Write Cycle										
t _{WC}	Write Cycle Time	20	—	25	—	30	—	ns		
t _{CW}	Chip Selection to End of Write	17	—	22	—	25	—	ns		
t _{AS}	Address Set-up Time	0	—	0	—	0	—	ns		
t _{AW}	Address Valid to End of Write	15	—	22	—	25	—	ns		
t _{WP}	Write Pulse Width	12	—	15	—	18	—	ns		
t _{WR}	Write Recovery Time	0	—	0	—	0	—	ns		
t _{WHZ}	Write to Output in High Z	0	10	0	12	0	15	ns		
t _{DW}	Data to Write Time Overlap	10	—	12	—	15	—	ns		
t _{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns		
t _{OHZ}	Output Disable to Output in High Z	0	10	0	12	0	15	ns		
t _{OW}	Output Active from End of Write	0	—	0	—	0	—	ns		

Note: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

**High Speed
SRAM**

Timing Waveforms
Read Cycle 1 (1,2,4)

Read Cycle 2 (1,3,4,6)

Read Cycle 3 (1,4,7,8)

Read Cycle 4 (1)


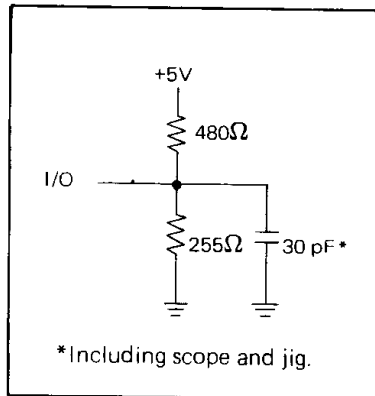
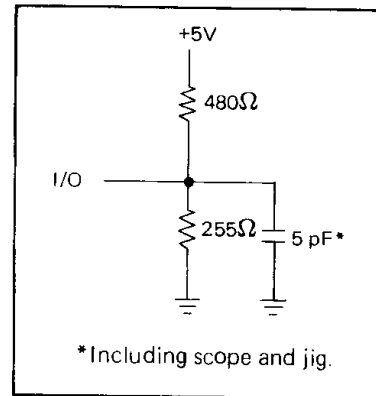
- Notes:
- \overline{WE} is high for READ cycle.
 - Device is continuously selected $\overline{CS}_1 = V_{IL}$ and $CS_2 = V_{IH}$.
 - Address valid prior to or coincident with \overline{CS}_1 transition low.
 - $\overline{OE} = V_{IL}$.
 - Transition is measured $\pm 500mV$ from steady state. This parameter is sampled and not 100% tested.
 - CS_2 is high.
 - \overline{CS}_1 is low.
 - Address valid prior to or coincident with CS_2 transition high.

Timing Waveforms (Continued)
Write Cycle 1

Write Cycle 2⁽⁶⁾


- Notes:
1. t_{AS} is measured from the address valid to the beginning of write.
 2. A write occurs during the overlap (t_{WP}) of a low \overline{CS}_1 , a high CS_2 and a low \overline{WE} .
 3. t_{WR} is measured from the earliest of \overline{CS}_1 or \overline{WE} going high or CS_2 going low to the end of write cycle.
 4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 5. If the \overline{CS}_1 low transition or the CS_2 high transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, outputs remain in a high impedance state.
 6. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$).
 7. D_{OUT} is the same phase of write data of this write cycle.
 8. D_{OUT} is the read data of next address.
 9. If \overline{CS}_1 is low and CS_2 is high during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to I/O pins.
 10. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.
 11. t_{CW} is measured from the later of \overline{CS}_1 going low or CS_2 going high to the end of write.

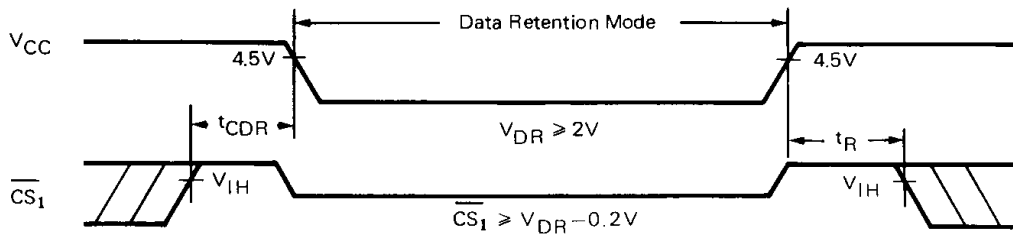
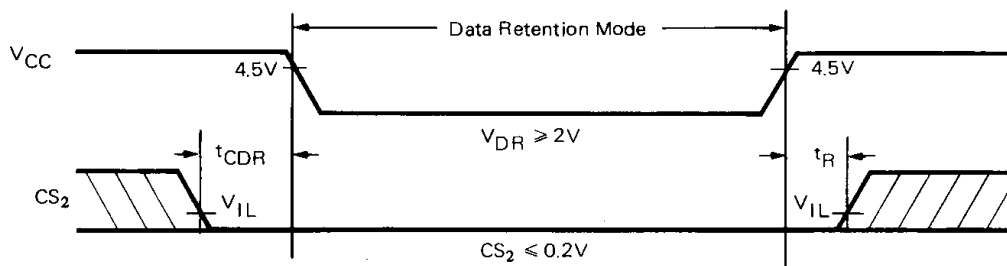
AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2


Figure 1. Output Load

**Figure 2. Output Load for t_{CLZ} ,
 t_{OLZ} , t_{CHZ} , t_{OHZ} , t_{WHZ} ,
and t_{OW}**
Data Retention Characteristics ($T_A = 0$ to $+70^\circ\text{C}$; L version only)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DR1}	V_{CC} for Data Retention	2.0	—	V	$\overline{CS}_1 \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$
V_{DR2}		2.0	—	V	$CS_2 \leq 0.2V$
I_{CCDR1}	Data Retention Current	—	100	μA	$V_{CC} = 3.0V$, $\overline{CS}_1 \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
I_{CCDR2}		—	100	μA	$\overline{CS}_1 \leq 0.2V$, $CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
t_{CDR}	Chip Deselect to Data Retention Time	0	—	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}^*	—	ns	

* t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform (\overline{CS}_1 Controlled)

Low V_{CC} Data Retention Waveform (CS_2 Controlled)

Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM6164M-20	20	170	2	28L SOP
UM6164M-20L	20	170	0.1	28L SOP
UM6164K-20	20	170	2	28L Skinny
UM6164K-20L	20	170	0.1	28L Skinny
UM6164M-25	25	145	2	28L SOP
UM6164M-25L	25	145	0.1	28L SOP
UM6164K-25	25	145	2	28L Skinny
UM6164K-25L	25	145	0.1	28L Skinny
UM6164M-30	30	125	2	28L SOP
UM6164M-30L	30	125	0.1	28L SOP
UM6164K-30	30	125	2	28L Skinny
UM6164K-30L	30	125	0.1	28L Skinny