MIL-PRF-38534 CERTIFIED

MSK

M.S.KENNEDY CORP.

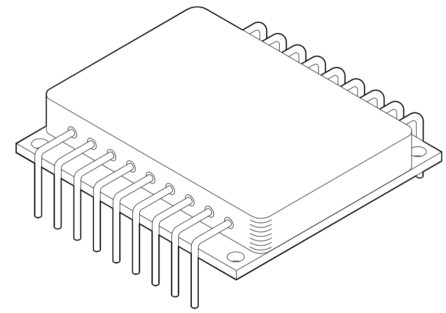
28 AMP, 500 VOLT IGBT PLUS DIODE SMART POWER 3-PHASE MOTOR DRIVE HYBRID

4357

4707 Dey Road Liverpool, N.Y. 13088 (315) 701-6751

FEATURES:

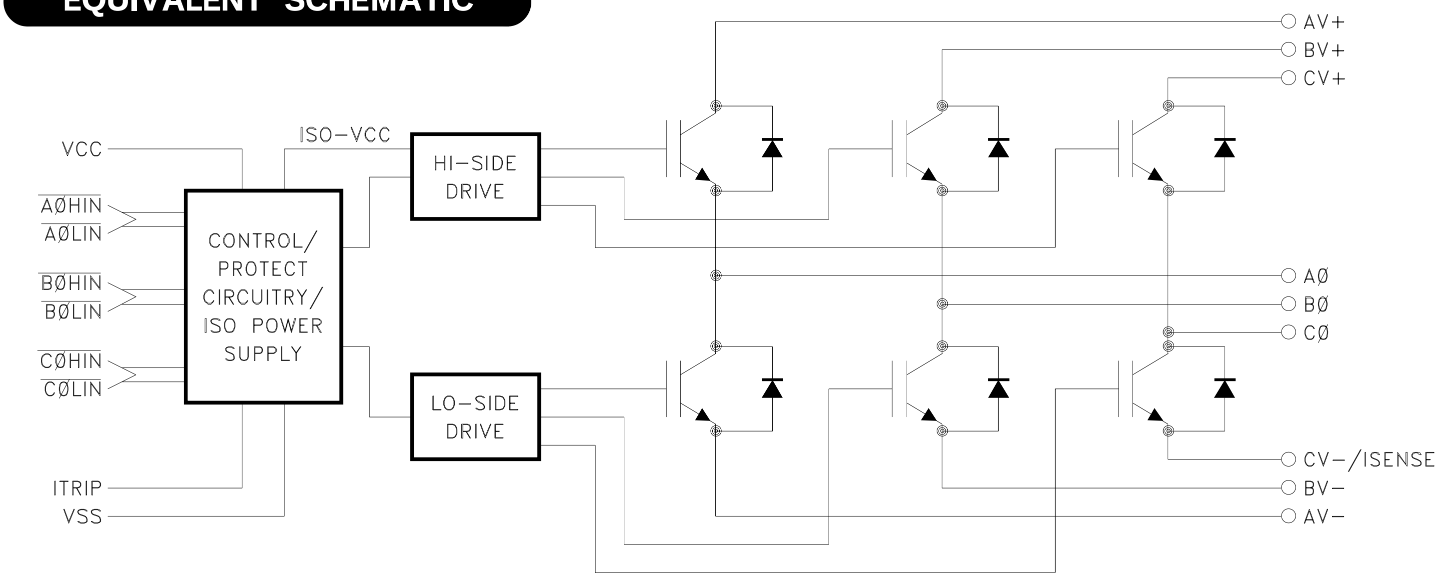
- 500V, 28 Amp Capability
- Ultra Low Thermal Resistance
- Integral Free Wheeling Fast Recovery Epitaxial Diode (FRED)
- Self-Contained, Smart Lowside/Highside Drive Circuitry
- Under-Voltage Lockout, Internal 2uS Deadtime
- Capable of Switching Frequencies to 25KHz
- Isolated Case Allows Direct Heat Sinking
- Case Bolt-down Design Allows Superior Heat Dissipation
- Contact MSK for MIL-PRF-38534 Qualification Status



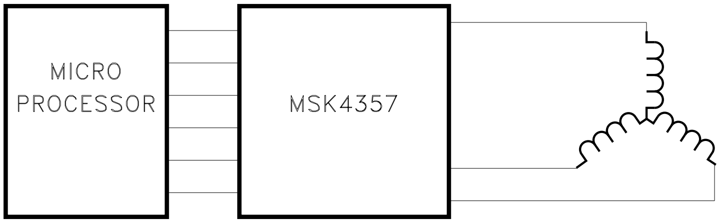
DESCRIPTION:

The MSK 4357 is a 28 Amp, 3 Phase Bridge Smart Power Motor Drive Hybrid with a 500 volt rating. The output switches are Insulated Gate Bipolar Transistors (IGBT's) tailored for high switching speeds. The free-wheeling diodes are the new Fast Recovery Epitaxial Diodes (FRED's) to provide matched current capabilities with the IGBT's and are specified with excellent reverse recovery times at high current ratings. This new smart power motor drive hybrid is compatible with 5V CMOS or TTL logic levels. The internal circuitry prevents simultaneous turn-on of the in-line half bridge transistors with a built-in 2uS deadtime to prevent shoot-through. Undervoltage lockout shuts down the bridge when the supply voltage gets to a point of incomplete turn-on of the output switches. The internal high-side power supply derived from the +15 volt supply completely eliminates the need for 3 floating independent power supplies for the high-side drive.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS



3 PHASE SIX STEP DC BRUSHLESS MOTOR DRIVE
OR 3 PHASE SINUSOIDAL INDUCTION MOTOR DRIVE

PIN-OUT INFORMATION

1	VCC	18	AV+
2	$\overline{\text{AØHIN}}$	17	AØ
3	$\overline{\text{AØLIN}}$	16	AV-
4	$\overline{\text{BØHIN}}$	15	BV+
5	$\overline{\text{BØLIN}}$	14	BØ
6	$\overline{\text{CØHIN}}$	13	BV-
7	$\overline{\text{CØLIN}}$	12	CV+
8	ITRIP	11	CØ
9	VSS	10	CV-/ISENSE

ABSOLUTE MAXIMUM RATING ⑥

- V_+ High Voltage Supply ⑦ 500V
- VCC Logic Supply 16V
- I_{OUT} Continuous Output Current 28A
- I_{PK} Peak Output Current 60A
- θ_{JC} Thermal Resistance . . . . 0.83°C/W
  (Output Switches) (Junction to Case @125°C)

- T_{ST} Storage Temperature Range -65°C to +150°C
- T_{LD} Lead Temperature Range(10 Seconds) . . . 300°C
- T_C Case Operating Temperature
  - MSK4357 . . . . -40°C to +85°C
  - MSK4357H/E . . . . -55°C to +125°C
- T_J Junction Temperature . . . . +150°C

ELECTRICAL SPECIFICATIONS

All Ratings: Tc = +25°C Unless Otherwise Specified

Parameters	Test Conditions	Group A Subgroup ⑤	MSK 4357H/E ③ Min.	Typ.	Max.	MSK 4357 ② Min.	Typ.	Max.	UNITS
OUTPUT CHARACTERISTICS									
VC-E On Voltage (Each IGBT)	$I_C = 28A$	1	-	2.3	2.7	-	2.3	2.8	V
		2	-	2.5	2.8	-	-	-	V
		3	-	2.3	2.7	-	-	-	V
Forward Voltage	$I_D = 28A$	1	-	1.7	1.9	-	1.7	2.05	V
(FRED Flyback Diode)		2	-	1.55	1.7	-	-	-	V
		3	-	1.8	2.15	-	-	-	V
Reverse Recovery Time ①	$I_D = 28A$, $di/dt = 100A/uS$, $V_r = 350V$	-	-	-	180	-	-	180	nS
Leakage Current	$V_+ = 500V$	1	-	34	400	-	34	400	uA
	$V_+ = 400V$	2	-	1.1	1.8	-	-	-	mA
	$V_+ = 500V$	3	-	19	400	-	-	-	uA
BIAS SUPPLY CHARACTERISTICS									
Quiescent Bias Current	VCC = 15V	1	-	140	180	-	140	180	mA
		2	-	105	150	-	-	-	mA
		3	-	180	220	-	-	-	mA
INPUT SIGNALS CHARACTERISTICS ①									
Positive Trigger Threshold Voltage	VCC = 15V	1,2,3	2.2	-	-	2.2	-	-	V
Negative Trigger Threshold Voltage	VCC = 15V	1,2,3	-	-	0.8	-	-	0.8	V
SWITCHING CHARACTERISTICS ①									
Upper Drive:	$V_+ = 270V$, VCC = 15V, $I_C = 28A$								
Turn-On Propagation Delay		4	-	659	1000	-	659	1000	nS
Turn-Off Propagation Delay		4	-	758	1000	-	758	1000	nS
Turn-On		4	-	38	50	-	38	50	nS
Turn-Off		4	-	60	100	-	60	100	nS
Lower Drive:	$V_+ = 270V$, VCC = 15V, $I_C = 28A$								
Turn-On Propagation Delay		4	-	656	1000	-	656	1000	nS
Turn-Off Propagation Delay		4	-	660	1000	-	660	1000	nS
Turn-On		4	-	35	50	-	35	50	nS
Turn-Off		4	-	34	50	-	34	50	nS
Dead Time		-	-	2	-	-	2	-	uS
Minimum Pulse Width		-	300	-	-	300	-	-	uS

NOTES:

① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Industrial grade and "E" suffix devices shall be tested to subgroups 1 and 4 unless otherwise specified.
③ Military grade devices ("H" suffix) shall be 100% tested to subgroups 1, 2, 3 and 4.
④ Subgroups 5 and 6 testing available upon request.
⑤ Subgroup
  - 1, 4 $T_A = T_C = +25°C$
  - 2, 5 $T_A = T_C = +125°C$
  - 3, 6 $T_A = T_C = -55°C$

⑥ Continuous operation at or above absolute maximum ratings may adversly effect the device performance and/or life cycle.
⑦ When applying power to the device, apply the low voltage followed by the high voltage or alternatively, apply both at the same time. Do not apply high voltage without low voltage present.

MSK4357 PIN DESCRIPTION

VCC - is the low voltage supply for all the internal logic and drivers. A 0.1uF ceramic capacitor in parallel with a 10uF tantalum capacitor is recommended bypassing for the VCC-VSS pins.

VSS - is the low voltage supply return pin and the input logic return reference. All logic input and logic output is referenced to this pin. This pin can vary ± 5V from the AV-,BV-,CV-/ISENSE power return pin without affecting any of the logic functions.

$\overline{\text{AØHIN}}$, $\overline{\text{BØHIN}}$, $\overline{\text{CØHIN}}$ - are low active logic inputs for signalling the corresponding phase high-side switch to turn on. The input levels are 5V **CMOS** or **TTL** compatible. Typical propagation delays are around 600nS.

$\overline{\text{AØLIN}}$, $\overline{\text{BØLIN}}$, $\overline{\text{CØLIN}}$ - are low active inputs for signalling the corresponding phase low-side switch to turn on. The input levels are 5V **CMOS** or **TTL** compatible. Typical propagation delays are around 600nS.

ITRIP - is an analog input pin for sensing current flowing from the AV-,BV-,CV-/ISENSE pin through a sense resistor to the high power ground. A 0.485 volt level at this pin with respect to **VSS** will signal an overcurrent condition and shut down all output switching. Bringing the voltage below this point (100 mV hysteresis) will remove the shutdown condition, and leaving the low-side logic inputs simultaneously high (de-activated) for 10uS will restore normal operation.

AV+,BV+,CV+ - are the connections from the tops of the three half bridges to the high voltage positive rail. Connections must be made individually from each pin to the rail, with enough current-handling capability for the load. Proper power supply bypassing must be connected to these three pins and the Vss connections for proper filtering. This bypassing must be done as close to the hybrid as possible.

AV-,BV- - are the connections from the bottoms of the AØ and BØ half bridges to the return of the high voltage negative rail. These pins should be tied to the CV-/ISENSE with as short a connection as possible.

CV-/ISENSE - is the connection from the bottom of the CØ half bridge to the return of the high voltage negative rail. There should be a connection to AV- and BV- here. If there is current sensing, then a sense resistor should go between this point and the return of the high voltage supply. If no sensing is desired, then this point should connect to Vss, the negative rail of the high voltage supply and any high voltage bypass capacitance.

AØ, BØ, CØ - are the pins connecting the 3 phase bridge switch outputs.

PROTECTION

- All logic inputs use a 300nS filter. A pulse width below this will get ignored.
- **VCC** voltage below the cutoff level of 8.65 volts will reset all switch outputs off and ignore subsequent logic inputs until **VCC** is restored.
- Undervoltage lockout of the internal drivers for the high-side switches also occurs at 8.65 volts. This may occur if the high-side output gets switched at greater than 25 kHZ without switching the low-side. The internal power supply for the high-side switch will sag too low for adequate switching. Either slow down the **PWM** rate or **PWM** the low-side switches instead.
- Switching a low-side logic input while the corresponding phase high-side logic input is activated will turn off both switches. The opposite condition is also true. This is cross-conduction lockout and will occur any time low and high-side inputs for a phase are activated at the same time.
- A 2uS deadtime is automatically inserted between high and low-side output switching to allow complete turn-off of each switch so no overlap will occur.
- An overcurrent condition detected by the **ITRIP** pin will shut down all output switches until the overcurrent condition is removed and all three low-side logic inputs are held high for 10uS, then normal operation will resume.
- **ITRIP** has a 400nS leading edge blanking time after switching to ignore any switching current transients.

TYPICAL OPERATION

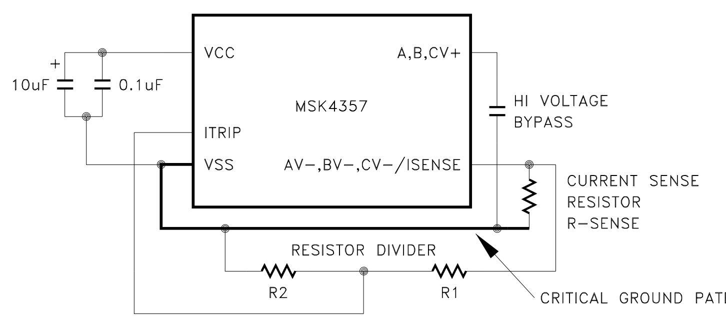
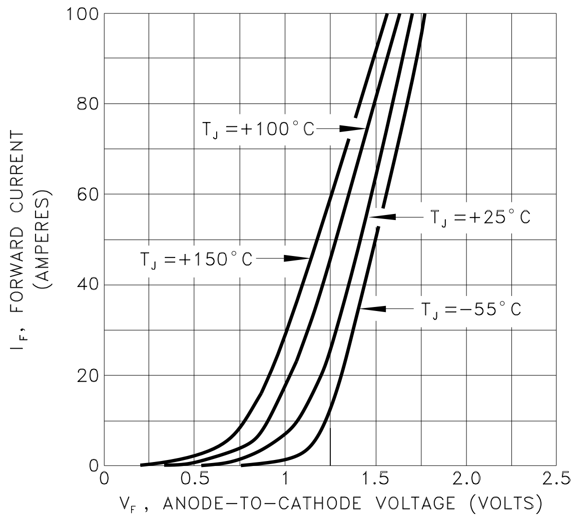


FIGURE 1
GROUNDING, BYPASSING, CURRENT SENSE

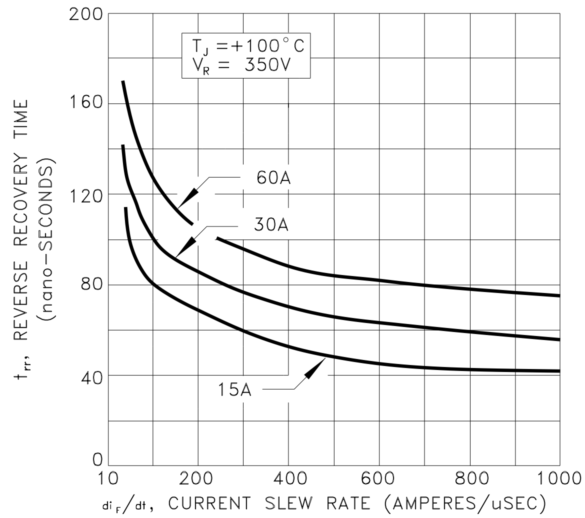
EXAMPLE:
FOR 20 AMP LIMIT:
R-SENSE = 0.050 OHMS
R-SENSE VOLT = 1 VOLT
R1 = 51.5 OHMS
R2 = 48.5 OHMS

TYPICAL PERFORMANCE CURVES

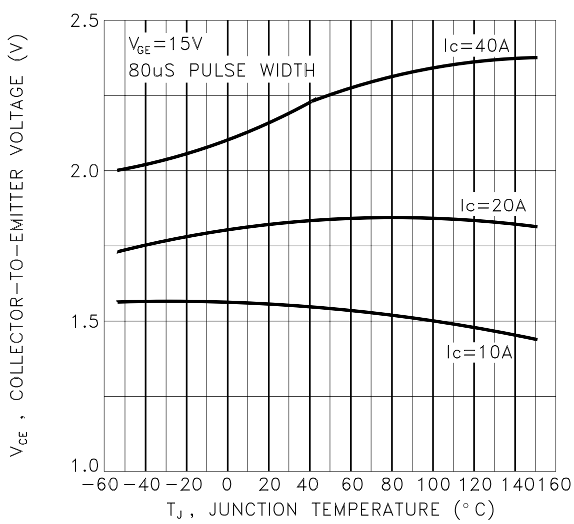
FORWARD VOLTAGE DROP vs FORWARD CURRENT



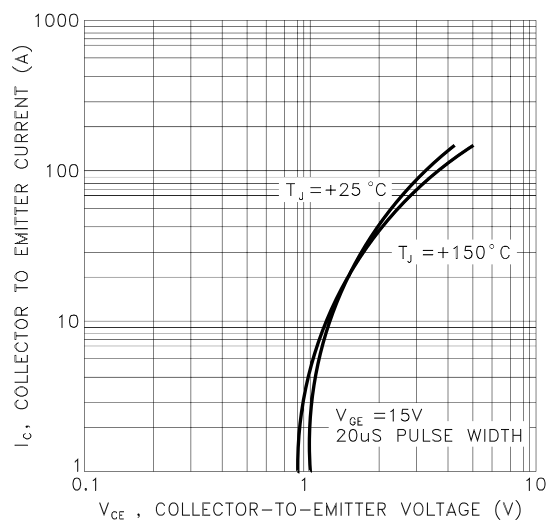
REVERSE RECOVERY TIME vs CURRENT SLEW RATE



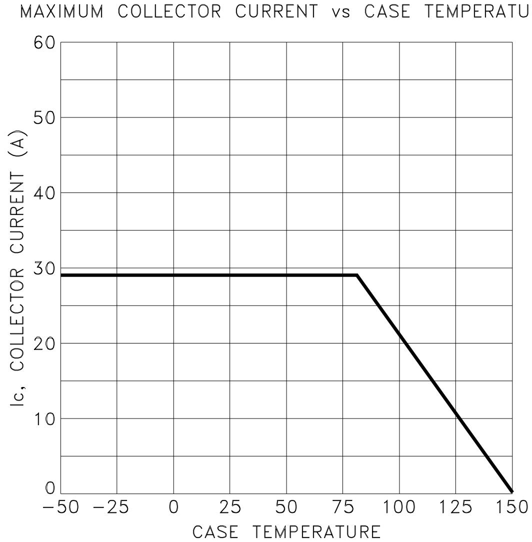
COLLECTOR TO EMITTER VOLTAGE vs. JUNCTION TEMPERATURE



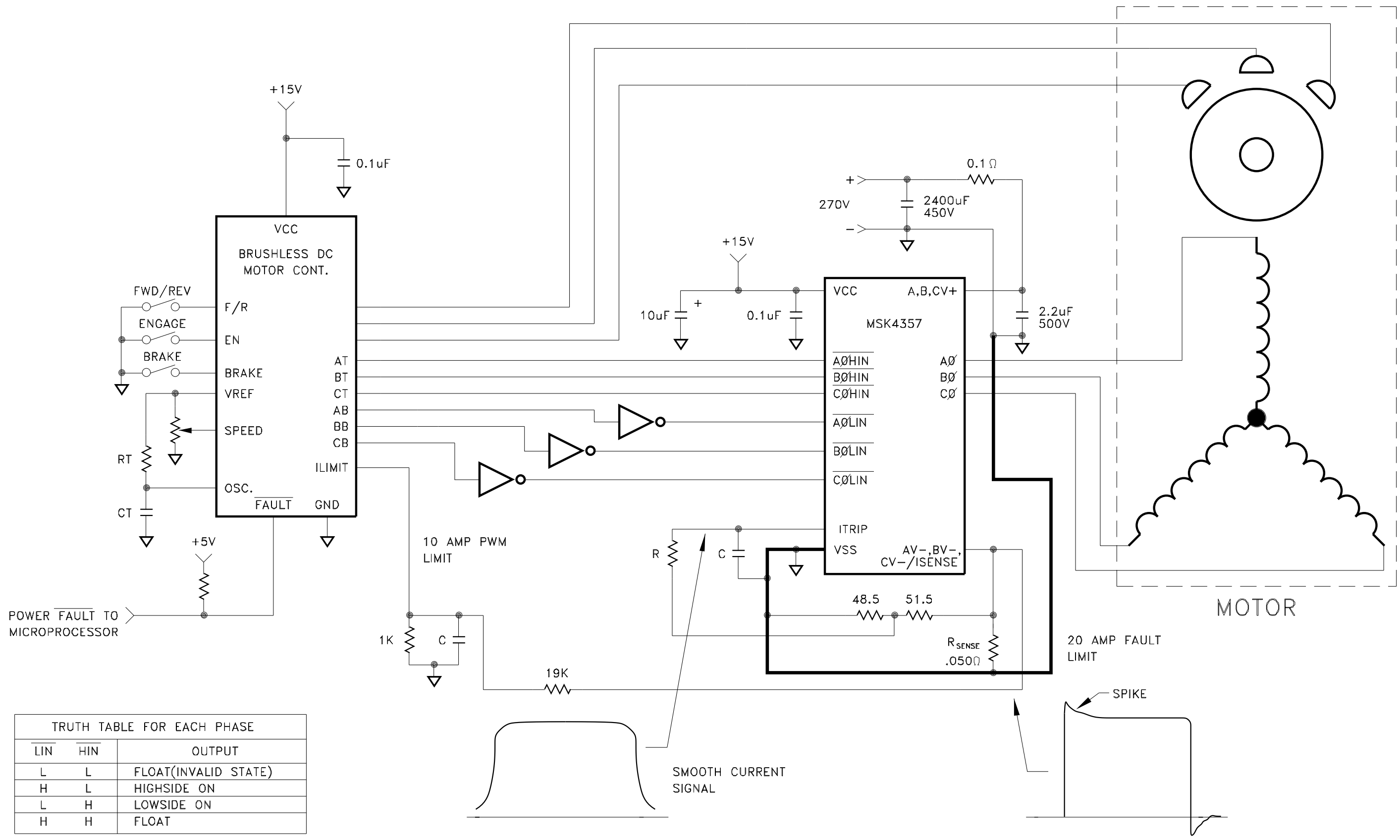
TYPICAL OUTPUT CHARACTERISTICS



MAXIMUM COLLECTOR CURRENT vs CASE TEMPERATURE



TYPICAL SYSTEM OPERATION



TRUTH TABLE FOR EACH PHASE

$\overline{LIN}$	$\overline{HIN}$	OUTPUT
L	L	FLOAT(INVALID STATE)
H	L	HIGHSIDE ON
L	H	LOWSIDE ON
H	H	FLOAT

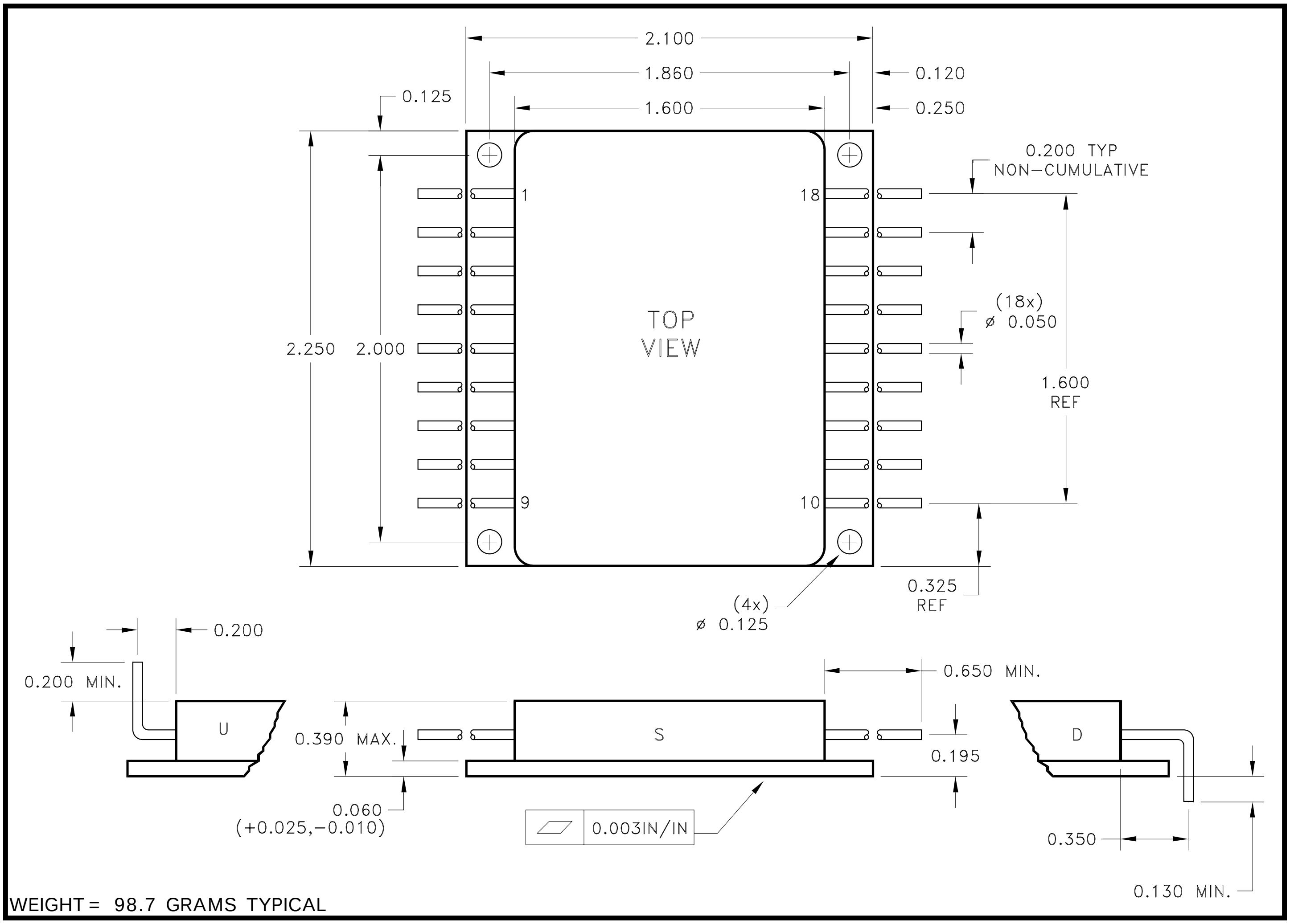
The MSK4357 is designed to be used with a +270 volt high voltage bus, +15 volt low power bus, and +5 volt logic signals. Proper derating should be applied when designing the MSK4357 into a system. High frequency layout techniques with ground planes on a printed circuit board is the only method that should be used for circuit construction. This will prevent pulse jitter caused by excessive noise pickup on the current sense signal or the error amp signal.

Ground planes for the low power circuitry and high power circuitry should be kept separate. The connection between the bottom of the current sense resistor, VSS pin and the high power ground are connected at this point. This is a critical path, and high currents should not be flowing between the current sense and VSS. Inductance in this path should be kept to a minimum. An RC filter (shown in 2 places) will filter out the current spikes and keep the detected noise for those circuits down to a minimum.

In the system shown, two types of current limit are implemented. The first limit is a PWM pulse by pulse limit controlled by the motor controller. A second absolute maximum limit is set up for the MSK4357 which will completely shut off the bridge in the event that current limit is exceeded.

The logic signals coming from the typical motor controller IC are set up for driving N channel low side and P channel high side switches directly, and are usually 15 volt levels. Provision should be made for getting 5 volt logic signals to the MSK4357 of the correct assertion levels. Typically, the low side signals out of the controller are high active and the high side are low active. Inverters are shown in the system schematic for the low side controller output.

MECHANICAL SPECIFICATIONS



ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE LABELED

ORDERING INFORMATION

MSK4357 H U

LEAD CONFIGURATION
S = STRAIGHT, U = BENT UP, D = BENT DOWN

SCREENING
BLANK = INDUSTRIAL, E = EXTENDED RELIABILITY;
H = MIL-PRF-38534 CLASS H

GENERAL PART NUMBER

THE ABOVE EXAMPLE IS A MILITARY GRADE HYBRID WITH LEADS BENT UP.

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