400MHz, 2500V/μs, 9mA Single/Dual Operational Amplifiers

FEATURES

- **400MHz Gain Bandwidth Product**
- **2500V/μs Slew Rate**
- **–85dBc Distortion at 5MHz**
- **9mA Supply Current Per Amplifier**
- 6nV/$\sqrt{Hz}$ Input Noise Voltage
- Unity-Gain Stable
- 1.5mV Maximum Input Offset Voltage
- 8μA Maximum Input Bias Current
- 800nA Maximum Input Offset Current
- 40mA Minimum Output Current, V_{OUT} = ±3V
- ±3.5V Minimum Input CMR, V_S = ±5V
- Specified at ±5V, Single 5V Supplies
- Operating Temperature Range: –40°C to 85°C
- Low Profile (1mm) TSOT-23 (ThinSOT™) Package

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Communication Receivers
- Cable Drivers
- Data Acquisition Systems

DESCRIPTION

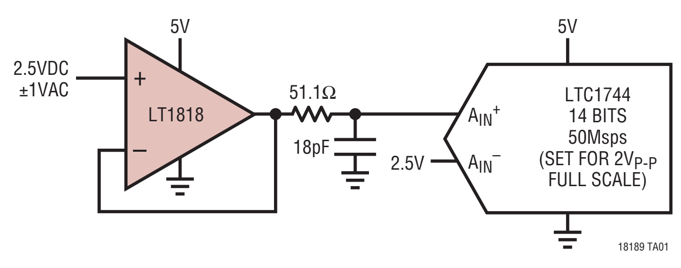
The LT®1818/LT1819 are single/dual wide bandwidth, high slew rate, low noise and distortion operational amplifiers with excellent DC performance. The LT1818/LT1819 have been designed for wider bandwidth and slew rate, much lower input offset voltage and lower noise and distortion than devices with comparable supply current. The circuit topology is a voltage feedback amplifier with the excellent slewing characteristics of a current feedback amplifier.

The output drives a 100Ω load to ±3.8V with ±5V supplies. On a single 5V supply, the output swings from 1V to 4V with a 100Ω load connected to 2.5V. The amplifier is unity-gain stable with a 20pF capacitive load without the need for a series resistor. Harmonic distortion is –85dBc up to 5MHz for a $2V_{P-P}$ output at a gain of 2.

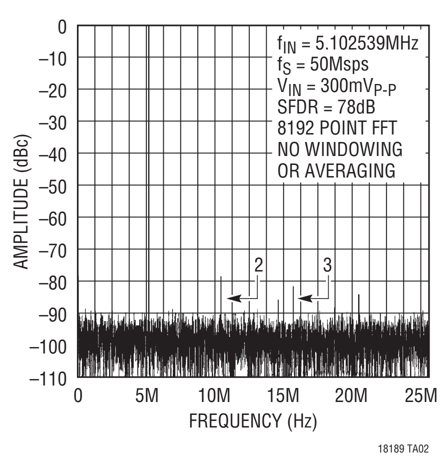
The LT1818/LT1819 are manufactured on Linear Technology's advanced low voltage complementary bipolar process. The LT1818 (single op amp) is available in TSOT-23 and SO-8 packages; the LT1819 (dual op amp) is available in MSOP-8 and SO-8 packages.

TYPICAL APPLICATION

Single Supply Unity-Gain ADC Driver for Oversampling Applications



FFT of Single Supply ADC Driver

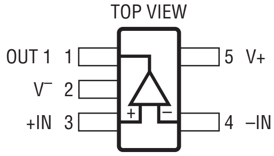


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Differential Input Voltage (Transient Only, Note 2).....±6V
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 8).... –40°C to 85°C
Specified Temperature Range (Note 9) .... –40°C to 85°C
Maximum Junction Temperature........................... 150°C
Storage Temperature Range................... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

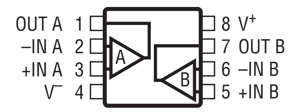
PIN CONFIGURATION

TOP VIEW



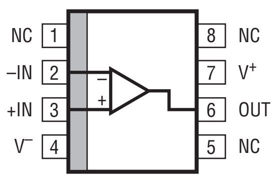
S5 PACKAGE
5-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 250°C/W (NOTE 10)

TOP VIEW



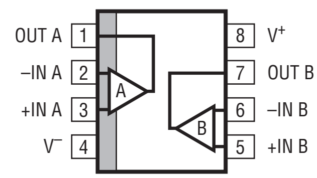
MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 250°C/W (NOTE 10)

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (NOTE 10)

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (NOTE 10)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1818CS5#PBF	LT1818CS5#TRPBF	LTF7	5-Lead Plastic TSOT-23	0°C to 70°C
LT1818IS5#PBF	LT1818IS5#TRPBF	LTF7	5-Lead Plastic TSOT-23	–40°C to 85°C
LT1818CS8#PBF	LT1818CS8#TRPBF	1818	8-Lead Plastic SO	0°C to 70°C
LT1818IS8#PBF	LT1818IS8#TRPBF	1818I	8-Lead Plastic SO	–40°C to 85°C
LT1819CMS8#PBF	LT1819CMS8#TRPBF	LTE7	8-Lead Plastic MSOP	0°C to 70°C
LT1819IMS8#PBF	LT1819IMS8#TRPBF	LTE5	8-Lead Plastic MSOP	–40°C to 85°C
LT1819CS8#PBF	LT1819CS8#TRPBF	1819	8-Lead Plastic SO	0°C to 70°C
LT1819IS8#PBF	LT1819IS8#TRPBF	1819I	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9) V_S = ±5V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4)			0.2	1.5	mV
		T_A = 0°C to 70°C	●			2.0	mV
		T_A = –40°C to 85°C	●			3.0	mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	T_A = 0°C to 70°C (Note 7)	●		10	15	μV/°C
		T_A = –40°C to 85°C (Note 7)	●		10	30	μV/°C
I_{OS}	Input Offset Current				60	800	nA
		T_A = 0°C to 70°C	●			1000	nA
		T_A = –40°C to 85°C	●			1200	nA
I_B	Input Bias Current				–2	±8	μA
		T_A = 0°C to 70°C	●			±10	μA
		T_A = –40°C to 85°C	●			±12	μA
e_n	Input Noise Voltage Density	f = 10kHz			6		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz			1.2		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = V^- + 1.5V$ to $V^+ - 1.5V$		1.5	5		MΩ
		Differential			750		kΩ
C_{IN}	Input Capacitance				1.5		pF
V_{CM}	Input Voltage Range (Positive/Negative)	Guaranteed by CMRR		±3.5	±4.2		V
		T_A = –40°C to 85°C	●	±3.5			V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3.5V		75	85		dB
		T_A = 0°C to 70°C	●	73			dB
		T_A = –40°C to 85°C	●	72			dB
	Minimum Supply Voltage	Guaranteed by PSRR			±1.25	±2	V
		T_A = –40°C to 85°C	●			±2	V
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±5.5V		78	97		dB
		T_A = 0°C to 70°C	●	76			dB
		T_A = –40°C to 85°C	●	75			dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±3V, R_L = 500Ω		1.5	2.5		V/mV
		T_A = 0°C to 70°C	●	1.0			V/mV
		T_A = –40°C to 85°C	●	0.6			V/mV
		V_{OUT} = ±3V, R_L = 100Ω		1.0	6		V/mV
		T_A = 0°C to 70°C	●	0.7			V/mV
		T_A = –40°C to 85°C	●	0.6			V/mV
	Channel Separation	V_{OUT} = ±3V, LT1819		82	100		dB
		T_A = 0°C to 70°C	●	81			dB
		T_A = –40°C to 85°C	●	80			dB
V_{OUT}	Output Swing (Positive/Negative)	R_L = 500Ω, 30mV Overdrive		±3.8	±4.1		V
		T_A = 0°C to 70°C	●	±3.7			V
		T_A = –40°C to 85°C	●	±3.6			V
		R_L = 100Ω, 30mV Overdrive		±3.50	±3.8		V
		T_A = 0°C to 70°C	●	±3.25			V
		T_A = –40°C to 85°C	●	±3.15			V
I_{OUT}	Output Current	V_{OUT} = ±3V, 30mV Overdrive		±40	±70		mA
		T_A = 0°C to 70°C	●	±35			mA
		T_A = –40°C to 85°C	●	±30			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, 1V Overdrive (Note 3)		±100	±200		mA
		T_A = 0°C to 70°C	●	±90			mA
		T_A = –40°C to 85°C	●	±70			mA
SR	Slew Rate	A_V = 1			2500		V/μs
		A_V = –1 (Note 5)		900	1800		V/μs
		TA = 0°C to 70°C	●	750			V/μs
		TA = –40°C to 85°C	●	600			V/μs
FPBW	Full-Power Bandwidth	$6V_{P-P}$ (Note 6)			95		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9) V_S = ±5V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GBW	Gain-Bandwidth Product	f = 4MHz, R_L = 500Ω T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●	270 260 250	400		MHz MHz MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V Step			0.6		ns
t_{PD}	Propagation Delay	A_V = 1, 50% to 50%, 0.1V Step			1.0		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω			20		%
t_S	Settling Time	A_V = –1, 0.1%, 5V			10		ns
HD	Harmonic Distortion	HD2, A_V = 2, f = 5MHz, V_{OUT} = $2V_{P-P}$, R_L = 500Ω HD3, A_V = 2, f = 5MHz, V_{OUT} = $2V_{P-P}$, R_L = 500Ω			–85 –89		dBc dBc
dG	Differential Gain	A_V = 2, R_L = 150Ω			0.07		%
dP	Differential Phase	A_V = 2, R_L = 150Ω			0.02		DEG
I_S	Supply Current	Per Amplifier T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●		9	10 13 14	mA mA mA

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9) V_S = 5V, 0V; V_{CM} = 2.5V, R_L to 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 4) T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●		0.4	2.0 2.5 3.5	mV mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 7) T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●		 10 10	 15 30	 μV/°C μV/°C
I_{OS}	Input Offset Current	 T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●		60	800 1000 1200	nA nA nA
I_B	Input Bias Current	 T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●		–2.4	±8 ±10 ±12	μA μA μA
e_n	Input Noise Voltage Density	f = 10kHz			6		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz			1.4		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = V^- + 1.5V to V^+ – 1.5V Differential		1.5	5 750		MΩ kΩ
C_{IN}	Input Capacitance				1.5		pF
V_{CM}	Input Voltage Range (Positive)	Guaranteed by CMRR T_A = –40°C to 85°C	 ●	3.5 3.5	4.2		V V
	Input Voltage Range (Negative)	Guaranteed by CMRR T_A = –40°C to 85°C	 ●		0.8	1.5 1.5	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = 1.5V to 3.5V T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●	73 71 70	82		dB dB dB
	Minimum Supply Voltage	Guaranteed by PSRR T_A = –40°C to 85°C	 ●		±1.25	±2 ±2	V V
PSRR	Power Supply Rejection Ratio	V_S = 4V to 11V T_A = 0°C to 70°C T_A = –40°C to 85°C	 ● ●	78 76 75	97		dB dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9) V_S = 5V, 0V; V_{CM} = 2.5V, R_L to 2.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = 1.5V to 3.5V, R_L = 500Ω		1.0	2		V/mV
		T_A = 0°C to 70°C	●	0.7			V/mV
		T_A = –40°C to 85°C	●	0.6			V/mV
		V_{OUT} = 1.5V to 3.5V, R_L = 100Ω		0.7	4		V/mV
		T_A = 0°C to 70°C	●	0.5			V/mV
		T_A = –40°C to 85°C	●	0.4			V/mV
	Channel Separation	V_{OUT} = 1.5V to 3.5V, LT1819		81	100		dB
		T_A = 0°C to 70°C	●	80			dB
		T_A = –40°C to 85°C	●	79			dB
V_{OUT}	Output Swing (Positive)	R_L = 500Ω, 30mV Overdrive		3.9	4.2		V
		T_A = 0°C to 70°C	●	3.8			V
		T_A = –40°C to 85°C	●	3.7			V
		R_L = 100Ω, 30mV Overdrive		3.7	4		V
		T_A = 0°C to 70°C	●	3.6			V
		T_A = –40°C to 85°C	●	3.5			V
	Output Swing (Negative)	R_L = 500Ω, 30mV Overdrive			0.8	1.1	V
		T_A = 0°C to 70°C	●			1.2	V
		T_A = –40°C to 85°C	●			1.3	V
		R_L = 100Ω, 30mV Overdrive			1	1.3	V
		T_A = 0°C to 70°C	●			1.4	V
		T_A = –40°C to 85°C	●			1.5	V
I_{OUT}	Output Current	V_{OUT} = 1.5V or 3.5V, 30mV Overdrive		±30	±50		mA
		T_A = 0°C to 70°C	●	±25			mA
		T_A = –40°C to 85°C	●	±20			mA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 2.5V, 1V Overdrive (Note 3)		±80	±140		mA
		T_A = 0°C to 70°C		±70			mA
		T_A = –40°C to 85°C		±50			mA
SR	Slew Rate	A_V = 1			1000		V/μs
		A_V = –1 (Note 5)		450	800		V/μs
		T_A = 0°C to 70°C	●	375			V/μs
		T_A = –40°C to 85°C	●	300			V/μs
FPBW	Full-Power Bandwidth	$2V_{P-P}$ (Note 6)			125		MHz
GBW	Gain-Bandwidth Product	f = 4MHz, R_L = 500Ω		240	360		MHz
		T_A = 0°C to 70°C	●	230			MHz
		T_A = –40°C to 85°C	●	220			MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10% to 90%, 0.1V Step			0.7		ns
t_{PD}	Propagation Delay	A_V = 1, 50% to 50%, 0.1V Step			1.1		ns
OS	Overshoot	A_V = 1, 0.1V, R_L = 100Ω			20		%
HD	Harmonic Distortion	HD2, A_V = 2, f = 5MHz, V_{OUT} = $2V_{P-P}$, R_L = 500Ω			–72		dBc
		HD3, A_V = 2, f = 5MHz, V_{OUT} = $2V_{P-P}$, R_L = 500Ω			–74		dBc
dG	Differential Gain	A_V = 2, R_L = 150Ω			0.07		%
dP	Differential Phase	A_V = 2, R_L = 150Ω			0.07		DEG
I_S	Supply Current	Per Amplifier			8.5	10	mA
		T_A = 0°C to 70°C	●			13	mA
		T_A = –40°C to 85°C	●			14	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Differential inputs of ±6V are appropriate for transient operation only, such as during slewing. Large sustained differential inputs can cause excessive power dissipation and may damage the part.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Input offset voltage is pulse tested and is exclusive of warm-up drift.

ELECTRICAL CHARACTERISTICS

Note 5: With ±5V supplies, slew rate is tested in a closed-loop gain of –1 by measuring the rise time of the output from –2V to 2V with an output step from –3V to 3V. With single 5V supplies, slew rate is tested in a closed-loop gain of –1 by measuring the rise time of the output from 1.5V to 3.5V with an output step from 1V to 4V. Falling edge slew rate is not production tested, but is designed, characterized and expected to be within 10% of the rising edge slew rate.

Note 6: Full-power bandwidth is calculated from the slew rate:

$FPBW = SR/2\pi V_P$

Note 7: This parameter is not 100% tested.

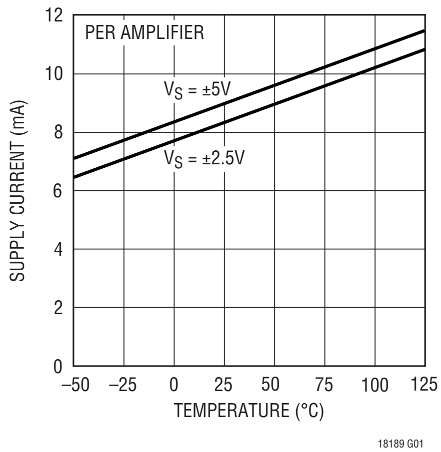
Note 8: The LT1818C/LT1818I and LT1819C/LT1819I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 9: The LT1818C/LT1819C are guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet the extended temperature limits, but is not tested at –40°C and 85°C. The LT1818I/LT1819I are guaranteed to meet the extended temperature limits.

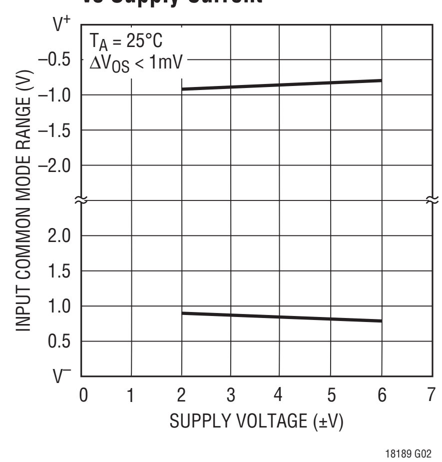
Note 10: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be significantly reduced by connecting the V^- pin to a large metal area.

TYPICAL PERFORMANCE CHARACTERISTICS

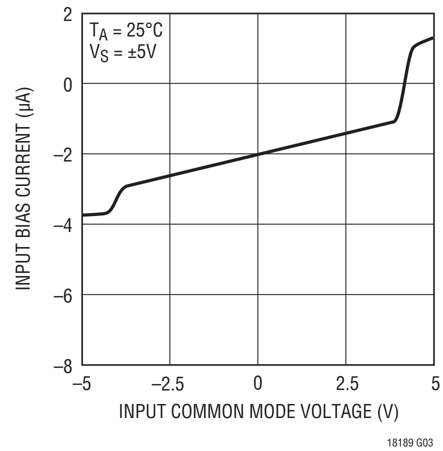
Supply Current vs Temperature



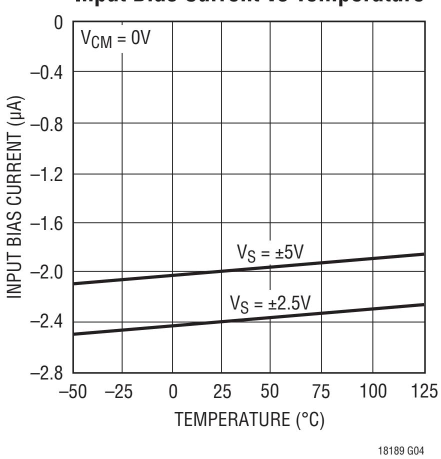
Input Common Mode Range vs Supply Current



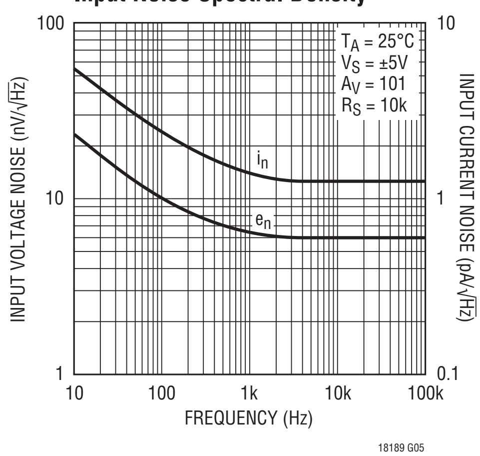
Input Bias Current vs Common Mode Voltage



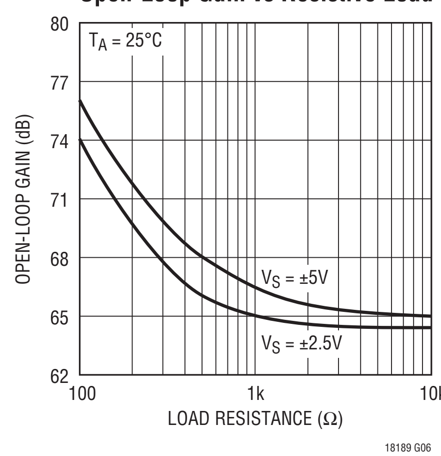
Input Bias Current vs Temperature



Input Noise Spectral Density

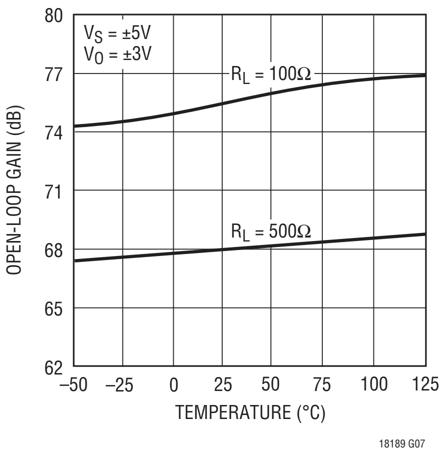


Open-Loop Gain vs Resistive Load

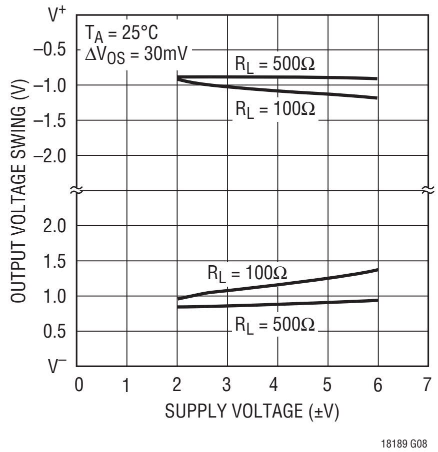


TYPICAL PERFORMANCE CHARACTERISTICS

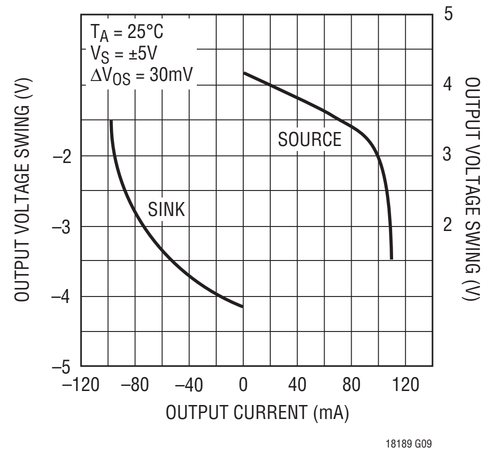
Open-Loop Gain vs Temperature



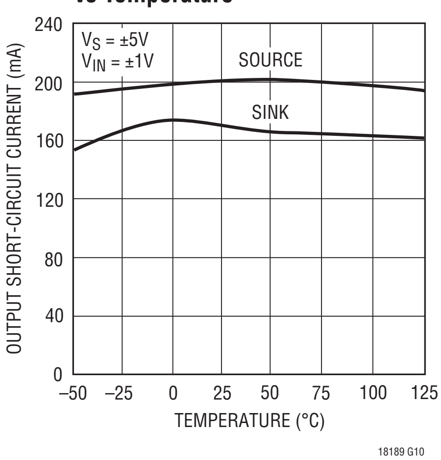
Output Voltage Swing vs Supply Voltage



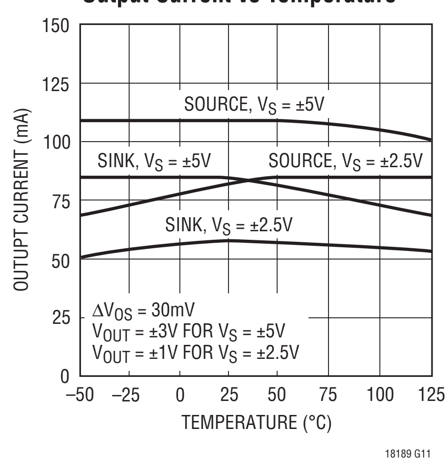
Output Voltage Swing vs Load Current



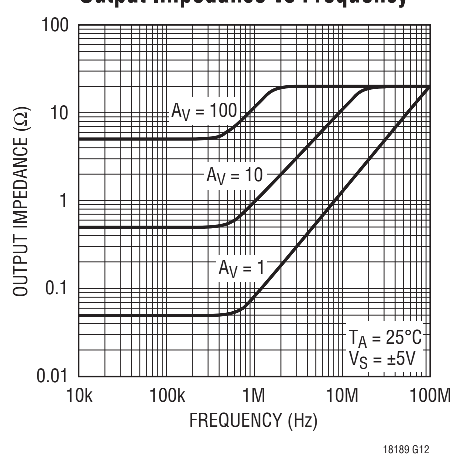
Output Short-Circuit Current vs Temperature



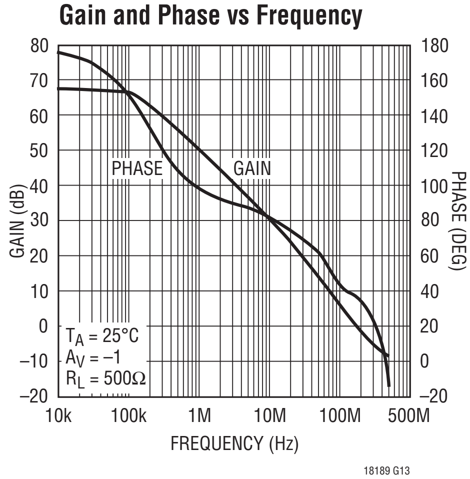
Output Current vs Temperature



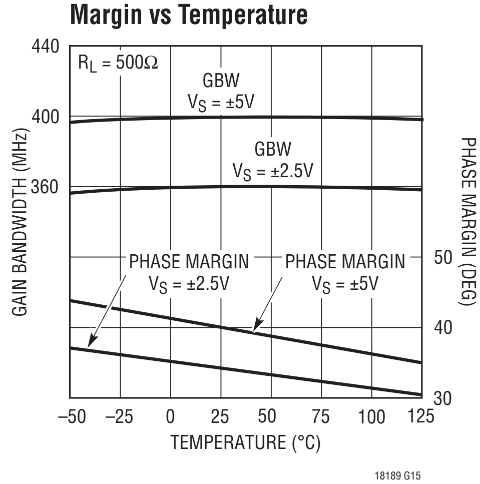
Output Impedance vs Frequency



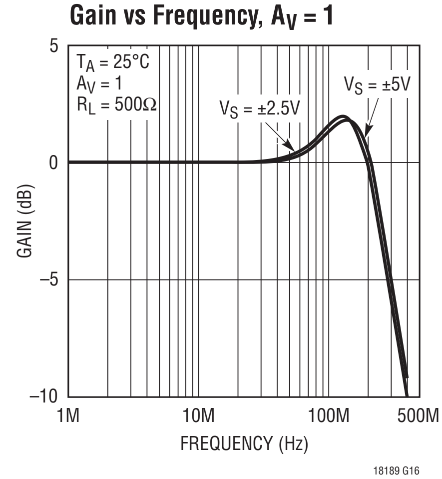
Gain and Phase vs Frequency



Gain Bandwidth and Phase Margin vs Temperature

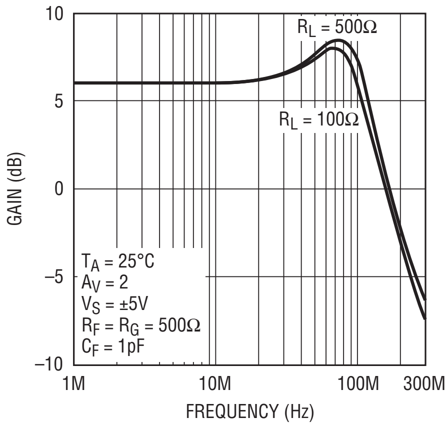


Gain vs Frequency, $A_V = 1$



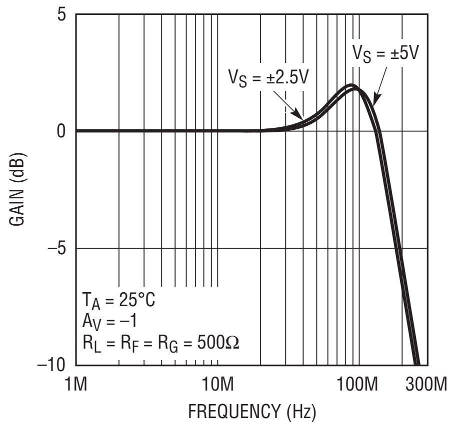
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency, $A_V = 2$



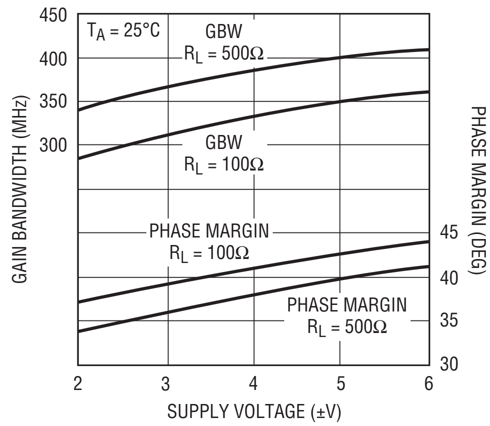
18189 G17

Gain vs Frequency, $A_V = –1$



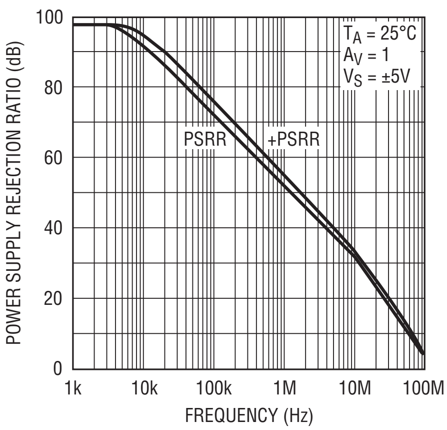
18189 G18

Gain-Bandwidth and Phase Margin vs Supply Voltage



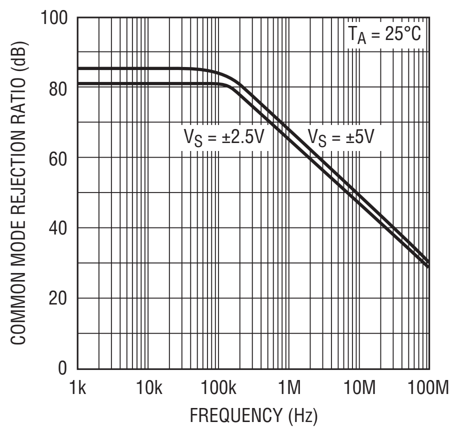
18189 G19

Power Supply Rejection Ratio vs Frequency



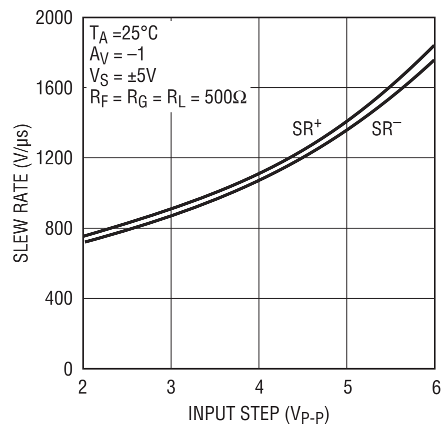
18189 G20

Common Mode Rejection Ratio vs Frequency



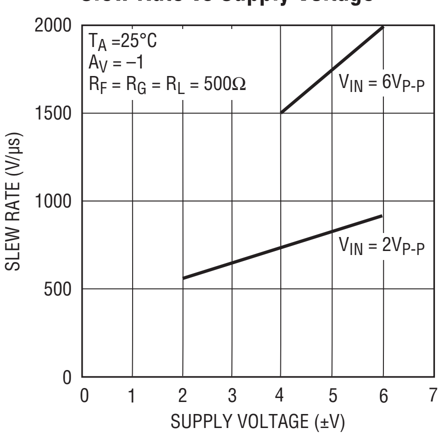
18189 G21

Slew Rate vs Input Step



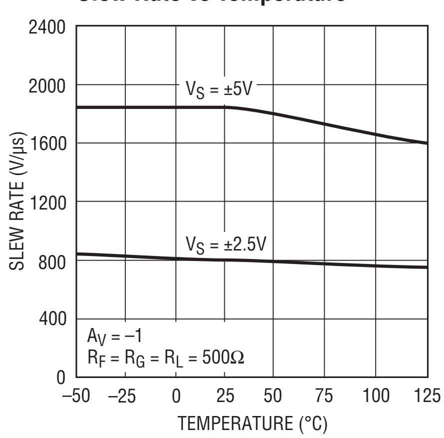
18189 G22

Slew Rate vs Supply Voltage



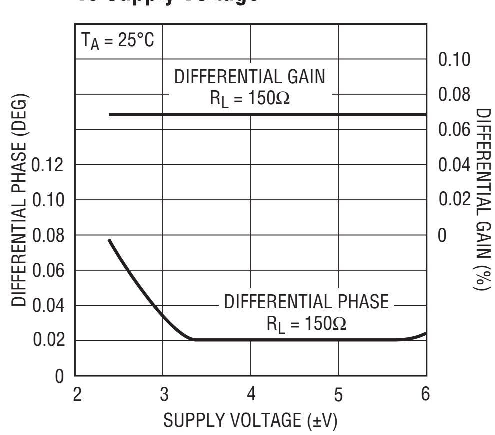
18189 G23

Slew Rate vs Temperature



18189 G24

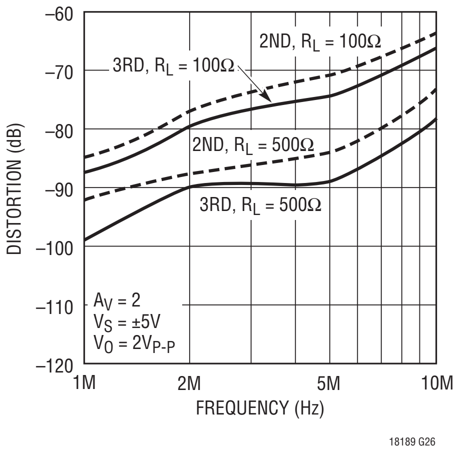
Differential Gain and Phase vs Supply Voltage



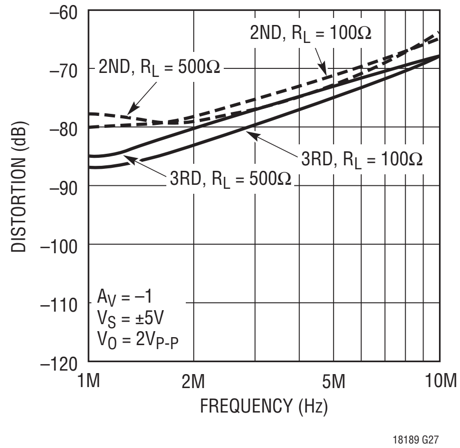
18189 G25

TYPICAL PERFORMANCE CHARACTERISTICS

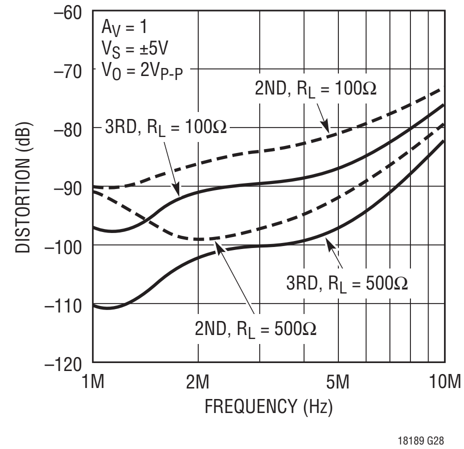
Distortion vs Frequency, $A_V = 2$



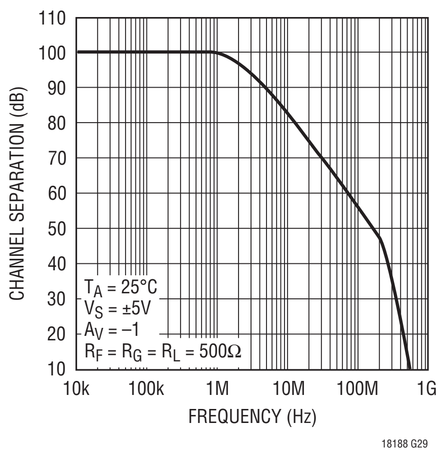
Distortion vs Frequency, $A_V = –1$



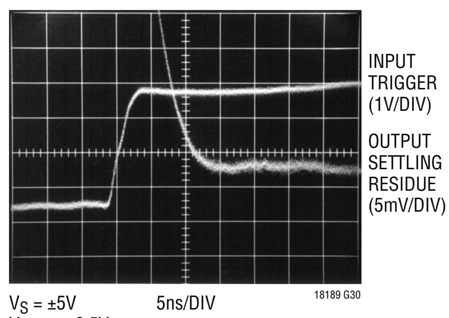
Distortion vs Frequency, $A_V = 1$



Channel Separation vs Frequency

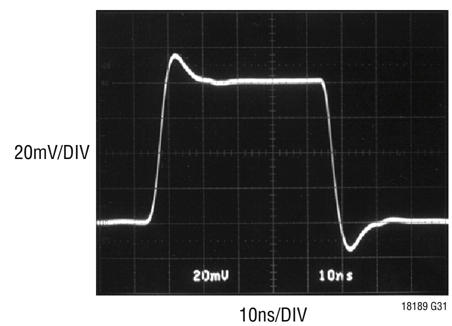


0.1% Settling Time

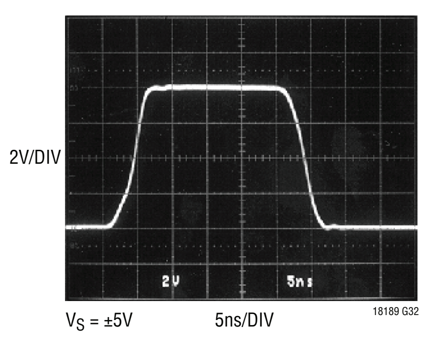


V_S = ±5V
V_{OUT} = ±2.5V
SETTLING TIME = 9ns
A_V = –1
R_F = R_G = 500Ω
C_F = 4.1pF

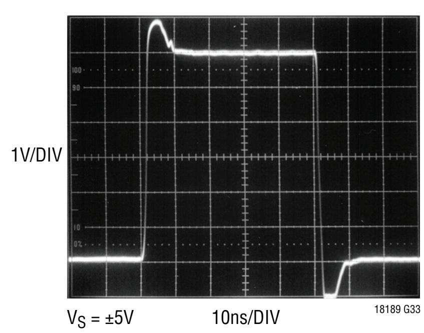
Small-Signal Transient, 20dB Gain



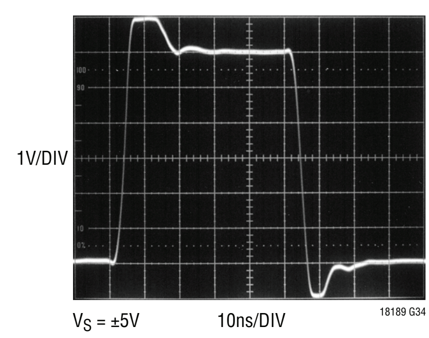
Large-Signal Transient, $A_V = –1$



Large-Signal Transient, $A_V = 1$



Large-Signal Transient, $A_V = –1$



APPLICATIONS INFORMATION

Layout and Passive Components

As with all high speed amplifiers, the LT1818/LT1819 require some attention to board layout. A ground plane is recommended and trace lengths should be minimized, especially on the negative input lead.

Low ESL/ESR bypass capacitors should be placed directly at the positive and negative supply (0.01µF ceramics are recommended). For high drive current applications, additional 1µF to 10µF tantalums should be added.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole that can cause peaking or even oscillations. If feedback resistors greater than 500Ω are used, a parallel capacitor of value

$C_F > R_G \bullet C_{IN}/R_F$

should be used to cancel the input pole and optimize dynamic performance (see Figure 1). For applications where the DC noise gain is 1 and a large feedback resistor is used, C_F should be greater than or equal to C_{IN}. An example would be an I-to-V converter.

In high closed-loop gain configurations, $R_F >> R_G$, no C_F needs to be added. To optimize the bandwidth in these applications, a capacitor, C_G, may be added in parallel with R_G in order to cancel out any parasitic C_F capacitance.

Capacitive Loading

The LT1818/LT1819 are optimized for low distortion and high gain bandwidth applications. The amplifiers can drive a capacitive load of 20pF in a unity-gain configuration and more with higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω must be connected between the output and the capacitive load to avoid ringing or oscillation (see R_S in Figure 1). The feedback must still be taken directly from the output so that the series resistor will isolate the capacitive load to ensure stability.

Input Considerations

The inputs of the LT1818/LT1819 amplifiers are connected to the bases of NPN and PNP bipolar transistors in parallel. The base currents are of opposite polarity and provide first order bias current cancellation. Due to variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current, however, does not depend on beta matching and is tightly controlled. Therefore, the use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. For example, with a 100Ω source resistance at each input, the 800nA maximum offset current results in only 80µV of extra offset, while without balance the 8µA maximum input bias current could result in an 0.8mV offset condition.

The inputs can withstand differential input voltages of up to 6V without damage and without needing clamping or series resistance for protection. This differential input voltage generates a large internal current (up to 50mA), which results in the high slew rate. In normal transient closed-loop operation, this does not increase power dissipation significantly because of the low duty cycle of the transient inputs. Sustained differential inputs, however, will result in excessive power dissipation and therefore **this device should not be used as a comparator.**

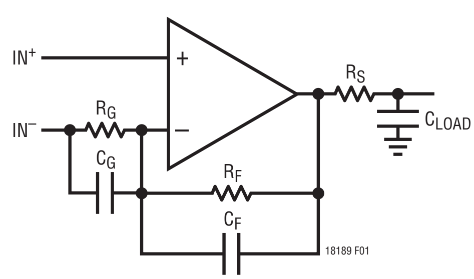


Figure 1

APPLICATIONS INFORMATION

Slew Rate

The slew rate of the LT1818/LT1819 is proportional to the differential input voltage. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 6V output step with a gain of 10 has a 0.6V input step, whereas at unity gain there is a 6V input step. The LT1818/LT1819 is tested for slew rate at a gain of –1. Lower slew rates occur in higher gain configurations, whereas the highest slew rate (2500V/µs) occurs in a noninverting unity-gain configuration.

Power Dissipation

The LT1818/LT1819 combine high speed and large output drive in small packages. It is possible to exceed the maximum junction temperature specification (150°C) under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A), power dissipation per amplifier (P_D) and number of amplifiers (n) as follows:

$$T_J = T_A + (n \bullet P_D \bullet \theta_{JA})$$

Power dissipation is composed of two parts. The first is due to the quiescent supply current and the second is due to on-chip dissipation caused by the load current. The worst-case load-induced power occurs when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 the supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-) \bullet (I_{SMAX}) + (V^+/2)2/R_L \text{ or}$$

$$P_{DMAX} = (V^+ - V^-) \bullet (I_{SMAX}) + (V^+ - V_{OMAX}) \bullet (V_{OMAX}/R_L)$$

Example: LT1819IS8 at 85°C, V_S = ±5V, R_L = 100Ω

$$P_{DMAX} = (10V) \bullet (14mA) + (2.5V)2/100\Omega = 202.5mW$$

$$T_{JMAX} = 85°C + (2 \bullet 202.5mW) \bullet (150°C/W) = 146°C$$

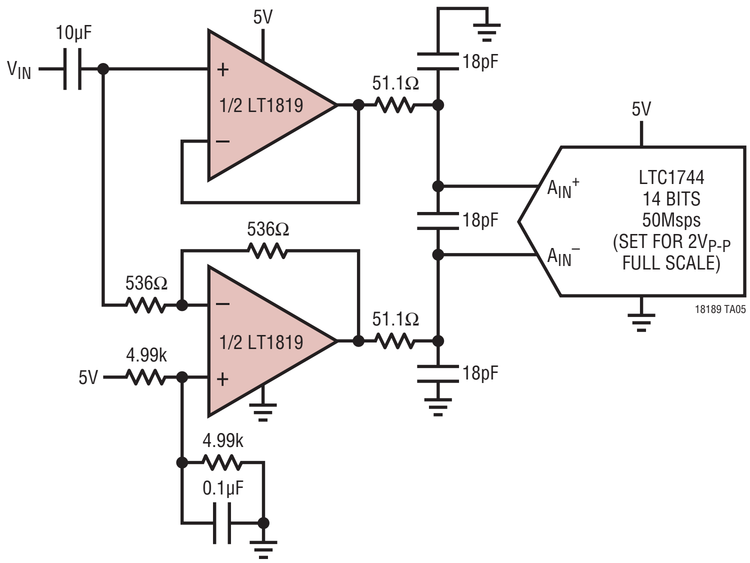
Circuit Operation

The LT1818/LT1819 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the Simplified Schematic. Complementary NPN and PNP emitter followers buffer the inputs and drive an internal resistor. The input voltage appears across the resistor, generating a current that is mirrored into the high impedance node.

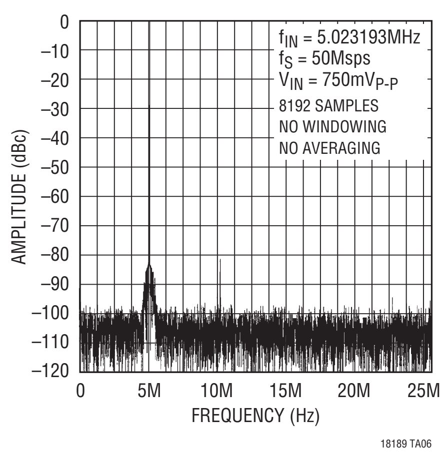
Complementary followers form an output stage that buffer the gain node from the load. The input resistor, input stage transconductance and the capacitor on the high impedance node determine the bandwidth. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input step. Highest slew rates are therefore seen in the lowest gain configurations.

TYPICAL APPLICATION

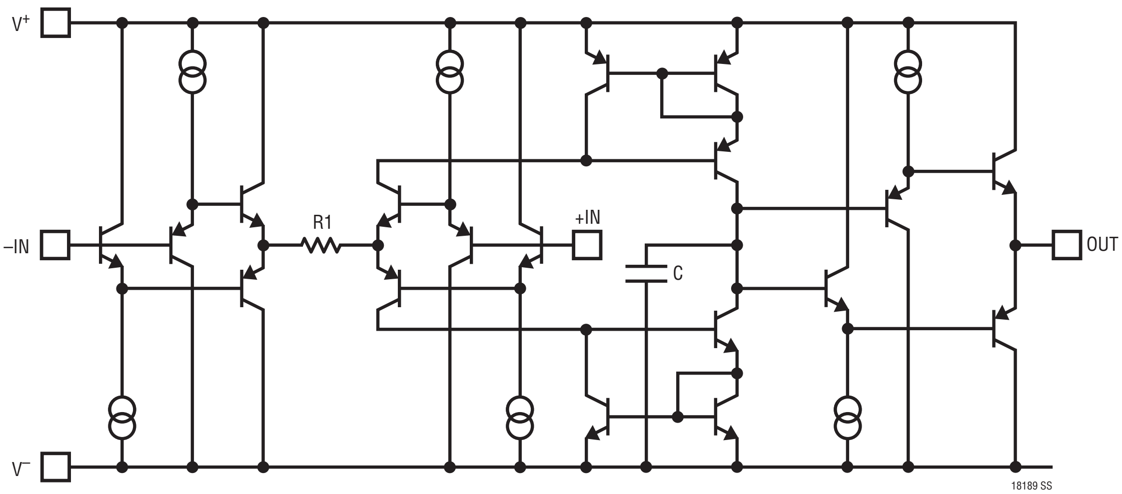
Single Supply Differential ADC Driver



Results Obtained with the Circuit of Figure 2 at 5MHz.
FFT Shows 81dB Overall Spurious Free Dynamic Range

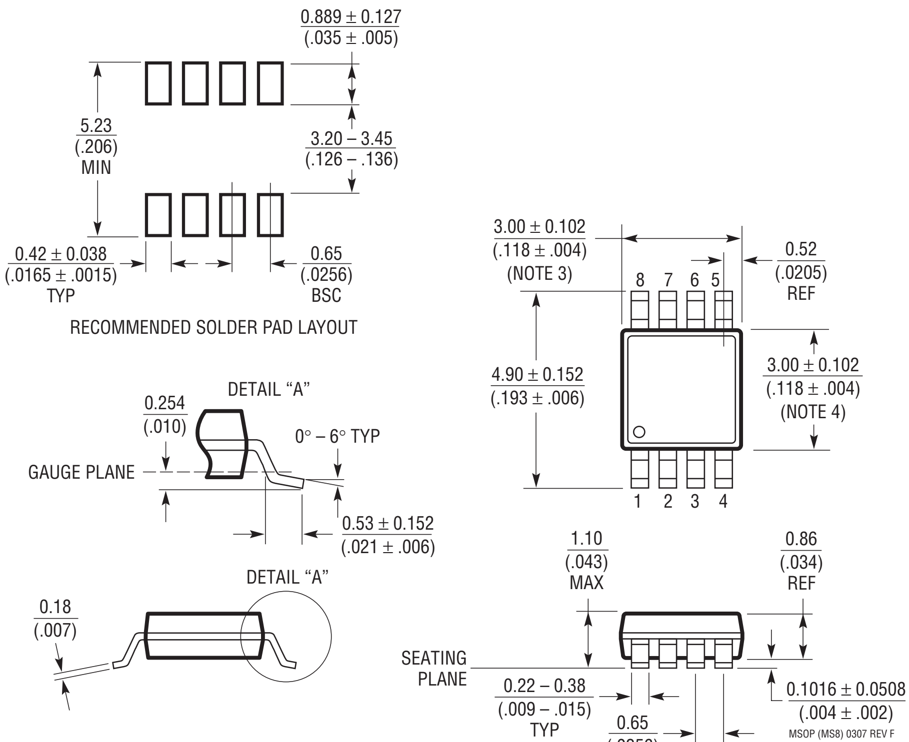


SIMPLIFIED SCHEMATIC (One Amplifier)



PACKAGE DESCRIPTION

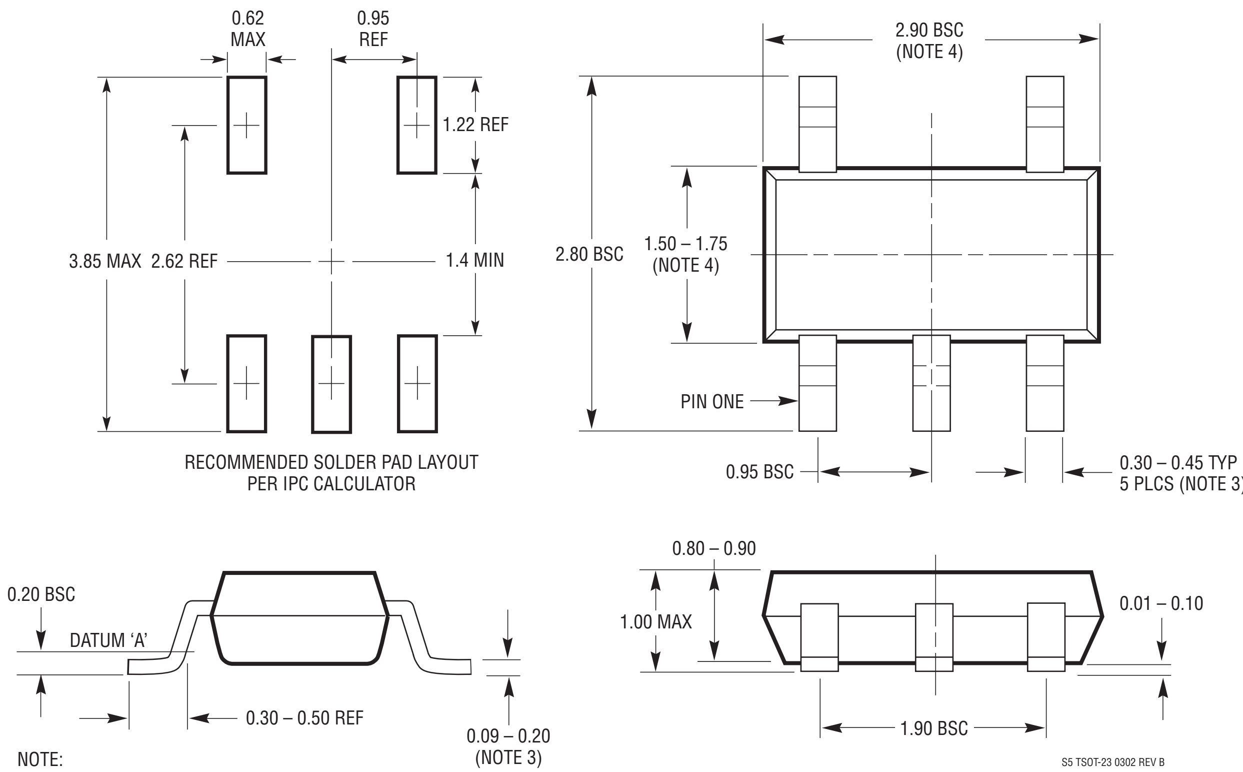
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

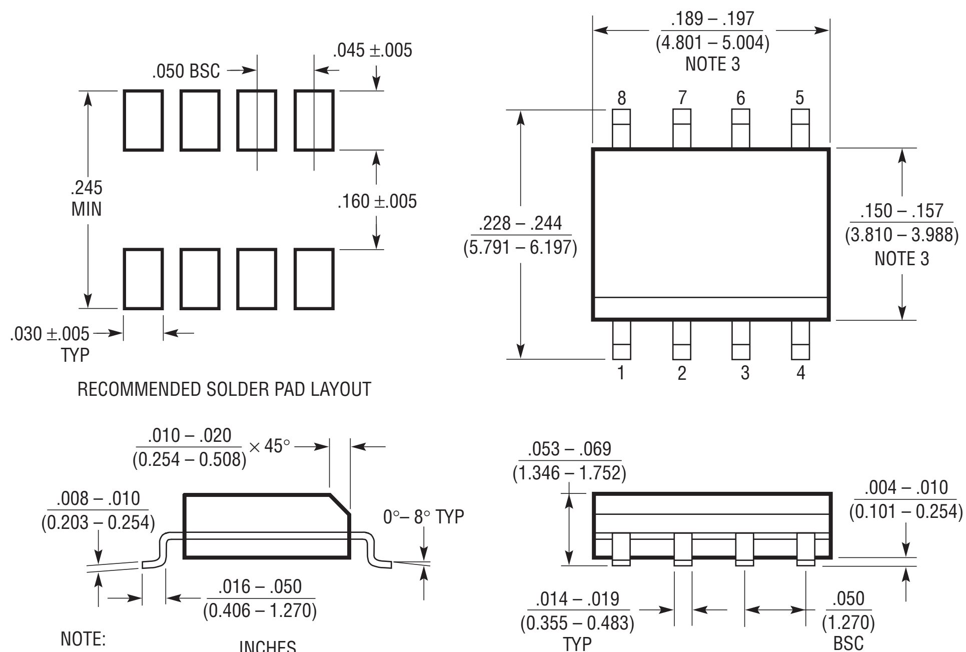
S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

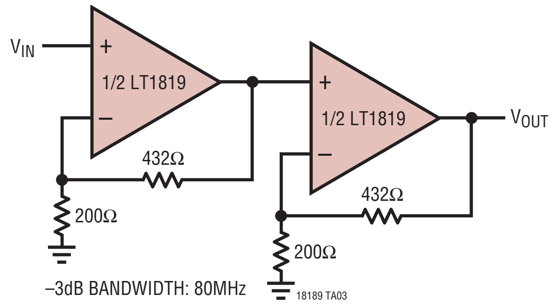
SO8 0303

REVISION HISTORY (Revision history begins at Rev B)

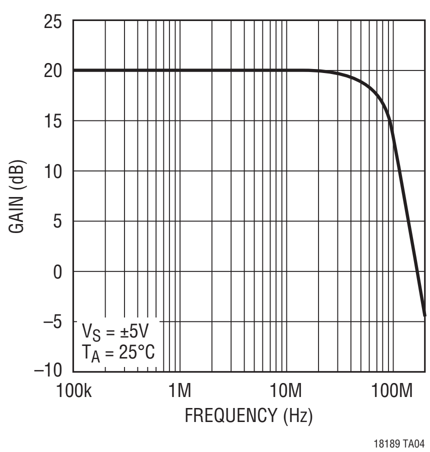
REV	DATE	DESCRIPTION	PAGE NUMBER
B	5/10	Updated Order Information Section	2

TYPICAL APPLICATION

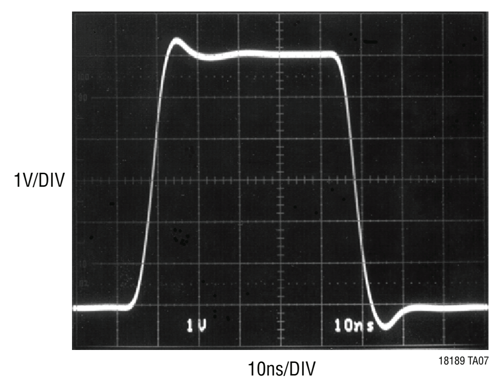
80MHz, 20dB Gain Block



20dB Gain Block Frequency Response



Large-Signal Transient Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1395/LT1396/LT1397	Single/Dual/Quad 400MHz Current Feedback Amplifiers	4.6mA Supply Current
LT1806/LT1807	Single/Dual 325MHz, 140V/μs Rail-to-Rail I/O Op Amps	Low Noise: 3.5nV/$\sqrt{Hz}$
LT1809/LT1810	Single/Dual 180MHz, 350V/μs Rail-to-Rail I/O Op Amps	Low Distortion: –90dBc at 5MHz
LT1812/LT1813/LT1814	Single/Dual/Quad 100MHz, 750V/μs Op Amps	Low Power: 3.6mA Max at ±5V
LT1815/LT1816/LT1817	Single/Dual/Quad 220MHz, 1500V/μs Op Amps	Programmable Supply Current
LT6203/LT6204	Dual/Quad 100MHz, Rail-to-Rail I/O Op Amps	1.9nV/$\sqrt{Hz}$ Noise, 3mA Max

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