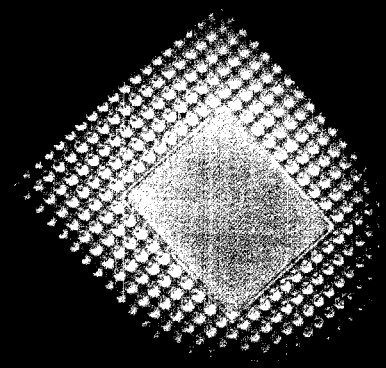
The Programmable Logic Data Book Supplement

XC4000XL/EX/E

Data Book



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XILINX

XC4000 Series Table of Contents

XC4000E and XC4000X Series Field Programmable Gate Arrays

XC4000E and XC4000X Series Features

Note: XC4000 Series devices described in this data sheet include the XC4000E family and XC4000X Series. XC4000X Series devices described in this data sheet include the XC4000EX and XC4000XL families. This information does not apply to the older Xilinx families: XC4000, XC4000A, XC4000D, XC4000H, or XC4000L. For information on these devices, see the Xilinx WEBLINX at http://www.xilinx.com.

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Fully PCI compliant (speed grades -2 and faster)
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 80 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XC4000E output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- XACT*step* Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization

Low-Voltage Versions Available

- Low-Voltage Devices Function at 3.0 - 3.6 Volts
- XC4000XL: High Performance Low-Voltage Versions of XC4000EX devices

Additional XC4000X Series Features

- Highest Performance — 3.3 V XC4000XL
- Highest Capacity — Over 180,000 Usable Gates
- 5V tolerant I/Os on XC4000XL
- 0.35µ SRAM process for XC4000XL
- Additional Routing Over XC4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
- 12-mA Sink Current Per XC4000X Output
- Flexible New High-Speed Clock Network
  - 8 additional Early Buffers for shorter clock delays
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 4 Additional Address Bits in Master Parallel Configuration Mode

Introduction

XC4000 Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

The XC4000E and XC4000X Series currently have 20 members, as shown in Table 1.

Note: *All functionality in low-voltage families is the same as in the corresponding 5-Volt family, except where numerical references are made to timing or power.*

Table 1: XC4000E and XC4000X Series Field Programmable Gate Arrays

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O
XC4003E	238	3,000	3,200	2,000 - 5,000	10 x 10	100	360	80
XC4005E/XL	466	5,000	6,272	3,000 - 9,000	14 x 14	196	616	112
XC4006E	608	6,000	8,192	4,000 - 12,000	16 x 16	256	768	128
XC4008E	770	8,000	10,368	6,000 - 15,000	18 x 18	324	936	144
XC4010E/XL	950	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	160
XC4013E/XL	1368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192
XC4020E/XL	1862	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	224
XC4025E	2432	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	256
XC4028EX/XL	2432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256
XC4036EX/XL	3078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288
XC4044XL	3800	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	320
XC4052XL	4598	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	352
XC4062XL	5472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384
XC4085XL	7448	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	448

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

Description

XC4000 Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave and peripheral modes).

XC4000 Series FPGAs are supported by powerful and sophisticated software, covering every aspect of design from schematic or behavioral entry, floorplanning, simulation, automatic block placement and routing of interconnects, to the creation, downloading, and readback of the configuration bit stream.

Because Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 5,000 systems per month. For lowest high-volume unit cost, a design can first be implemented in the XC4000E or XC4000X, then migrated to one of Xilinx' compatible HardWire mask-programmed devices.

Taking Advantage of Reconfiguration

FPGA devices can be reconfigured to change logic function while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be reconfigured dynamically to perform different functions at different times.

Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement multi-purpose hardware for a given application. As an added benefit, using reconfigurable FPGA devices simplifies hardware design and debugging and shortens product time-to-market.

XC4000E and XC4000X Series Compared to the XC4000

For readers already familiar with the XC4000 family of Xilinx Field Programmable Gate Arrays, the major new features in the XC4000 Series devices are listed in this section. The biggest advantages of XC4000E and XC4000X devices are significantly increased system speed, greater capacity, and new architectural features, particularly Select-RAM memory. The XC4000X devices also offer many new routing features, including special high-speed clock buffers that can be used to capture input data with minimal delay.

Any XC4000E device is pinout- and bitstream-compatible with the corresponding XC4000 device. An existing XC4000 bitstream can be used to program an XC4000E device. However, since the XC4000E includes many new features, an XC4000E bitstream cannot be loaded into an XC4000 device.

XC4000X Series devices are not bitstream-compatible with equivalent array size devices in the XC4000 or XC4000E families. However, equivalent array size devices, such as the XC4025, XC4025E, XC4028EX, and XC4028XL, are pinout-compatible.

Improvements in XC4000E and XC4000X

Increased System Speed

XC4000E and XC4000X devices can run at synchronous system clock rates of up to 80 MHz, and internal performance can exceed 150 MHz. This increase in performance over the previous families stems from improvements in both device processing and system architecture. XC4000 Series devices use a sub-micron multi-layer metal process. In addition, many architectural improvements have been made, as described below.

The XC4000XL family is a high performance 3.3V family based on 0.35µ SRAM technology and supports system speeds to 80 MHz.

PCI Compliance

XC4000 Series -2 and faster speed grades are fully PCI compliant. XC4000E and XC4000X devices can be used to implement a one-chip PCI solution.

Carry Logic

The speed of the carry logic chain has increased dramatically. Some parameters, such as the delay on the carry chain through a single CLB (TBYP), have improved by as much as 50% from XC4000 values. See "Fast Carry Logic" on page 16 for more information.

Select-RAM Memory: Edge-Triggered, Synchronous RAM Modes

The RAM in any CLB can be configured for synchronous, edge-triggered, write operation. The read operation is not affected by this change to an edge-triggered write.

Dual-Port RAM

A separate option converts the 16x2 RAM in any CLB into a 16x1 dual-port RAM with simultaneous Read/Write.

The function generators in each CLB can be configured as either level-sensitive (asynchronous) single-port RAM, edge-triggered (synchronous) single-port RAM, edge-triggered (synchronous) dual-port RAM, or as combinatorial logic.

Configurable RAM Content

The RAM content can now be loaded at configuration time, so that the RAM starts up with user-defined data.

H Function Generator

In current XC4000 Series devices, the H function generator is more versatile than in the original XC4000. Its inputs can come not only from the F and G function generators but also from up to three of the four control input lines. The H function generator can thus be totally or partially independent of the other two function generators, increasing the maximum capacity of the device.

IOB Clock Enable

The two flip-flops in each IOB have a common clock enable input, which through configuration can be activated individually for the input or output flip-flop or both. This clock enable operates exactly like the EC pin on the XC4000 CLB. This new feature makes the IOBs more versatile, and avoids the need for clock gating.

Output Drivers

The output pull-up structure defaults to a TTL-like totem-pole. This driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc, just like the XC4000 family outputs. Alternatively, XC4000 Series devices can be globally configured with CMOS outputs, with p-channel pull-up transistors pulling to Vcc. Also, the configurable pull-up resistor in the XC4000 Series is a p-channel transistor that pulls to Vcc, whereas in the original XC4000 family it is an n-channel transistor that pulls to a voltage one transistor threshold below Vcc.

Input Thresholds

The input thresholds of 5V devices can be globally configured for either TTL (1.2 V threshold) or CMOS (2.5 V threshold), just like XC2000 and XC3000 inputs. The two global adjustments of input threshold and output level are independent of each other. The XC4000XL family has an

input threshold of 1.6V, compatible with both 3.3V CMOS and TTL levels.

Global Signal Access to Logic

There is additional access from global clocks to the F and G function generator inputs.

Configuration Pin Pull-Up Resistors

During configuration, the three mode pins, M0, M1, and M2, have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected.

The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors after configuration.

The $\overline{\text{PROGRAM}}$ input pin has a permanent weak pull-up.

Soft Start-up

Like the XC3000A, XC4000 Series devices have "Soft Start-up." When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. Immediately after start-up, the slew rate of the individual outputs is, as in the XC4000 family, determined by the individual configuration option.

XC4000 and XC4000A Compatibility

Existing XC4000 bitstreams can be used to configure an XC4000E device. XC4000A bitstreams must be recompiled for use with the XC4000E due to improved routing resources, although the devices are pin-for-pin compatible.

Additional Improvements in XC4000X Only

Increased Routing

New interconnect in the XC4000X includes twenty-two additional vertical lines in each column of CLBs and twelve new horizontal lines in each row of CLBs. The twelve "Quad Lines" in each CLB row and column include optional repowering buffers for maximum speed. Additional high-performance routing near the IOBs enhances pin flexibility.

Faster Input and Output

A fast, dedicated early clock sourced by global clock buffers is available for the IOBs. To ensure synchronization with the regular global clocks, a Fast Capture latch driven by the early clock is available. The input data can be initially loaded into the Fast Capture latch with the early clock, then transferred to the input flip-flop or latch with the low-skew global clock. A programmable delay on the input can be used to avoid hold-time requirements. See "IOB Input Signals" on page 18 for more information.

Latch Capability in CLBs

Storage elements in the XC4000X CLB can be configured as either flip-flops or latches. This capability makes the FPGA highly synthesis-compatible.

IOB Output MUX From Output Clock

A multiplexer in the IOB allows the output clock to select either the output data or the IOB clock enable as the output to the pad. Thus, two different data signals can share a single output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. This multiplexer can also be configured as an AND-gate to implement a very fast pin-to-pin path. See "IOB Output Signals" on page 21 for more information.

Additional Address Bits

Larger devices require more bits of configuration data. A daisy chain of several large XC4000X devices may require a PROM that cannot be addressed by the eighteen address bits supported in the XC4000E. The XC4000X Series therefore extends the addressing in Master Parallel configuration mode to 22 bits.

Detailed Functional Description

XC4000 Series devices achieve high speed through advanced semiconductor technology and improved architecture. The XC4000E and XC4000X support system clock rates of up to 80 MHz and internal performance in excess of 150 MHz. Compared to older Xilinx FPGA families, XC4000 Series devices are more powerful. They offer on-chip edge-triggered and dual-port RAM, clock enables on I/O flip-flops, and wide-input decoders. They are more versatile in many applications, especially those involving RAM. Design cycles are faster due to a combination of increased routing resources and more sophisticated software.

Basic Building Blocks

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.

Three other types of circuits are also available:

- 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
- Wide edge decoders are available around the periphery of each device.
- An on-chip oscillator is provided.

Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Each of these available circuits is described in this section.

Configurable Logic Blocks (CLBs)

Configurable Logic Blocks implement most of the logic in an FPGA. The principal CLB elements are shown in Figure 1.

Two 4-input function generators (F and G) offer unrestricted versatility. Most combinatorial logic functions need four or fewer inputs. However, a third function generator (H) is provided. The H function generator has three inputs. Either zero, one, or two of these inputs can be the outputs of F and G; the other input(s) are from outside the CLB. The CLB can, therefore, implement certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

Each CLB contains two storage elements that can be used to store the function generator outputs. However, the storage elements and function generators can also be used independently. These storage elements can be configured as flip-flops in both XC4000E and XC4000X devices; in the XC4000X they can optionally be configured as latches. DIN can be used as a direct input to either of the two storage elements. H1 can drive the other through the H function generator. Function generator outputs can also drive two outputs independent of the storage element outputs. This versatility increases logic capacity and simplifies routing.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and storage elements. These inputs and outputs connect to the programmable interconnect resources outside the block.

Function Generators

Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, with outputs labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of four inputs. The function generators are implemented as memory look-up tables. The propagation delay is therefore independent of the function implemented.

A third function generator, labeled H', can implement any Boolean function of its three inputs. Two of these inputs can optionally be the F' and G' functional generator outputs. Alternatively, one or both of these inputs can come from outside the CLB (H2, H0). The third input must come from outside the block (H1).

Signals from the function generators can exit the CLB on two outputs. F' or H' can be connected to the X output. G' or H' can be connected to the Y output.

A CLB can be used to implement any of the following functions:

- any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables[1]
- any single function of five variables
- any function of four variables together with some functions of six variables
- some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

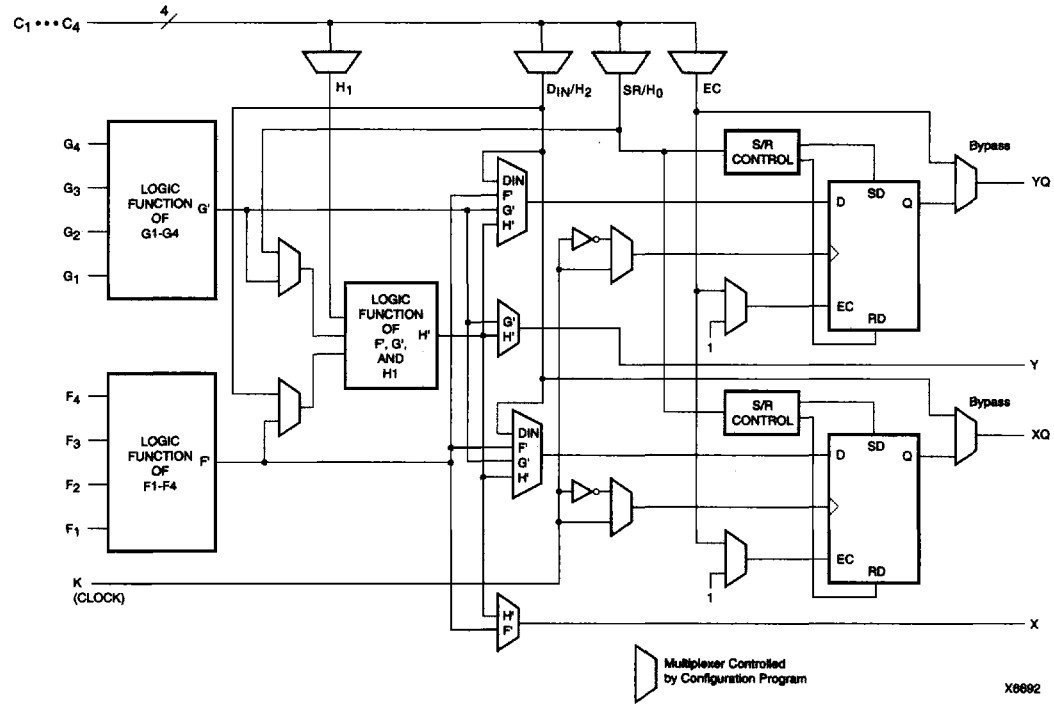


Figure 1: Simplified Block Diagram of XC4000 Series CLB (RAM and Carry Logic functions not shown)

Flip-Flops

The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well.

The two edge-triggered D-type flip-flops have common clock (K) and clock enable (EC) inputs. Either or both clock inputs can also be permanently enabled. Storage element functionality is described in Table 2.

Latches (XC4000X only)

The CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Storage element functionality is described in Table 2.

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The clock pin is shared by both storage elements. However, the clock is individually invertible for each storage element. Any inverter placed on the clock input is automatically absorbed into the CLB.

Clock Enable

The clock enable signal (EC) is active High. The EC pin is shared by both storage elements. If left unconnected for either, the clock enable for that storage element defaults to the active state. EC is not invertible within the CLB.

Table 2: CLB Storage Element Functionality (active rising edge is shown)

Mode	K	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop	X	X	1	X	SR
	↑	1*	0*	D	D
	0	X	0*	X	Q
Latch	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X	Don't care
↑	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Set/Reset

An asynchronous storage element input (SR) can be configured as either set or reset. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a Global Set/Reset pulse during normal operation, and the effect of a pulse on the SR pin of the CLB. All three set/reset functions for any single flip-flop are controlled by the same configuration data bit.

The set/reset state can be independently specified for each flip-flop. This input can also be independently disabled for either flip-flop.

The set/reset state is specified by using the INIT attribute, or by placing the appropriate set or reset flip-flop library symbol.

SR is active High. It is not invertible within the CLB.

Global Set/Reset

A separate Global Set/Reset line (not shown in Figure 1) sets or clears each storage element during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, a reset flip-flop is reset by both SR and GSR.

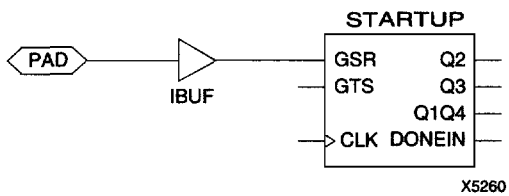


Figure 2: Schematic Symbols for Global Set/Reset

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 2.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global Set/Reset signal.

Alternatively, GSR can be driven from any internal node.

Data Inputs and Outputs

The source of a storage element data input is programmable. It is driven by any of the functions F', G', and H', or by the Direct In (DIN) block input. The flip-flops or latches drive the XQ and YQ CLB outputs.

Two fast feed-through paths are available, as shown in Figure 1. A two-to-one multiplexer on each of the XQ and YQ outputs selects between a storage element output and any of the control inputs. This bypass is sometimes used by the automated router to repower internal signals.

Control Signals

Multiplexers in the CLB map the four control inputs (C1 - C4 in Figure 1) into the four internal control signals (H1, DIN/H2, SR/H0, and EC). Any of these inputs can drive any of the four internal control signals.

When the logic function is enabled, the four inputs are:

- EC — Enable Clock
- SR/H0 — Asynchronous Set/Reset or H function generator Input 0
- DIN/H2 — Direct In or H function generator Input 2
- H1 — H function generator Input 1.

When the memory function is enabled, the four inputs are:

- EC — Enable Clock
- WE — Write Enable
- D0 — Data Input to F and/or G function generator
- D1 — Data input to G function generator (16x1 and 16x2 modes) or 5th Address bit (32x1 mode).

Using FPGA Flip-Flops and Latches

The abundance of flip-flops in the XC4000 Series invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever throughput is more important than latency.

To include a CLB flip-flop, place the appropriate library symbol. For example, FDCE is a D-type flip-flop with clock enable and asynchronous clear. The corresponding latch symbol (for the XC4000X only) is called LDCE.

In XC4000 Series devices, the flip flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This ability increases the functional capacity of the devices.

The CLB setup time is specified between the function generator inputs and the clock input K. Therefore, the specified CLB flip-flop setup time includes the delay through the function generator.

Using Function Generators as RAM

Optional modes for each CLB make the memory look-up tables in the F' and G' function generators usable as an array of Read/Write memory cells. Available modes are level-sensitive (similar to the XC4000/A/H families), edge-triggered, and dual-port edge-triggered. Depending on the selected mode, a single CLB can be configured as either a 16x2, 32x1, or 16x1 bit array.

Supported CLB memory configurations and timing modes for single- and dual-port modes are shown in Table 3.

XC4000 Series devices are the first programmable logic devices with edge-triggered (synchronous) and dual-port RAM accessible to the user. Edge-triggered RAM simplifies system timing. Dual-port RAM doubles the effective throughput of FIFO applications. These features can be individually programmed in any XC4000 Series CLB.

Advantages of On-Chip and Edge-Triggered RAM

The on-chip RAM is extremely fast. The read access time is the same as the logic delay. The write access time is slightly slower. Both access times are much faster than any off-chip solution, because they avoid I/O delays.

Edge-triggered RAM, also called synchronous RAM, is a feature never before available in a Field Programmable Gate Array. The simplicity of designing with edge-triggered RAM, and the markedly higher achievable performance, add up to a significant improvement over existing devices with on-chip RAM.

Three application notes are available from Xilinx that discuss edge-triggered RAM: "*XC4000E Edge-Triggered and Dual-Port RAM Capability*," "*Implementing FIFOs in XC4000E RAM*," and "*Synchronous and Asynchronous FIFO Designs*." All three application notes apply to both XC4000E and XC4000X RAM.

Table 3: Supported RAM Modes

	16 x 1	16 x 2	32 x 1	Edge-Triggered Timing	Level-Sensitive Timing
Single-Port	√	√	√	√	√
Dual-Port	√			√	

RAM Configuration Options

The function generators in any CLB can be configured as RAM arrays in the following sizes:

- Two 16x1 RAMs: two data inputs and two data outputs with identical or, if preferred, different addressing for each RAM
- One 32x1 RAM: one data input and one data output.

One F or G function generator can be configured as a 16x1 RAM while the other function generators are used to implement any function of up to 5 inputs.

Additionally, the XC4000 Series RAM may have either of two timing modes:

- Edge-Triggered (Synchronous): data written by the designated edge of the CLB clock. WE acts as a true clock enable.
- Level-Sensitive (Asynchronous): an external WE signal acts as the write strobe.

The selected timing mode applies to both function generators within a CLB when both are configured as RAM.

The number of read ports is also programmable:

- Single Port: each function generator has a common read and write port
- Dual Port: both function generators are configured together as a single 16x1 dual-port RAM with one write port and two read ports. Simultaneous read and write operations to the same or different addresses are supported.

RAM configuration options are selected by placing the appropriate library symbol.

Choosing a RAM Configuration Mode

The appropriate choice of RAM mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Recommended usage is shown in Table 4.

The difference between level-sensitive, edge-triggered, and dual-port RAM is only in the write operation. Read operation and timing is identical for all modes of operation.

Table 4: RAM Mode Selection

	Level-Sensitive	Edge-Triggered	Dual-Port Edge-Triggered
Use for New Designs?	No	Yes	Yes
Size (16x1, Registered)	1/2 CLB	1/2 CLB	1 CLB
Simultaneous Read/Write	No	No	Yes
Relative Performance	X	2X	2X (4X effective)

RAM Inputs and Outputs

The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table.

The functionality of the CLB control signals changes when the function generators are configured as RAM. The DIN/H2, H1, and SR/H0 lines become the two data inputs (D0, D1) and the Write Enable (WE) input for the 16x2 memory. When the 32x1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input.

The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs. They can exit the CLB through its X and Y outputs, or can be captured in the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other por-

tions of the CLB, with the exception of the redefinition of the control signals. In 16x2 and 16x1 modes, the H' function generator can be used to implement Boolean functions of F', G', and D1, and the D flip-flops can latch the F', G', H', or D0 signals.

Single-Port Edge-Triggered Mode

Edge-triggered (synchronous) RAM simplifies timing requirements. XC4000 Series edge-triggered RAM timing operates like writing to a data register. Data and address are presented. The register is enabled for writing by a logic High on the write enable input, WE. Then a rising or falling clock edge loads the data into the register, as shown in Figure 3.

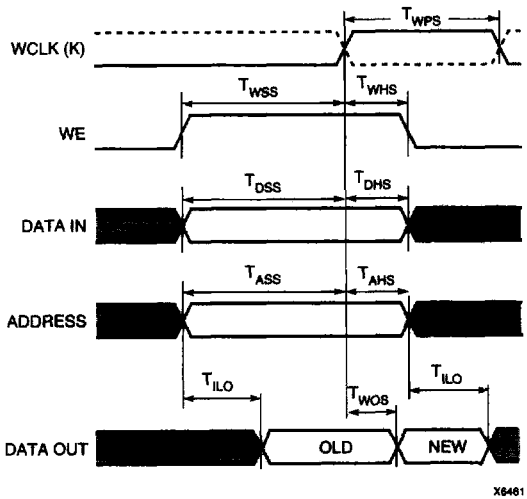


Figure 3: Edge-Triggered RAM Write Timing

Complex timing relationships between address, data, and write enable signals are not required, and the external write enable pulse becomes a simple clock enable. The active edge of WCLK latches the address, input data, and WE signals. An internal write pulse is generated that performs the write. See Figure 4 and Figure 5 for block diagrams of a CLB configured as 16x2 and 32x1 edge-triggered, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port, edge-triggered mode are shown in Table 5.

The Write Clock input (WCLK) can be configured as active on either the rising edge (default) or the falling edge. It uses the same CLB pin (K) used to clock the CLB flip-flops, but it can be independently inverted. Consequently, the RAM output can optionally be registered within the same CLB either by the same clock edge as the RAM, or by the opposite edge of this clock. The sense of WCLK applies to both function generators in the CLB when both are configured as RAM.

The WE pin is active-High and is not invertible within the CLB.

Note: The pulse following the active edge of WCLK (T_{WPS} in Figure 3) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

Table 5: Single-Port Edge-Triggered RAM Signals

RAM Signal	CLB Pin	Function
D	D0 or D1 (16x2, 16x1), D0 (32x1)	Data In
A[3:0]	F1-F4 or G1-G4	Address
A[4]	D1 (32x1)	Address
WE	WE	Write Enable
WCLK	K	Clock
SPO (Data Out)	F' or G'	Single Port Out (Data Out)

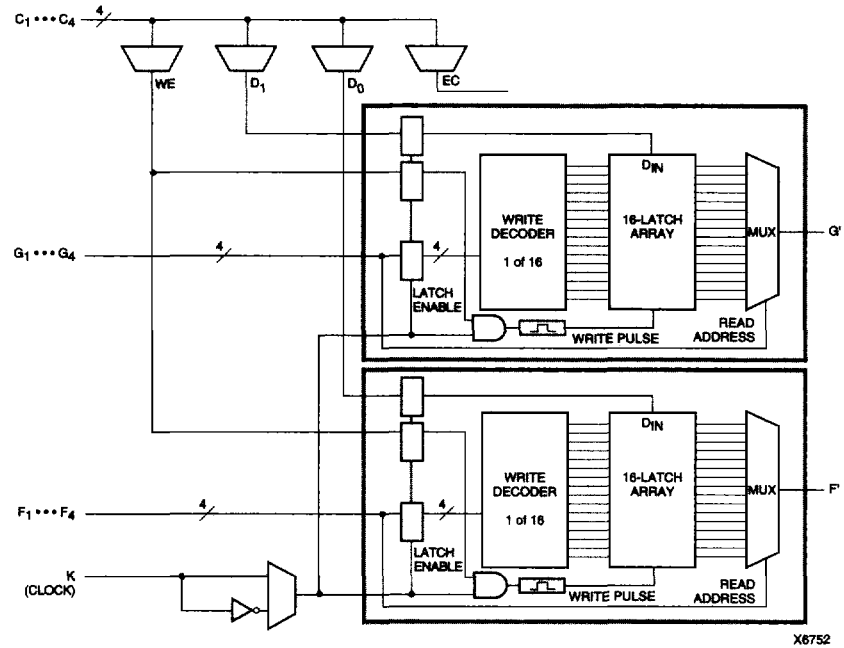


Figure 4: 16x2 (or 16x1) Edge-Triggered Single-Port RAM

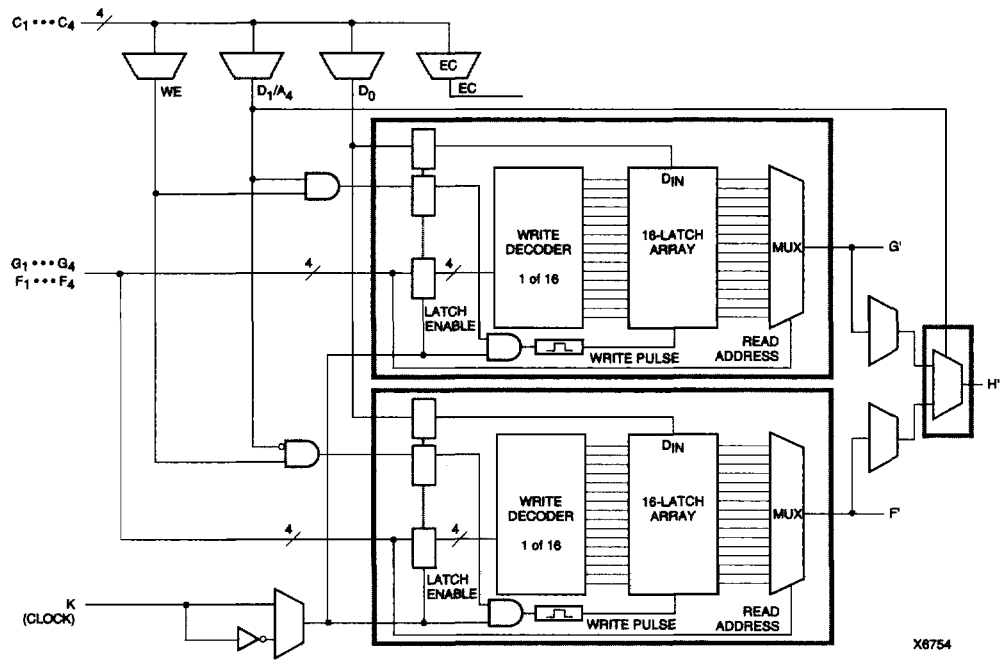


Figure 5: 32x1 Edge-Triggered Single-Port RAM (F and G addresses are identical)

Dual-Port Edge-Triggered Mode

In dual-port mode, both the F and G function generators are used to create a single 16x1 RAM array with one write port and two read ports. The resulting RAM array can be read and written simultaneously at two independent addresses. Simultaneous read and write operations at the same address are also supported.

Dual-port mode always has edge-triggered write timing, as shown in Figure 3.

Figure 6 shows a simple model of an XC4000 Series CLB configured as dual-port RAM. One address port, labeled A[3:0], supplies both the read and write address for the F function generator. This function generator behaves the same as a 16x1 single-port edge-triggered RAM array. The RAM output, Single Port Out (SPO), appears at the F function generator output. SPO, therefore, reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the G function generator. The write address for the G function generator, however, comes from the address A[3:0]. The output from this 16x1 RAM array, Dual Port Out (DPO), appears at the G function generator output. DPO, therefore, reflects the data at address DPRA[3:0].

Therefore, by using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. Simultaneous access doubles the effective throughput of the FIFO.

The relationships between CLB pins and RAM inputs and outputs for dual-port, edge-triggered mode are shown in Table 6. See Figure 7 on page 14 for a block diagram of a CLB configured in this mode.

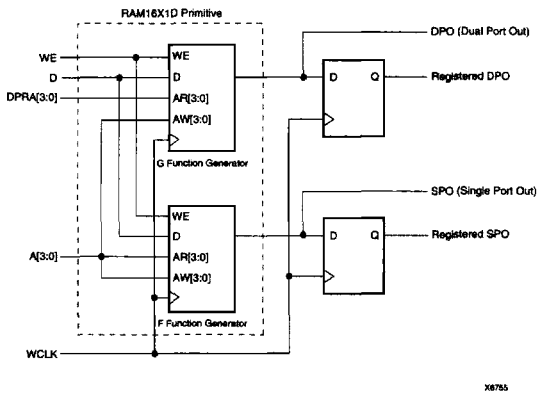


Figure 6: XC4000 Series Dual-Port RAM, Simple Model

Table 6: Dual-Port Edge-Triggered RAM Signals

RAM Signal	CLB Pin	Function
D	D0	Data In
A[3:0]	F1-F4	Read Address for F, Write Address for F and G
DPRA[3:0]	G1-G4	Read Address for G
WE	WE	Write Enable
WCLK	K	Clock
SPO	F'	Single Port Out (addressed by A[3:0])
DPO	G'	Dual Port Out (addressed by DPRA[3:0])

Note: The pulse following the active edge of WCLK (T_{WPS} in Figure 3) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

Single-Port Level-Sensitive Timing Mode

Note: Edge-triggered mode is recommended for all new designs. Level-sensitive mode, also called asynchronous mode, is still supported for XC4000 Series backward-compatibility with the XC4000 family.

Level-sensitive RAM timing is simple in concept but can be complicated in execution. Data and address signals are presented, then a positive pulse on the write enable pin (WE) performs a write into the RAM at the designated address. As indicated by the "level-sensitive" label, this RAM acts like a latch. During the WE High pulse, changing the data lines results in new data written to the old address. Changing the address lines while WE is High results in spurious data written to the new address—and possibly at other addresses as well, as the address lines inevitably do not all change simultaneously.

The user must generate a carefully timed WE signal. The delay on the WE signal and the address lines must be carefully verified to ensure that WE does not become active until after the address lines have settled, and that WE goes inactive before the address lines change again. The data must be stable before and after the falling edge of WE.

In practical terms, WE is usually generated by a 2X clock. If a 2X clock is not available, the falling edge of the system clock can be used. However, there are inherent risks in this approach, since the WE pulse must be guaranteed inactive before the next rising edge of the system clock. Several older application notes are available from Xilinx that discuss the design of level-sensitive RAMs. These application notes include XAPP031, "*Using the XC4000 RAM Capability*," and XAPP042, "*High-Speed RAM Design in XC4000*." However, the edge-triggered RAM available in the XC4000 Series is superior to level-sensitive RAM for almost every application.

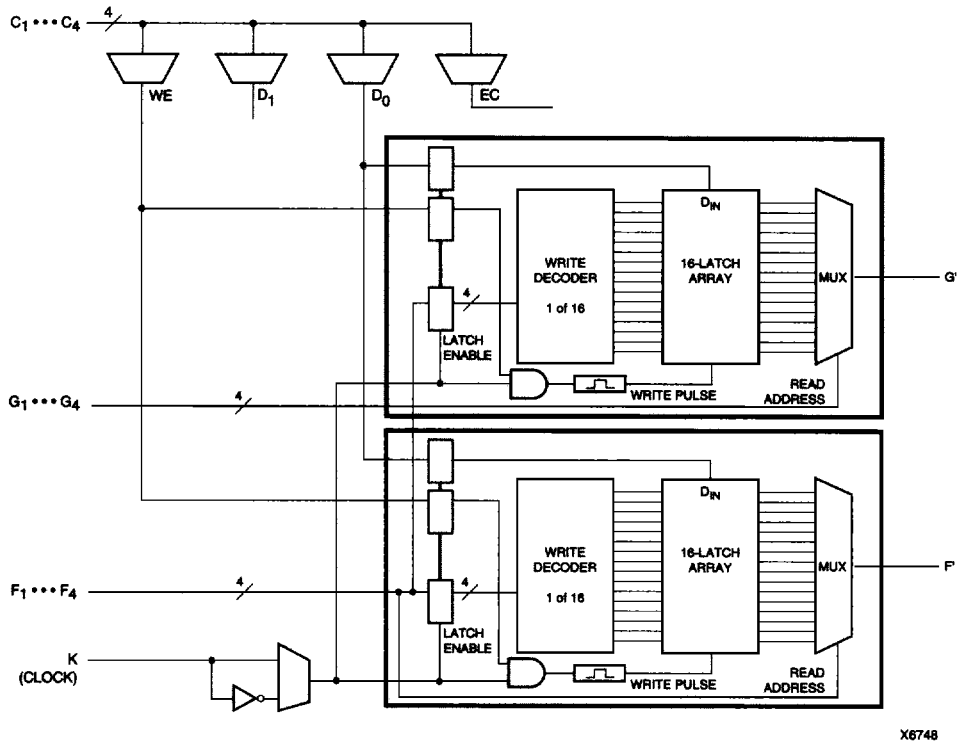


Figure 7: 16x1 Edge-Triggered Dual-Port RAM

Figure 8 shows the write timing for level-sensitive, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port level-sensitive mode are shown in Table 7.

Figure 9 and Figure 10 show block diagrams of a CLB configured as 16x2 and 32x1 level-sensitive, single-port RAM.

Initializing RAM at Configuration

Both RAM and ROM implementations of the XC4000 Series devices are initialized during configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the schematic library guide. If not defined, all RAM contents are initialized to all zeros, by default.

RAM initialization occurs only during configuration. The RAM content is not affected by Global Set/Reset.

Table 7: Single-Port Level-Sensitive RAM Signals

RAM Signal	CLB Pin	Function
D	D0 or D1	Data In
A[3:0]	F1-F4 or G1-G4	Address
WE	WE	Write Enable
O	F' or G'	Data Out

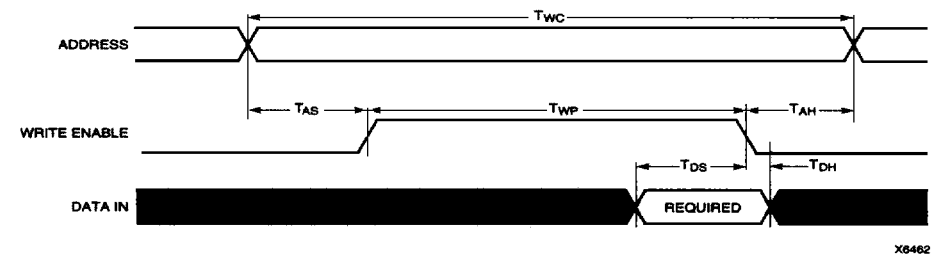


Figure 8: Level-Sensitive RAM Write Timing

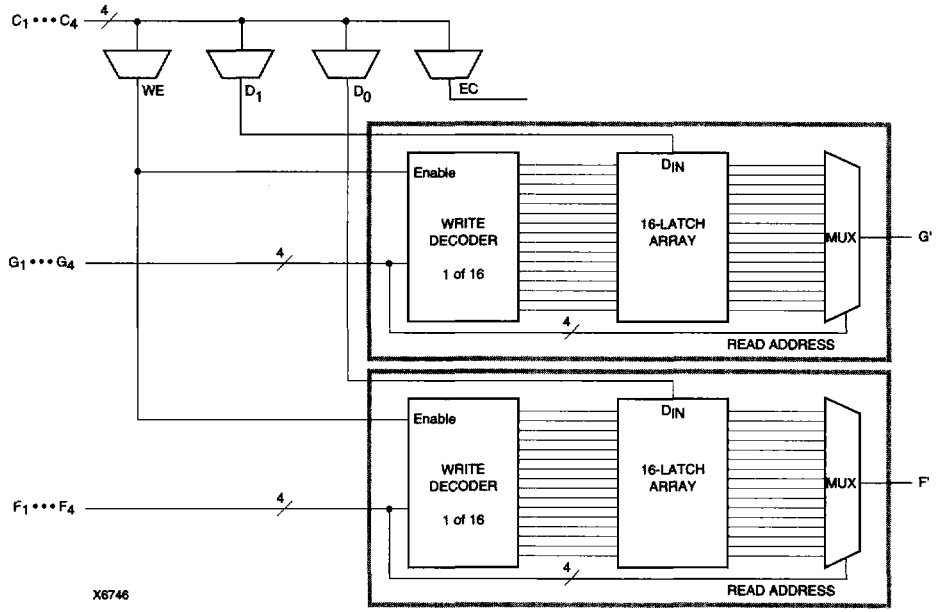


Figure 9: 16x2 (or 16x1) Level-Sensitive Single-Port RAM

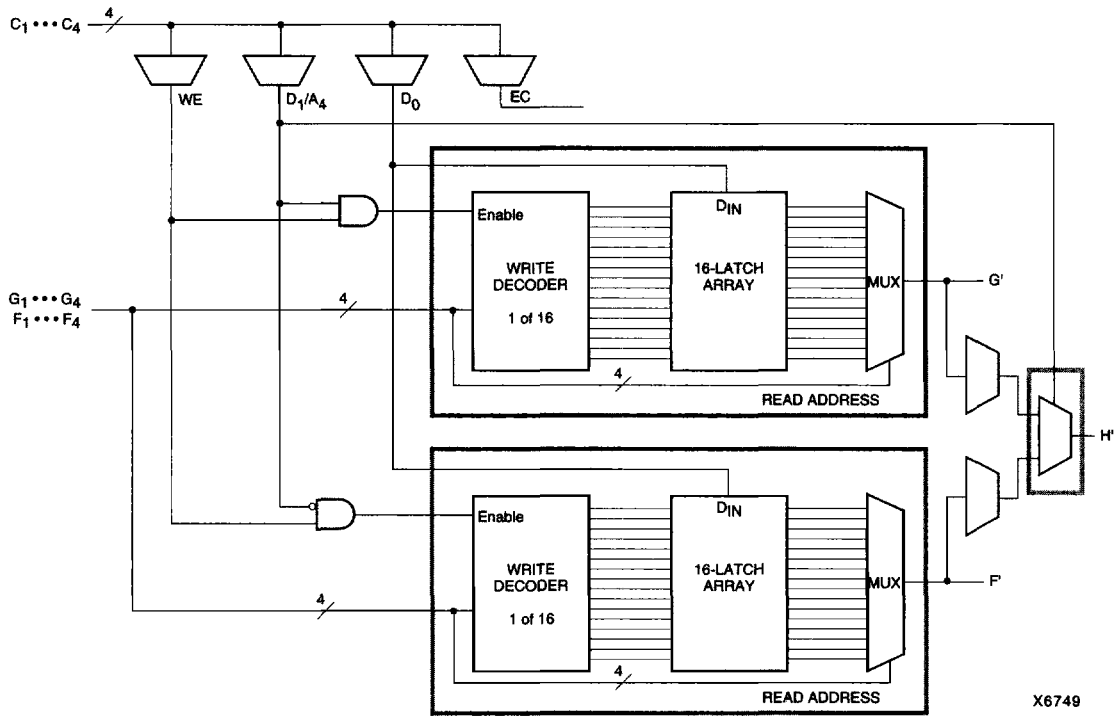


Figure 10: 32x1 Level-Sensitive Single-Port RAM (F and G addresses are identical)

Fast Carry Logic

Each CLB F and G function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources.

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

This fast carry logic is one of the more significant features of the XC4000 Series, speeding up arithmetic and counting into the 70 MHz range.

The carry chain in XC4000E devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. (See Figure 11.) In order to improve speed in the high-capacity XC4000X devices, which can potentially have very long carry chains, the carry chain travels upward only, as shown in Figure 12. Additionally, standard interconnect can be used to route a carry signal in the downward direction.

Figure 13 on page 17 shows an XC4000E CLB with dedicated fast carry logic. The carry logic in the XC4000X is similar, except that COUT exits at the top only, and the signal CINDOWN does not exist. As shown in Figure 13, the carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 14 on page 18 shows the details of the carry logic for the XC4000E. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 13. The XC4000X carry logic is very similar, but a multiplexer on the pass-through carry chain has been eliminated to reduce delay. Additionally, in the XC4000X the multiplexer on the G4 path has a memory-programmable 0 input, which permits G4 to directly connect to COUT. G4 thus becomes an additional high-speed initialization path for carry-in.

The dedicated carry logic is discussed in detail in Xilinx document XAPP 013: "*Using the Dedicated Carry Logic in XC4000.*" This discussion also applies to XC4000E devices, and to XC4000X devices when the minor logic changes are taken into account.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

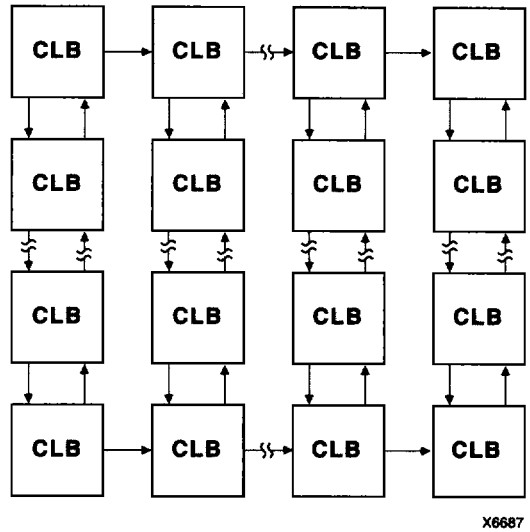


Figure 11: Available XC4000E Carry Propagation Paths

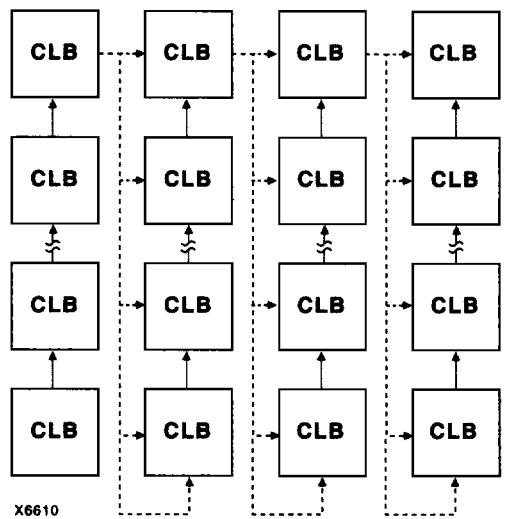


Figure 12: Available XC4000X Carry Propagation Paths (dotted lines use general interconnect)

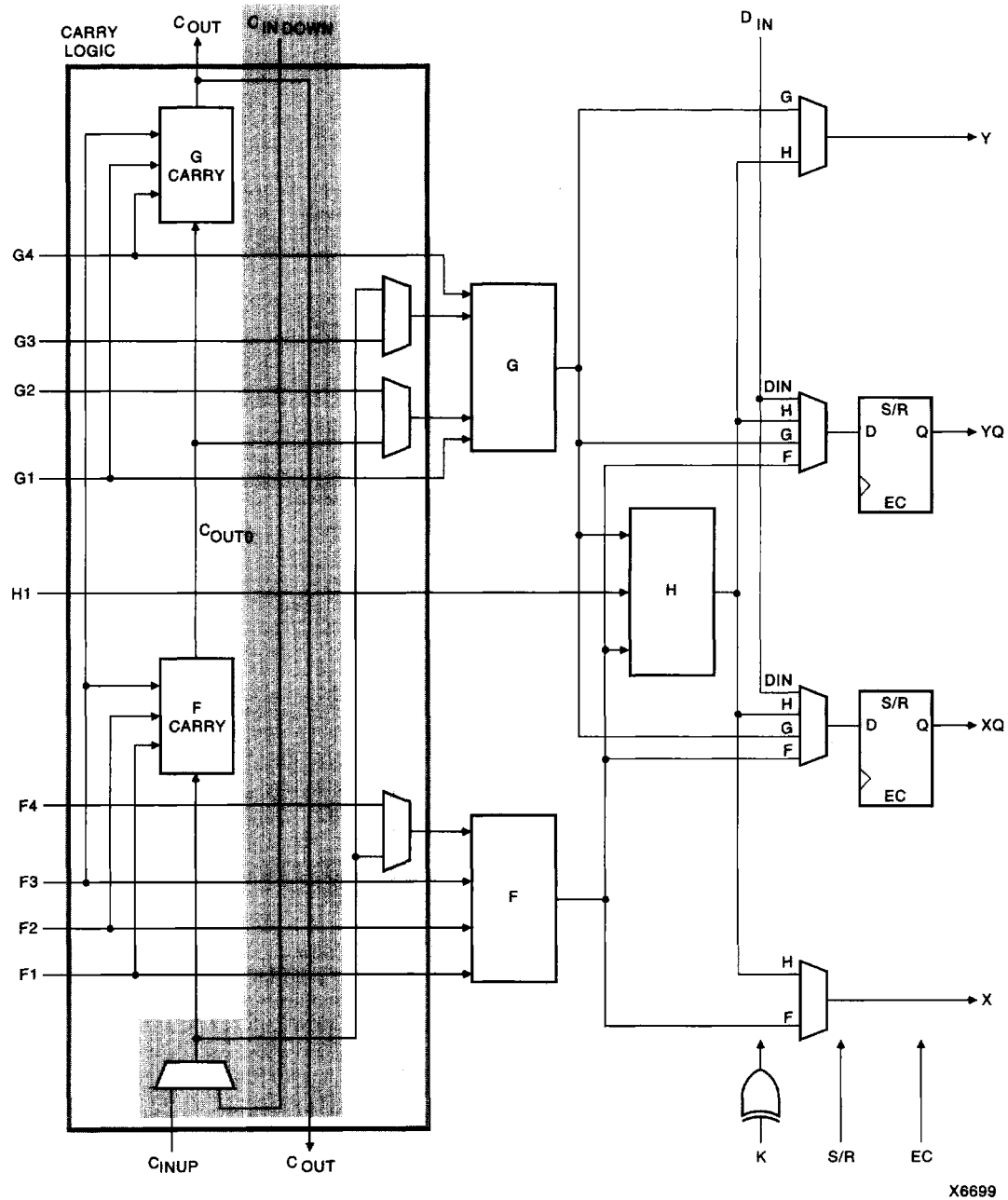


Figure 13: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000X)

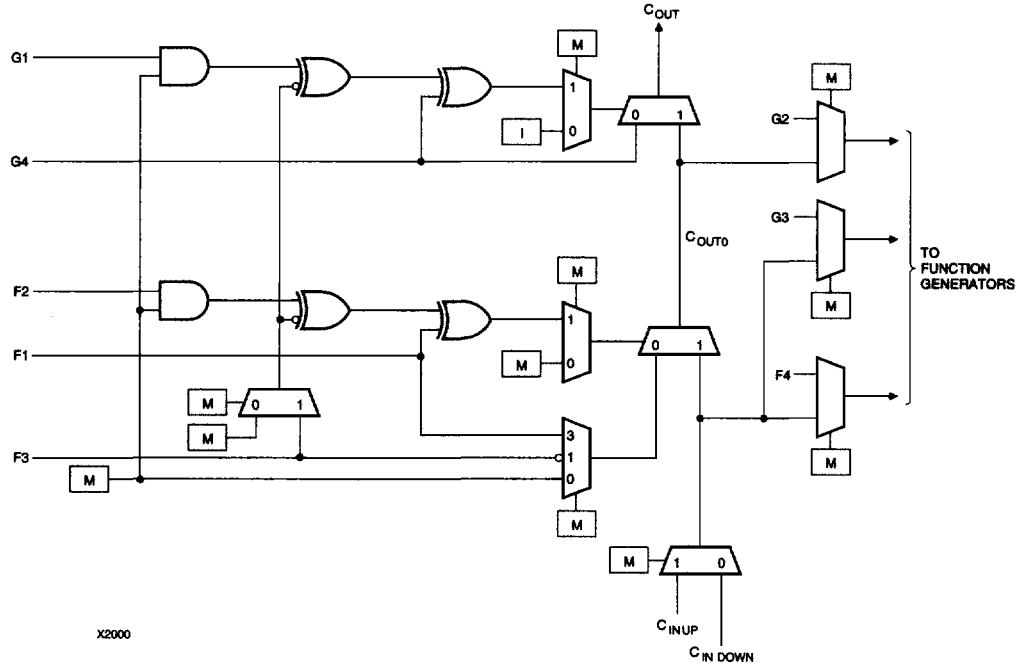


Figure 14: Detail of XC4000E Dedicated Carry Logic

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

Figure 15 shows a simplified block diagram of the XC4000E IOB. A more complete diagram of the XC4000E IOB can be found in Figure 40 on page 41, in the "Boundary Scan" section. Figure 40 includes the boundary scan logic in the IOB.

Figure 16 shows a simplified block diagram of the XC4000X IOB. The XC4000X IOB contains some special features not included in the XC4000E IOB. These features are highlighted in Figure 16, and discussed throughout this section. When XC4000X special features are discussed, they are clearly identified in the text. Any feature not so identified is present in both XC4000E and XC4000X devices.

IOB Input Signals

Two paths, labeled I1 and I2 in Figure 15 and Figure 16, bring input signals into the array. Inputs also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive latch.

The choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are available, and some combinations of latches and flip-flops can be implemented in a single IOB, as described in the *XACT Libraries Guide*.

The XC4000E inputs can be globally configured for either TTL (1.2V) or 5.0 volt CMOS thresholds, using an option in the bitstream generation software. There is a slight input hysteresis of about 300mV. The XC4000E output levels are also configurable; the two global adjustments of input threshold and output level are independent.

Inputs on the XC4000XL are TTL compatible and 3.3V CMOS compatible. Outputs on the XC4000XL are pulled to the 3.3V positive supply.

The inputs of XC4000 Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC4000 Series device inputs are shown in Table 8.

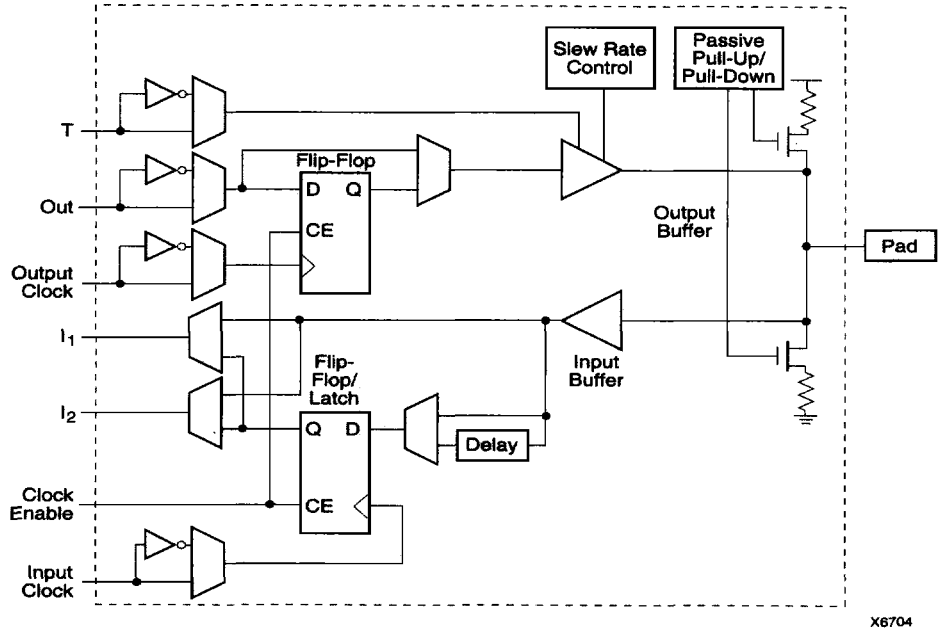


Figure 15: Simplified Block Diagram of XC4000E IOB

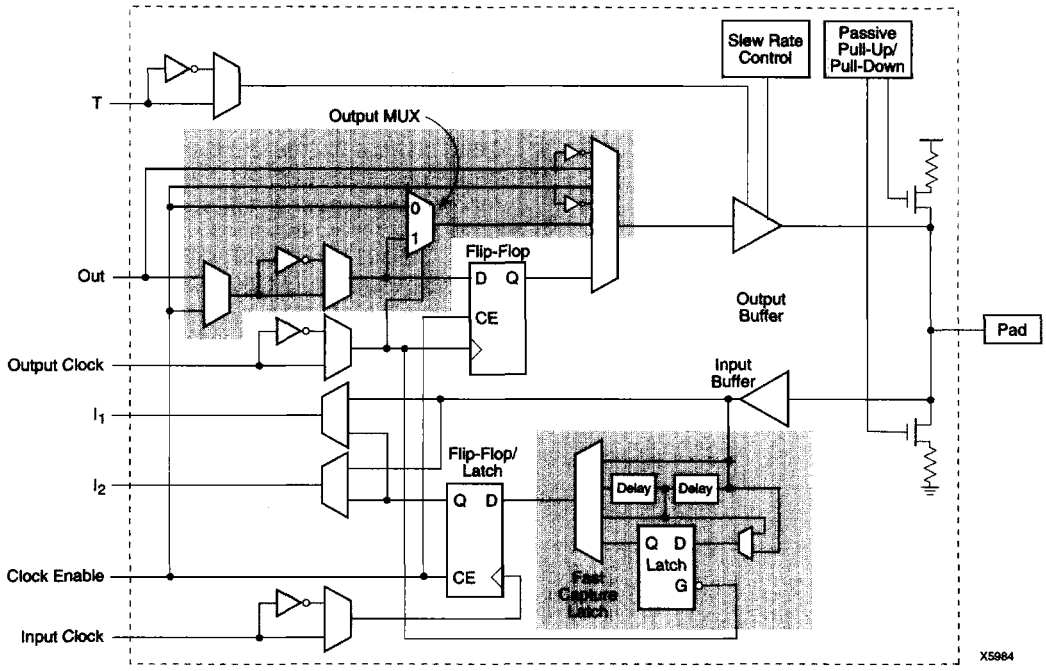


Figure 16: Simplified Block Diagram of XC4000X IOB (shaded areas indicate differences from XC4000E)

Table 8: Supported Sources for XC4000 Series Device Inputs

Source	XC4000E/EX Series Inputs		XC4000XL Series Inputs
	5 V, TTL	5 V, CMOS	3.3 V CMOS
Any device, Vcc = 3.3 V, CMOS outputs	√	Unreli -able Data	√
XC4000 Series, Vcc = 5 V, TTL outputs	√		√
Any device, Vcc = 5 V, TTL outputs (Voh ≤ 3.7 V)	√		√
Any device, Vcc = 5 V, CMOS outputs	√	√	√

XC4000XL 5-Volt Tolerant I/Os

The I/Os on the XC4000XL are fully 5-volt tolerant even though the V_{CC} is 3.3 volts. This allows 5 V signals to directly connect to the XC4000XL inputs without damage, as shown in Table 8. In addition, the 3.3 volt V_{CC} can be applied before or after 5 volt signals are applied to the I/Os. This makes the XC4000XL immune to power supply sequencing problems.

Registered Inputs

The I1 and I2 signals that exit the block can each carry either the direct or registered input signal.

The input and output storage elements in each IOB have a common clock enable input, which, through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC pin on the XC4000 Series CLB. It cannot be inverted within the IOB.

The storage element behavior is shown in Table 9.

Table 9: Input Register Functionality (active rising edge is shown)

Mode	Clock	Clock Enable	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	⎍	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care
⎍	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Optional Delay Guarantees Zero Hold Time

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the IOB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the IOB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the default.

The XC4000E IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC4000E global clock buffers. (See "Global Nets and Buffers (XC4000E only)" on page 33 for a description of the global clock buffers in the XC4000E.) For a shorter input register setup time, with non-zero hold, attach a NODELAY attribute or property to the flip-flop.

The XC4000X IOB has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The attributes or properties used to select the desired delay are shown in Table 10. The choices are no added attribute, MEDDELAY, and NODELAY. The default setting, with no added attribute, ensures no hold time with respect to any of the XC4000X clock buffers, including the Global Low-Skew buffers. MEDDELAY ensures no hold time with respect to the Global Early buffers. Inputs with NODELAY may have a positive hold time with respect to all clock buffers. For a description of each of these buffers, see "Global Nets and Buffers (XC4000X only)" on page 35.

Table 10: XC4000X IOB Input Delay Element

Value	When to Use
full delay (default, no attribute added)	Zero Hold with respect to Global Low-Skew Buffer, Global Early Buffer
MEDDELAY	Zero Hold with respect to Global Early Buffer
NODELAY	Short Setup, positive Hold time

Additional Input Latch for Fast Capture (XC4000X only)

The XC4000X IOB has an additional optional latch on the input. This latch, as shown in Figure 16, is clocked by the output clock — the clock used for the output flip-flop — rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the very fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To use this Fast Capture technique, drive the output clock pin (the Fast Capture latching signal) from the output of one of the Global Early buffers supplied in the XC4000X. The second storage element should be clocked by a Global Low-Skew buffer, to synchronize the incoming data to the internal logic. (See Figure 17.) These special buffers are described in "Global Nets and Buffers (XC4000X only)" on page 35.

The Fast Capture latch (FCL) is designed primarily for use with a Global Early buffer. For Fast Capture, a single clock signal is routed through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) The Fast Capture latch is clocked by the Global Early buffer, and the standard IOB flip-flop or latch is clocked by the Global Low-Skew buffer. This mode is the safest way to use the Fast Capture latch, because the clock buffers on both storage elements are driven by the same pad. There is no external skew between clock pads to create potential problems.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active-High input flip-flop. ILFLX is a transparent-Low Fast Capture latch followed by a transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB. If a single BUFG output is used to drive both clock inputs, the software automatically runs the clock through both a Global Low-Skew buffer and a Global Early buffer, and clocks the Fast Capture latch appropriately.

Figure 16 on page 19 also shows a two-tap delay on the input. By default, if the Fast Capture latch is used, the Xilinx software assumes a Global Early buffer is driving the clock, and selects MEDDELAY to ensure a zero hold time. Select the desired delay based on the discussion in the previous subsection.

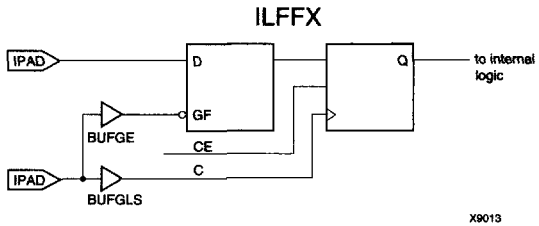


Figure 17: Examples Using XC4000X FCL

IOB Output Signals

Output signals can be optionally inverted within the IOB, and can pass directly to the pad or be stored in an edge-triggered flip-flop. The functionality of this flip-flop is shown in Table 11.

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The 4-mA maximum output current specification of many FPGAs often forces the user to add external buffers, which are especially cumbersome on bidirectional I/O lines. The XC4000E and XC4000EX/XL devices solve many of these problems by providing a guaranteed output sink current of 12 mA. Two adjacent outputs can be interconnected externally to sink up to 24 mA. The XC4000E and XC4000EX/XL FPGAs can thus directly drive buses on a printed circuit board.

By default, the output pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with p-channel pull-up transistors pulling to Vcc. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable. In the XC4000XL, all outputs are pulled to the positive supply rail.

Table 11: Output Flip-Flop Functionality (active rising edge is shown)

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	↑	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
↑	Rising edge
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

Any XC4000 Series 5-Volt device with its outputs configured in TTL mode can drive the inputs of any typical 3.3-Volt device. (For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

Supported destinations for XC4000 Series device outputs are shown in Table 12.

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 18.)

Table 12: Supported Destinations for XC4000 Series Outputs

Destination	XC4000 Series Outputs		
	3.3 V, CMOS	5 V, TTL	5 V, CMOS
Any typical device, Vcc = 3.3 V, CMOS-threshold inputs	√	√	some[1]
Any device, Vcc = 5 V, TTL-threshold inputs	√	√	√
Any device, Vcc = 5 V, CMOS-threshold inputs	Unreliable Data		√

1. Only if destination device has 5-V tolerant inputs

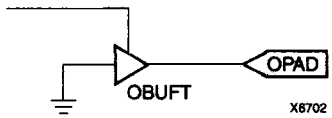


Figure 18: Open-Drain Output

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC4000E devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For XC4000X devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce. Therefore, the maximum total capacitive load is 300 pF between each external Power/Ground pin pair. Maximum loading may vary for the low-voltage devices.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC4000E devices and 600 pF for XC4000X devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC4000 Series.

XC4000 Series devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Global Three-State

A separate Global 3-State line (not shown in Figure 15 or Figure 16) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to GSR. See Figure 2 on page 9 for details.

Alternatively, GTS can be driven from any internal node.

Output Multiplexer/2-Input Function Generator (XC4000X only)

As shown in Figure 16 on page 19, the output path in the XC4000X IOB contains an additional multiplexer not available in the XC4000E IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass-gate, AND-gate, OR-gate, or XOR-gate, with 0, 1, or 2 inverted inputs. The logic used to implement these functions is shown in the upper gray area of Figure 16.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad; effectively doubling the number of device outputs without requiring a larger, more expensive package.

When the MUX is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global Early buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe Driven by a BUFGE buffer, as shown in Figure 19. The critical-path pin-to-pin delay of this circuit is less than 6 nanoseconds.

As shown in Figure 16, the IOB input pins Out, Output Clock, and Clock Enable have different delays and different flexibilities regarding polarity. Additionally, Output Clock sources are more limited than the other inputs. Therefore, the Xilinx software does not move logic into the IOB function generators unless explicitly directed to do so.

The user can specify that the IOB function generator be used, by placing special library symbols beginning with the letter "O." For example, a 2-input AND-gate in the IOB function generator is called OAND2. Use the symbol input pin labelled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 20.

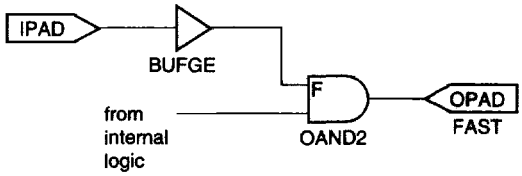


Figure 19: Fast Pin-to-Pin Path in XC4000X

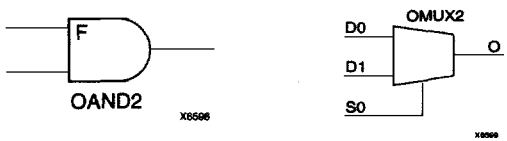


Figure 20: AND & MUX Symbols in XC4000X IOB

Other IOB Options

There are a number of other programmable options in the XC4000 Series IOB.

Pull-up and Pull-down Resistors

Programmable pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground.

The value of these resistors is 50 kΩ – 100 kΩ. This high value makes them unsuitable as wired-AND pull-up resistors.

The pull-up resistors for most user-programmable IOBs are active during the configuration process. See Table 22 on page 64 for a list of pins with pull-ups active before and during configuration.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Independent Clocks

Separate clock signals are provided for the input and output flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent, except that in the XC4000X, the Fast Capture latch shares an IOB input with the output clock pin.

Early Clock for IOBs (XC4000X only)

Special early clocks are available for IOBs. These clocks are sourced by the same sources as the Global Low-Skew buffers, but are separately buffered. They have fewer loads and therefore less delay. The early clock can drive either the IOB output clock or the IOB input clock, or both. The early clock allows fast capture of input data, and fast clock-to-output on output data. The Global Early buffers that drive these clocks are described in "Global Nets and Buffers (XC4000X only)" on page 35.

Global Set/Reset

As with the CLB registers, the Global Set/Reset signal (GSR) can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set

or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops. The choice of set or clear applies to both the initial state of the flip-flop and the response to the Global Set/Reset pulse. See "Global Set/Reset" on page 9 for a description of how to use GSR.

JTAG Support

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, permitting easy chip and board-level testing. More information is provided in "Boundary Scan" on page 40.

Three-State Buffers

A pair of 3-state buffers is associated with each CLB in the array. (See Figure 27 on page 28.) These 3-state buffers can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources. Programmable pull-up resistors attached to these longlines help to implement a wide wired-AND function.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in Table 13.

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. (See Figure 33 on page 32.)

The horizontal longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Special longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal longlines. These longlines form the wide edge decoders discussed in "Wide Edge Decoders" on page 25.

Three-State Buffer Modes

The 3-state buffers can be configured in three modes:

- Standard 3-state buffer
- Wired-AND with input on the I pin
- Wired OR-AND

Standard 3-State Buffer

All three pins are used. Place the library element BUFT. Connect the input to the I pin and the output to the O pin. The T pin is an active-High 3-state (i.e. an active-Low enable). Tie the T pin to Ground to implement a standard buffer.

Wired-AND with Input on the I Pin

The buffer can be used as a Wired-AND. Use the WAND1 library symbol, which is essentially an open-drain buffer. WAND4, WAND8, and WAND16 are also available. See the *XACT Libraries Guide* for further information.

The T pin is internally tied to the I pin. Connect the input to the I pin and the output to the O pin. Connect the outputs of all the WAND1s together and attach a PULLUP symbol.

Wired OR-AND

The buffer can be configured as a Wired OR-AND. A High level on either input turns off the output. Use the WOR2AND library symbol, which is essentially an open-drain 2-input OR gate. The two input pins are functionally equivalent. Attach the two inputs to the I0 and I1 pins and tie the output to the O pin. Tie the outputs of all the WOR2ANDs together and attach a PULLUP symbol.

Three-State Buffer Examples

Figure 21 shows how to use the 3-state buffers to implement a wired-AND function. When all the buffer inputs are High, the pull-up resistor(s) provide the High output.

Figure 22 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in Table 13.

Table 13: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN

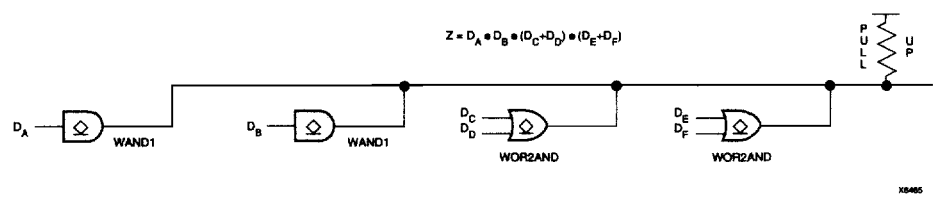


Figure 21: Open-Drain Buffers Implement a Wired-AND Function

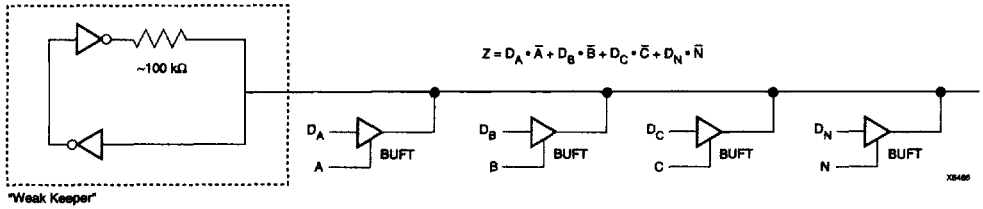


Figure 22: 3-State Buffers Implement a Multiplexer

Wide Edge Decoders

Dedicated decoder circuitry boosts the performance of wide decoding functions. When the address or data field is wider than the function generator inputs, FPGAs need multi-level decoding and are thus slower than PALs. XC4000 Series CLBs have nine inputs. Any decoder of up to nine inputs is, therefore, compact and fast. However, there is also a need for much wider decoders, especially for address decoding in large microprocessor systems.

An XC4000 Series FPGA has four programmable decoders located on each edge of the device. The inputs to each decoder are any of the IOB I1 signals on that edge plus one local interconnect per CLB row or column. Each row or column of CLBs provides up to three variables or their compliments., as shown in Figure 23. Each decoder generates a High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to a product term in typical PAL devices.

Each of these wired-AND gates is capable of accepting up to 42 inputs on the XC4005E and 72 on the XC4013E. There are up to 96 inputs for each decoder on the XC4028X and 132 on the XC4052X. The decoders may also be split in two when a larger number of narrower decoders are required, for a maximum of 32 decoders per device.

The decoder outputs can drive CLB inputs, so they can be combined with other logic to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This decoding feature covers what has long been considered a weakness of older FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000 Series device can implement these functions fast and efficiently.

To use the wide edge decoders, place one or more of the WAND library symbols (WAND1, WAND4, WAND8, WAND16). Attach a DECODE attribute or property to each WAND symbol. Tie the outputs together and attach a PULLUP symbol. Location attributes or properties such as L (left edge) or TR (right half of top edge) should also be used to ensure the correct placement of the decoder inputs.

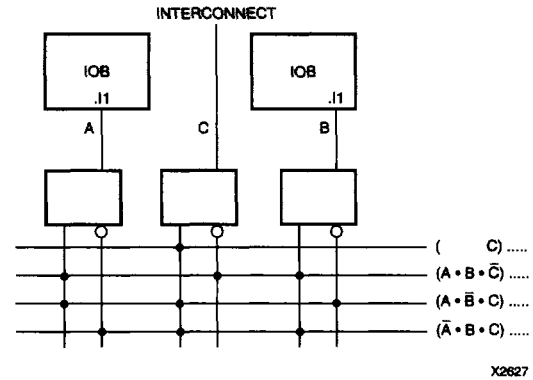


Figure 23: XC4000 Series Edge Decoding Example

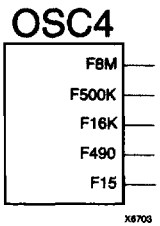


Figure 24: XC4000 Series Oscillator Symbol

On-Chip Oscillator

XC4000 Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16kHz, 490Hz and 15Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code (see Figure 24).

The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing resources is provided to achieve efficient automated routing.

The XC4000E and XC4000X share a basic interconnect structure. XC4000X devices, however, have additional routing not available in the XC4000E. The extra routing resources allow high utilization in high-capacity devices. All XC4000X-specific routing resources are clearly identified throughout this section. Any resources not identified as XC4000X-specific are present in all XC4000 Series devices.

This section describes the varied routing resources available in XC4000 Series devices. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design.

Interconnect Overview

There are several types of interconnect.

- CLB routing is associated with each row and column of the CLB array.
- IOB routing forms a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the internal logic blocks.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

Five interconnect types are distinguished by the relative length of their segments: single-length lines, double-length lines, quad and octal lines (XC4000X only), and longlines. In the XC4000X, direct connects allow fast data flow between adjacent CLBs, and between IOBs and CLBs.

Extra routing is included in the IOB pad ring. The XC4000X also includes a ring of octal interconnect lines near the IOBs to improve pin-swapping and routing to locked pins.

XC4000E/X devices include two types of global buffers. These global buffers have different properties, and are intended for different purposes. They are discussed in detail later in this section.

CLB Routing Connections

A high-level diagram of the routing resources associated with one CLB is shown in Figure 25. The shaded arrows represent routing present only in XC4000X devices.

Table 14 shows how much routing of each type is available in XC4000E and XC4000X CLB arrays. Clearly, very large designs, or designs with a great deal of interconnect, will route more easily in the XC4000X. Smaller XC4000E designs, typically requiring significantly less interconnect, do not require the additional routing.

Figure 27 on page 28 is a detailed diagram of both the XC4000E and the XC4000X CLB, with associated routing. The shaded square is the programmable switch matrix, present in both the XC4000E and the XC4000X. The L-shaped shaded area is present only in XC4000X devices. As shown in the figure, the XC4000X block is essentially an XC4000E block with additional routing.

CLB inputs and outputs are distributed on all four sides, providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.

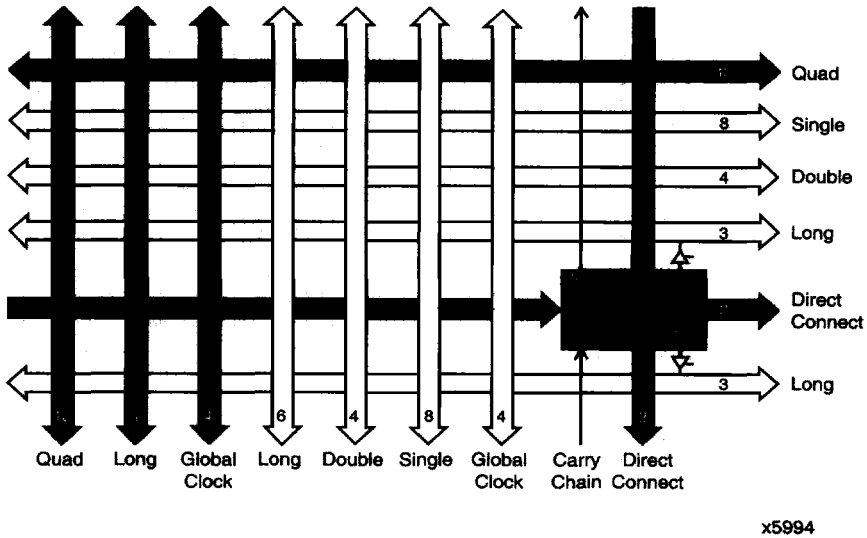


Figure 25: High-Level Routing Diagram of XC4000 Series CLB (shaded arrows indicate XC4000X only)

Table 14: Routing per CLB in XC4000 Series Devices

	XC4000E		XC4000X	
	Vertical	**Horizontal**	**Vertical**	**Horizontal**
Singles	8	8	8	8
Doubles	4	4	4	4
Quads	0	0	12	12
Longlines	6	6	10	6
Direct Connects	0	0	2	2
Globals	4	0	8	0
Carry Logic	2	0	1	0
Total	24	18	45	32

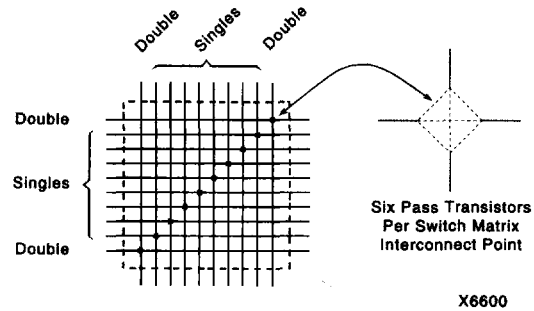


Figure 26: Programmable Switch Matrix (PSM)

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each switch matrix consists of programmable pass transistors used to establish connections between the lines (see Figure 26).

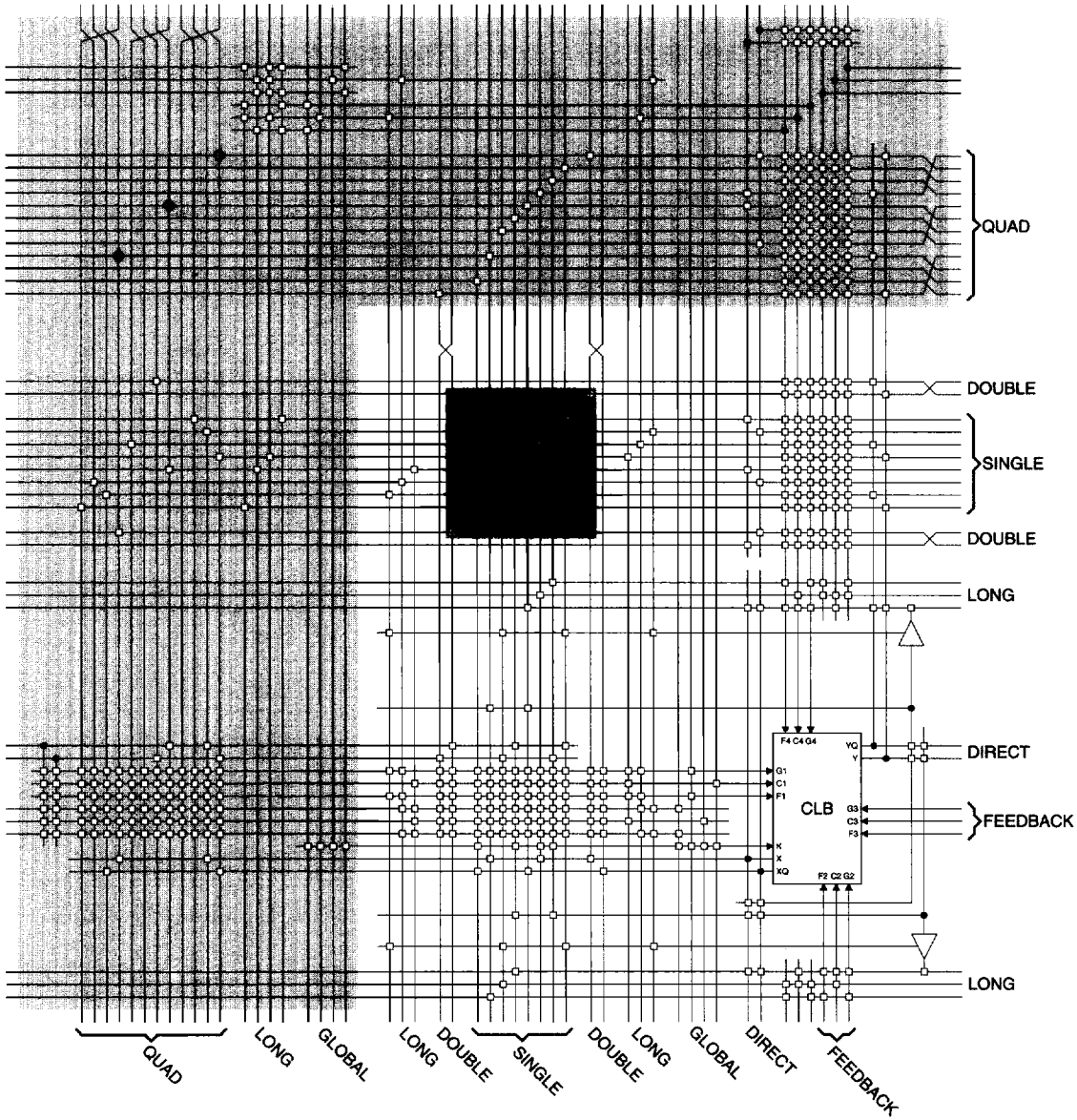
For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and a column of CLBs.

Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 28. Routing connectivity is shown in Figure 27.

Single-length lines incur a delay whenever they go through a switching matrix. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.



Common to XC4000E and XC4000X

XC4000X only

Programmable Switch Matrix

Figure 27: Detail of Programmable Interconnect Associated with XC4000 Series CLB

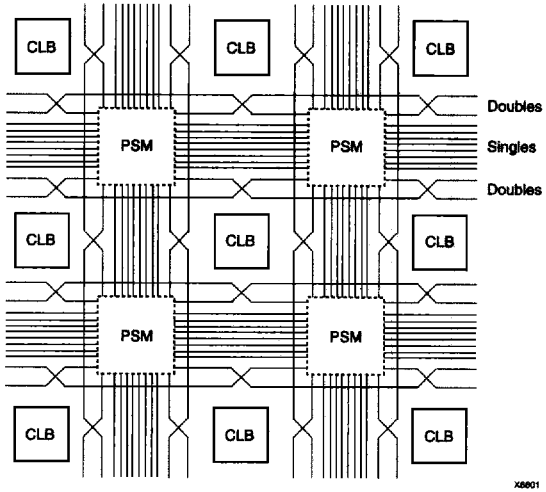


Figure 28: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a switch matrix. Double-length lines are grouped in pairs with the switch matrices staggered, so that each line goes through a switch matrix at every other row or column of CLBs (see Figure 28).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility. Double-length lines are connected by way of the programmable switch matrices. Routing connectivity is shown in Figure 27.

Quad Lines (XC4000X only)

XC4000X devices also include twelve vertical and twelve horizontal quad lines per CLB row and column. Quad lines are four times as long as the single-length lines. They are interconnected via buffered switch matrices (shown as diamonds in Figure 27 on page 28). Quad lines run past four CLBs before entering a buffered switch matrix. They are grouped in fours, with the buffered switch matrices staggered, so that each line goes through a buffered switch matrix at every fourth CLB location in that row or column. (See Figure 29.)

The buffered switch matrixes have four pins, one on each edge. All of the pins are bidirectional. Any pin can drive any or all of the other pins.

Each buffered switch matrix contains one buffer and six pass transistors. It resembles the programmable switch matrix shown in Figure 26, with the addition of a programmable buffer. There can be up to two independent inputs

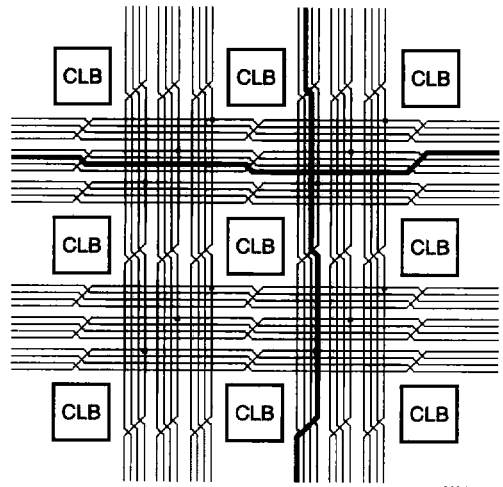


Figure 29: Quad Lines (XC4000X only)

and up to two independent outputs. Only one of the independent inputs can be buffered.

The place and route software automatically uses the timing requirements of the design to determine whether or not a quad line signal should be buffered. A heavily loaded signal is typically buffered, while a lightly loaded one is not. One scenario is to alternate buffers and pass transistors. This allows both vertical and horizontal quad lines to be buffered at alternating buffered switch matrices.

Due to the buffered switch matrices, quad lines are very fast. They provide the fastest available method of routing heavily loaded signals for long distances across the device.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances. In XC4000X devices, quad lines are preferred for critical nets, because the buffered switch matrices make them faster for high fan-out nets.

Two horizontal longlines per CLB can be driven by 3-state or open-drain drivers (TBUFs). They can therefore implement unidirectional or bidirectional buses, wide multiplexers, or wired-AND functions. (See "Three-State Buffers" on page 24 for more details.)

Each horizontal longline driven by TBUFs has either two (XC4000E) or eight (XC4000X) pull-up resistors. To activate these resistors, attach a PULLUP symbol to the longline net. The software automatically activates the appropriate number of pull-ups. There is also a weak keeper at each end of these two horizontal longlines. This circuit pre-

vents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Each XC4000E longline has a programmable splitter switch at its center, as does each XC4000X longline driven by TBUFs. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Each XC4000X longline not driven by TBUFs has a buffered programmable splitter switch at the 1/4, 1/2, and 3/4 points of the array. Due to the buffering, XC4000X longline performance does not deteriorate with the larger array sizes. If the longline is split, the resulting partial longlines are independent.

Routing connectivity of the longlines is shown in Figure 27 on page 28.

Direct Interconnect (XC4000X only)

The XC4000X offers two direct, efficient and fast connections between adjacent CLBs. These nets facilitate a data flow from the left to the right side of the device, or from the top to the bottom, as shown in Figure 30. Signals routed on the direct interconnect exhibit minimum interconnect propagation delay and use no general routing resources.

The direct interconnect is also present between CLBs and adjacent IOBs. Each IOB on the left and top device edges has a direct path to the nearest CLB. Each CLB on the right and bottom edges of the array has a direct path to the nearest two IOBs, since there are two IOBs for each row or column of CLBs.

The place and route software uses direct interconnect whenever possible, to maximize routing resources and minimize interconnect delays.

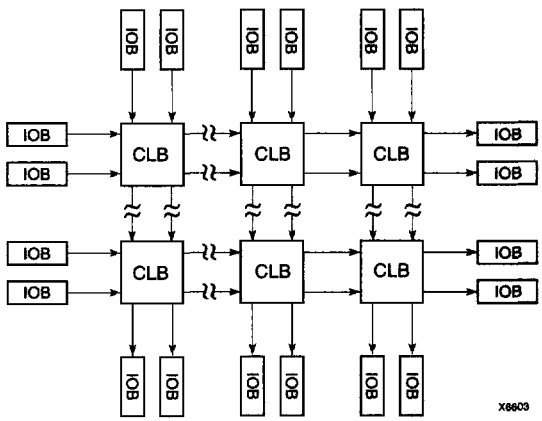


Figure 30: XC4000X Direct Interconnect

I/O Routing

XC4000 Series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines spanning two CLBs (four IOBs), and four longlines. Global lines and Wide Edge Decoder lines are provided. XC4000X devices also include eight octal lines.

A high-level diagram of the VersaRing is shown in Figure 31. The shaded arrows represent routing present only in XC4000X devices.

Figure 33 on page 32 is a detailed diagram of the XC4000E and XC4000X VersaRing. The area shown includes two IOBs. There are two IOBs per CLB row or column, therefore this diagram corresponds to the CLB routing diagram shown in Figure 27 on page 28. The shaded areas represent routing and routing connections present only in XC4000X devices.

Octal I/O Routing (XC4000X only)

Between the XC4000X CLB array and the pad ring, eight interconnect tracks provide for versatility in pin assignment and fixed pinout flexibility. (See Figure 32 on page 31.)

These routing tracks are called octals, because they can be broken every eight CLBs (sixteen IOBs) by a programmable buffer that also functions as a splitter switch. The buffers are staggered, so each line goes through a buffer at every eighth CLB location around the device edge.

The octal lines bend around the corners of the device. The lines cross at the corners in such a way that the segment most recently buffered before the turn has the farthest distance to travel before the next buffer, as shown in Figure 32.

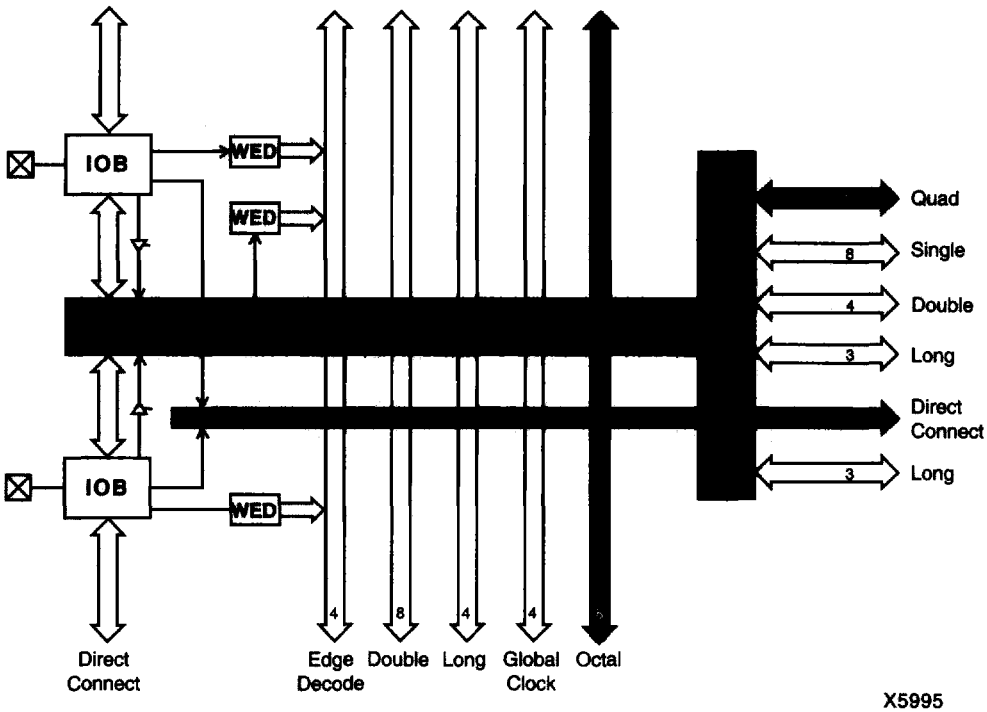


Figure 31: High-Level Routing Diagram of XC4000 Series VersaRing (Left Edge)
WED = Wide Edge Decoder, IOB = I/O Block (shaded arrows indicate XC4000X only)

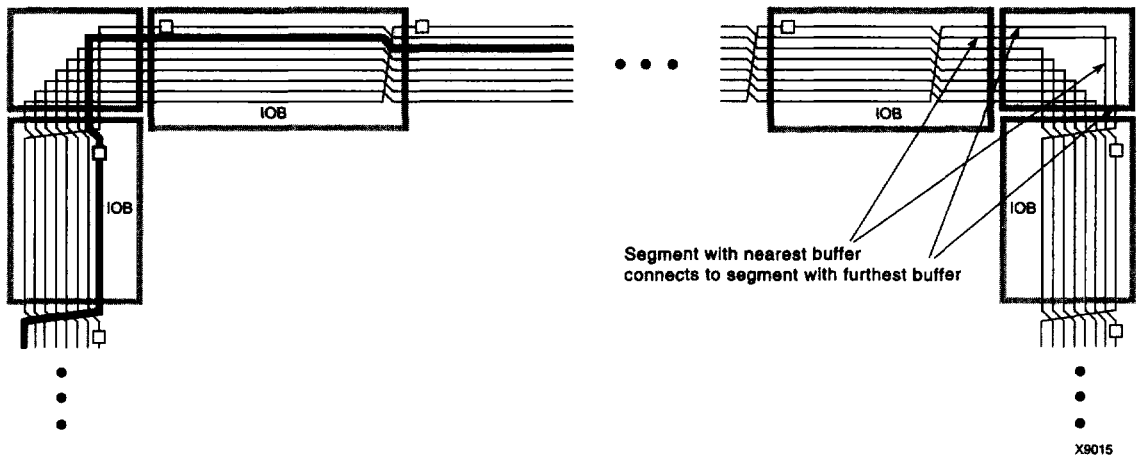


Figure 32: XC4000X Octal I/O Routing

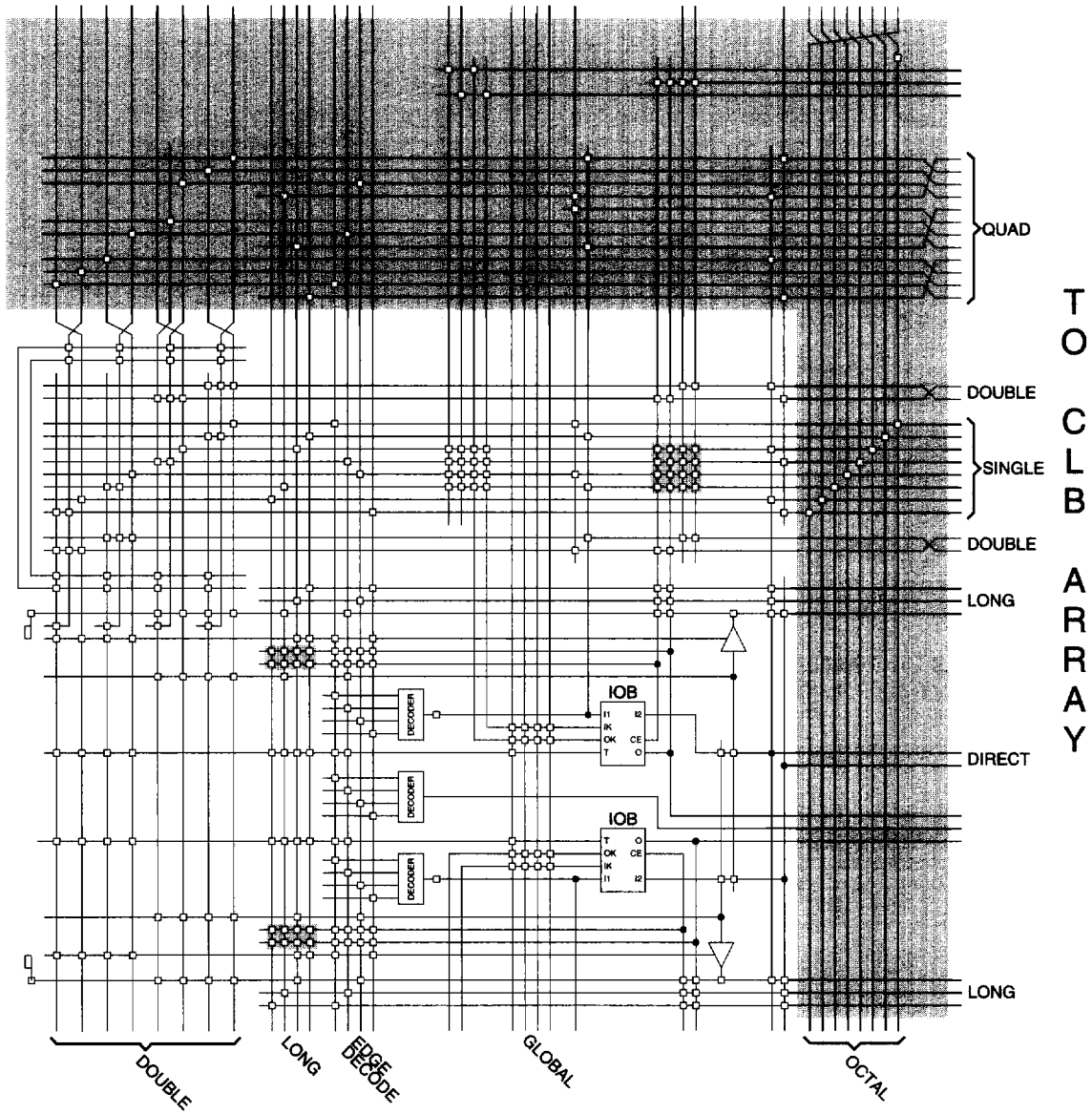


Figure 33: Detail of Programmable Interconnect Associated with XC4000 Series IOB (Left Edge)

IOB inputs and outputs interface with the octal lines via the single-length interconnect lines. Single-length lines are also used for communication between the octals and double-length lines, quads, and longlines within the CLB array.

Segmentation into buffered octals was found to be optimal for distributing signals over long distances around the device.

Global Nets and Buffers

Both the XC4000E and the XC4000X have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew. The global buffers are described in detail in the following sections. The text descriptions and diagrams are summarized in Table 15. The table shows which CLB and IOB clock pins can be sourced by which global buffers.

In both XC4000E and XC4000X devices, placement of a library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. The detailed information in these sections is included only for reference.

Global Nets and Buffers (XC4000E only)

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The four global lines can be driven by either of two types of global buffers. The clock pins of every CLB and IOB can also be sourced from local interconnect.

Two different types of clock buffers are available in the XC4000E:

- Primary Global Buffers (BUFGP)
- Secondary Global Buffers (BUFGS)

Four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs.

The Primary Global buffers must be driven by the semi-dedicated pads. The Secondary Global buffers can be sourced by either semi-dedicated pads or internal nets.

Each CLB column has four dedicated vertical Global lines. Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 34. Each corner of the device has one Primary buffer and one Secondary buffer.

IOBs along the left and right edges have four vertical global longlines. Top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), or BUFG (either primary or secondary buffer) element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=L attribute or property to a BUFGS symbol to direct that a buffer be placed in one of the two Secondary Global buffers on the left edge of the device, or a LOC=BL to indicate the Secondary Global buffer on the bottom edge of the device, on the left.

Table 15: Clock Pin Access

	XC4000E		XC4000X			Local Interconnect
	BUFGP	BUFGS	BUFGLS	L & R BUFGE	T & B BUFGE	
All CLBs in Quadrant	√	√	√	√	√	√
All CLBs in Device	√	√	√			√
IOBs on Adjacent Vertical Half Edge	√	√	√	√	√	√
IOBs on Adjacent Vertical Full Edge	√	√	√	√		√
IOBs on Adjacent Horizontal Half Edge (Direct)				√		√
IOBs on Adjacent Horizontal Half Edge (through CLB globals)	√	√	√	√	√	√
IOBs on Adjacent Horizontal Full Edge (through CLB globals)	√	√	√			√

L = Left, R = Right, T = Top, B = Bottom

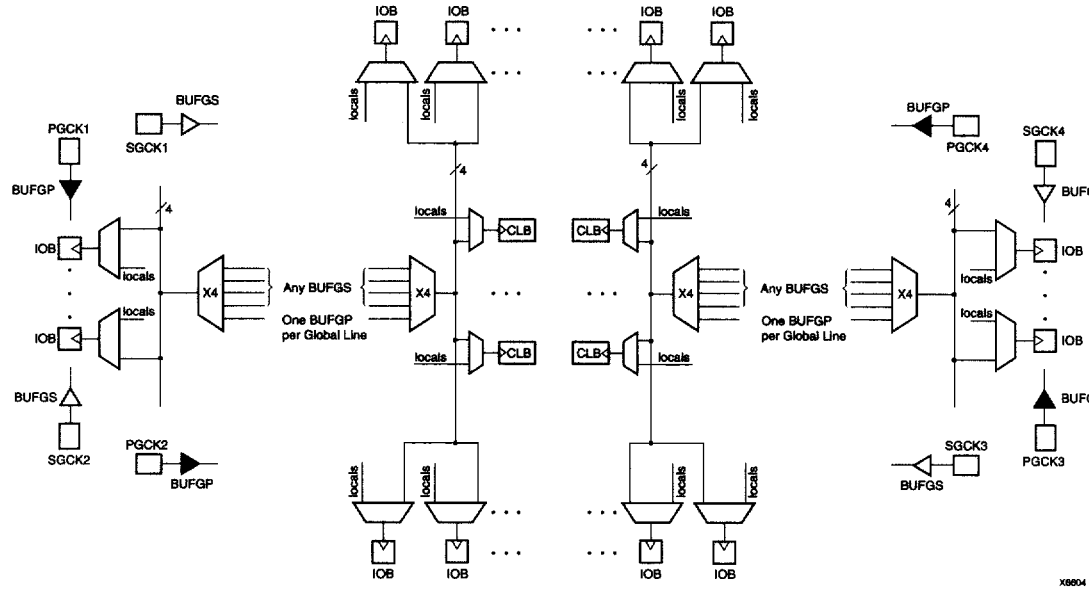


Figure 34: XC4000E Global Net Distribution

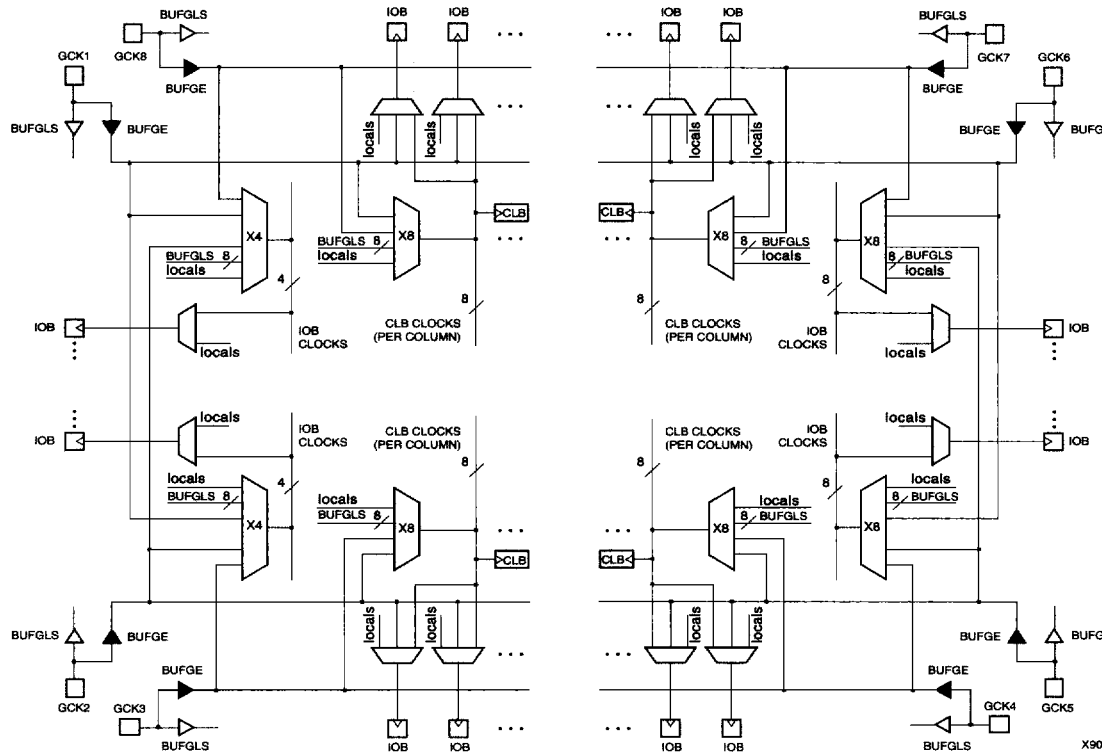


Figure 35: XC4000X Global Net Distribution

Global Nets and Buffers (XC4000X only)

Eight vertical longlines in each CLB column are driven by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The global lines are broken in the center of the array, to allow faster distribution and to minimize skew across the whole array. Each half-column global line has its own buffered multiplexer, as shown in Figure 35. The top and bottom global lines cannot be connected across the center of the device, as this connection might introduce unacceptable skew. The top and bottom halves of the global lines must be separately driven — although they can be driven by the same global buffer.

The eight global lines in each CLB column can be driven by either of two types of global buffers. They can also be driven by internal logic, because they can be accessed by single, double, and quad lines at the top, bottom, half, and quarter points. Consequently, the number of different clocks that can be used simultaneously in an XC4000X device is very large.

There are four global lines feeding the IOBs at the left edge of the device. IOBs along the right edge have eight global lines. There is a single global line along the top and bottom edges with access to the IOBs. All IOB global lines are broken at the center. They cannot be connected across the center of the device, as this connection might introduce unacceptable skew.

IOB global lines can be driven from two types of global buffers, or from local interconnect. Alternatively, top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

Two different types of clock buffers are available in the XC4000X:

- Global Low-Skew Buffers (BUFGLS)
- Global Early Buffers (BUFGE)

Global Low-Skew Buffers are the standard clock buffers. They should be used for most internal clocking, whenever a large portion of the device must be driven.

Global Early Buffers are designed to provide a faster clock access, but CLB access is limited to one-fourth of the device. They also facilitate a faster I/O interface.

Figure 35 is a conceptual diagram of the global net structure in the XC4000X.

Global Early buffers and Global Low-Skew buffers share a single pad. Therefore, the same IPAD symbol can drive one buffer of each type, in parallel. This configuration is particularly useful when using the Fast Capture latches, as described in "IOB Input Signals" on page 18. Paired Global Early and Global Low-Skew buffers share a common input; they cannot be driven by two different signals.

Choosing an XC4000X Clock Buffer

The clocking structure of the XC4000X provides a large variety of features. However, it can be simple to use, without understanding all the details. The software automatically handles clocks, along with all other routing, when the appropriate clock buffer is placed in the design. In fact, if a buffer symbol called BUFG is placed, rather than a specific type of buffer, the software even chooses the buffer most appropriate for the design. The detailed information in this section is provided for those users who want a finer level of control over their designs.

If fine control is desired, use the following summary and Table 15 on page 33 to choose an appropriate clock buffer.

- The simplest thing to do is to use a Global Low-Skew buffer.
- If a faster clock path is needed, try a BUFG. The software will first try to use a Global Low-Skew Buffer. If timing requirements are not met, a faster buffer will automatically be used.
- If a single quadrant of the chip is sufficient for the clocked logic, and the timing requires a faster clock than the Global Low-Skew buffer, use a Global Early buffer.

Global Low-Skew Buffers

Each corner of the XC4000X device has two Global Low-Skew buffers. Any of the eight Global Low-Skew buffers can drive any of the eight vertical Global lines in a column of CLBs. In addition, any of the buffers can drive any of the four vertical lines accessing the IOBs on the left edge of the device, and any of the eight vertical lines accessing the IOBs on the right edge of the device. (See Figure 36 on page 36.)

IOBs at the top and bottom edges of the device are accessed through the vertical Global lines in the CLB array, as in the XC4000E. Any Global Low-Skew buffer can, therefore, access every IOB and CLB in the device.

The Global Low-Skew buffers can be driven by either semi-dedicated pads or internal logic.

To use a Global Low-Skew buffer, instantiate a BUFGLS element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGLS be placed in one of the two Global Low-Skew buffers on the top edge of the device, or a LOC=TR to indicate the Global Low-Skew buffer on the top edge of the device, on the right.

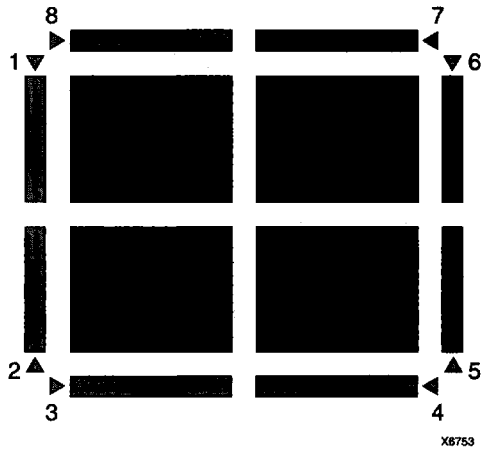


Figure 36: Any BUFGLS (GCK1 - GCK8) Can Drive Any or All Clock Inputs on the Device

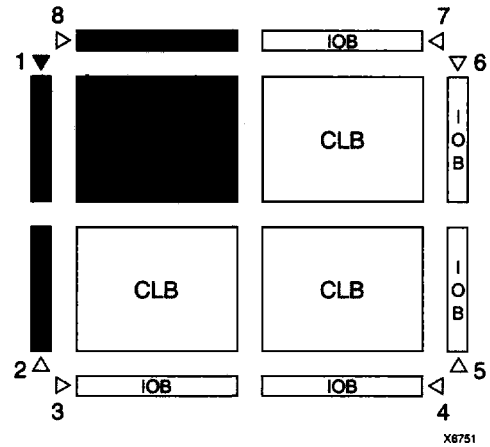


Figure 37: Left and Right BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant or Edge (GCK1 is shown. GCK2, GCK5 and GCK6 are similar.)

Global Early Buffers

Each corner of the XC4000X device has two Global Early buffers. The primary purpose of the Global Early buffers is to provide an earlier clock access than the potentially heavily-loaded Global Low-Skew buffers. A clock source applied to both buffers will result in the Global Early clock edge occurring several nanoseconds earlier than the Global Low-Skew buffer clock edge, due to the lighter loading.

Global Early buffers also facilitate the fast capture of device inputs, using the Fast Capture latches described in "IOB Input Signals" on page 18. For Fast Capture, take a single clock signal, and route it through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) Use the Global Early buffer to clock the Fast Capture latch, and the Global Low-Skew buffer to clock the normal input flip-flop or latch, as shown in Figure 17 on page 21.

The Global Early buffers can also be used to provide a fast Clock-to-Out on device output pins. However, an early clock in the output flip-flop IOB must be taken into consideration when calculating the internal clock speed for the design.

The Global Early buffers at the left and right edges of the chip have slightly different capabilities than the ones at the top and bottom. Refer to Figure 37, Figure 38, and Figure 35 on page 34 while reading the following explanation.

Each Global Early buffer can access the eight vertical Global lines for all CLBs in the quadrant. Therefore, only one-fourth of the CLB clock pins can be accessed. This restriction is in large part responsible for the faster speed of the buffers, relative to the Global Low-Skew buffers.

The left-side Global Early buffers can each drive two of the four vertical lines accessing the IOBs on the entire left edge of the device. The right-side Global Early buffers can each drive two of the eight vertical lines accessing the IOBs on the entire right edge of the device. (See Figure 37.)

Each left and right Global Early buffer can also drive half of the IOBs along either the top or bottom edge of the device, using a dedicated line that can only be accessed through the Global Early buffers.

The top and bottom Global Early buffers can drive half of the IOBs along either the left or right edge of the device, as shown in Figure 38. They can only access the top and bottom IOBs via the CLB global lines.

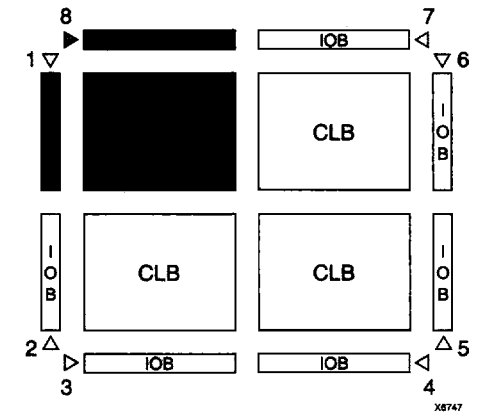


Figure 38: Top and Bottom BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant (GCK8 is shown. GCK3, GCK4 and GCK7 are similar.)

The top and bottom Global Early buffers are about 1 ns slower clock to out than the left and right Global Early buffers.

The Global Early buffers can be driven by either semi-dedicated pads or internal logic. They share pads with the Global Low-Skew buffers, so a single net can drive both global buffers, as described above.

To use a Global Early buffer, place a BUFGE element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGE be placed in one of the two Global Early buffers on the top edge of the device, or a LOC=TR to indicate the Global Early buffer on the top edge of the device, on the right.

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in Figure 39. An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically, a 0.1 µF capacitor connected between each Vcc pin and the board's Ground plane will provide adequate decoupling.

Output buffers capable of driving/sinking the specified 12 mA loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.

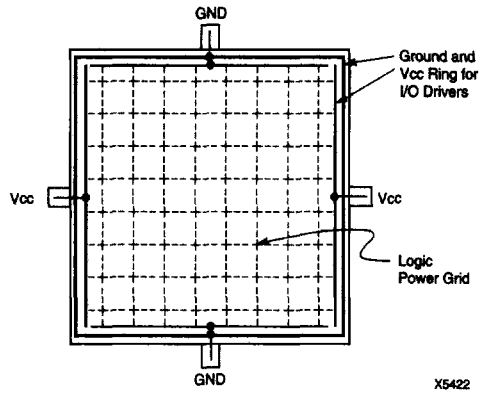


Figure 39: XC4000 Series Power Distribution

Pin Descriptions

There are three types of pins in the XC4000 Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 kΩ - 100 kΩ pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 kΩ - 100 kΩ pull-up resistor.

XC4000 Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See "Global Set/Reset" on page 9 for more information on GSR.

XC4000 Series devices have no Powerdown control input, as the XC3000 and XC2000 families do. The XC3000/XC2000 Powerdown control also 3-stated all of the device I/O pins. For XC4000 Series devices, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode. See "IOB Output Signals" on page 21 for more information on GTS.

Device pins for XC4000 Series devices are described in Table 16. Pin functions during configuration for each of the seven configuration modes are summarized in Table 22 on page 64, in the "Configuration Timing" section.

Table 16: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
VCC	I	I	Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for low-voltage devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 µF capacitor to Ground.
GND	I	I	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode and Synchronous Peripheral mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High time restriction on XC4000 Series devices, except during Readback. See "Violating the Maximum High and Low Time Specification for the Readback Clock" on page 54 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the XACT*step* program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
User I/O Pins That Can Have Special Functions			
RDY/$\overline{\text{BUSY}}$	O	I/O	During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/$\overline{\text{BUSY}}$ is a user-programmable I/O pin. RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pull-up prior to $\overline{\text{INIT}}$ going High.
$\overline{\text{RCLK}}$	O	I/O	During Master Parallel configuration, each change on the A0-A17 outputs (A0 - A21 for XC4000X) is preceded by a rising edge on $\overline{\text{RCLK}}$, a redundant output signal. $\overline{\text{RCLK}}$ is useful for clocked PROMs. It is rarely used during configuration. After configuration, $\overline{\text{RCLK}}$ is a user-programmable I/O pin.
M0, M1, M2	I	I (M0), O (M1), I (M2)	As Mode inputs, these pins are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers. During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors. A pull-down resistor value of 4.7 kΩ is recommended. These pins can only be used as inputs or outputs when called out by special schematic definitions. To use these pins, place the library components MD0, MD1, and MD2 instead of the usual pad symbols. Input or output buffers must still be used.
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.

Table 16: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (XC4000X only)	Weak Pull-up	I or I/O	Eight inputs can each drive a Global Low-Skew buffer. In addition, each can drive a Global Early buffer. Each pair of global buffers can also be driven from internal logic, but must share an input signal. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFGLS or BUFGE symbol is automatically placed on one of these pins.
$\overline{\text{CS0}}$, CS1, $\overline{\text{WS}}$, $\overline{\text{RS}}$	I	I/O	These four inputs are used in Asynchronous Peripheral mode. The chip is selected when $\overline{\text{CS0}}$ is Low and CS1 is High. While the chip is selected, a Low on Write Strobe ($\overline{\text{WS}}$) loads the data present on the D0 - D7 inputs into the internal data buffer. A Low on Read Strobe ($\overline{\text{RS}}$) changes D7 into a status output — High if Ready, Low if Busy — and drives D0 - D6 High. In Express mode, CS1 is used as a serial-enable signal for daisy-chaining. $\overline{\text{WS}}$ and $\overline{\text{RS}}$ should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.
A0 - A17	O	I/O	During Master Parallel configuration, these 18 output pins address the configuration EPROM. After configuration, they are user-programmable I/O pins.

Table 16: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
A18 - A21 (XC4000X only)	O	I/O	During Master Parallel configuration with an XC4000X master, these 4 output pins add 4 more bits to address the configuration EPROM. After configuration, they are user-programmable I/O pins. (See Master Parallel Configuration section for additional details.)
D0 - D7	I	I/O	During Master Parallel and Peripheral configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. During Parallel configuration, DIN is the D0 input. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During configuration in any mode but Express mode, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor (50 kΩ - 100 kΩ) that defines the logic level as High.

Boundary Scan

The 'bed of nails' has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The XC4000 Series implements IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: "*Boundary Scan in XC4000 Devices*."

Figure 40 on page 41 shows a simplified block diagram of the XC4000E Input/Output Block with boundary scan implemented. XC4000X boundary scan logic is identical.

Figure 41 on page 42 is a diagram of the XC4000 Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

XC4000 Series devices can also be configured through the boundary scan logic. See "Readback" on page 53.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. $\overline{\text{PROGRAM}}$, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is

always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

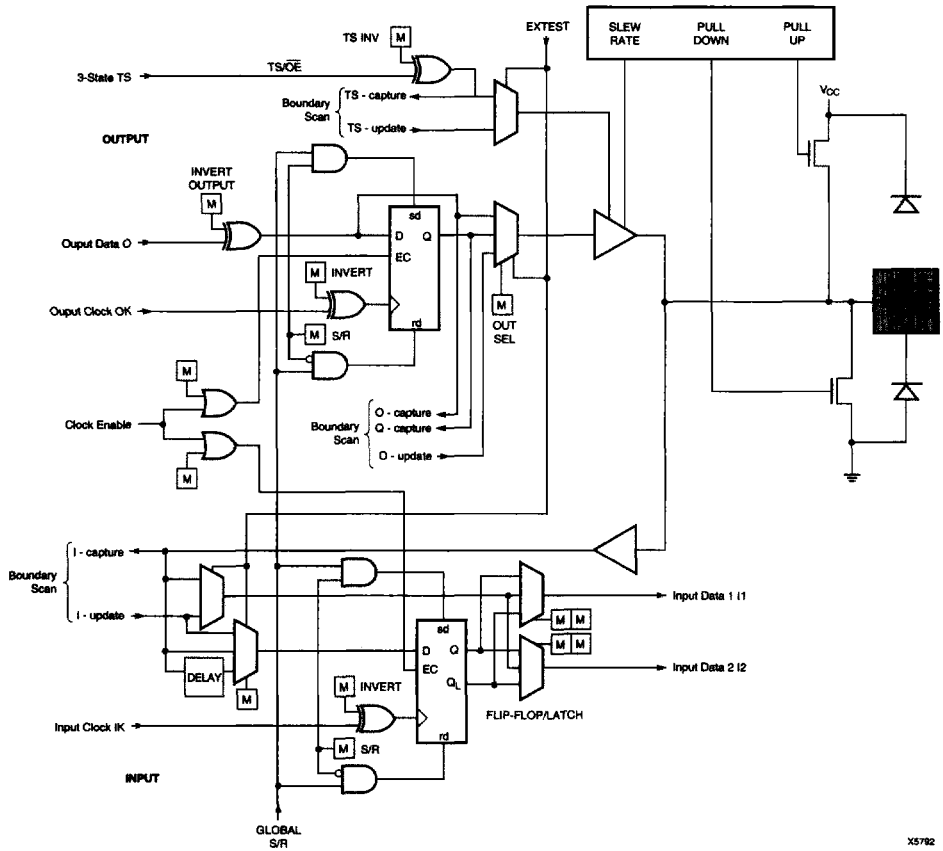


Figure 40: Block Diagram of XC4000E IOB with Boundary Scan (some details not shown). XC4000X Boundary Scan Logic is Identical.

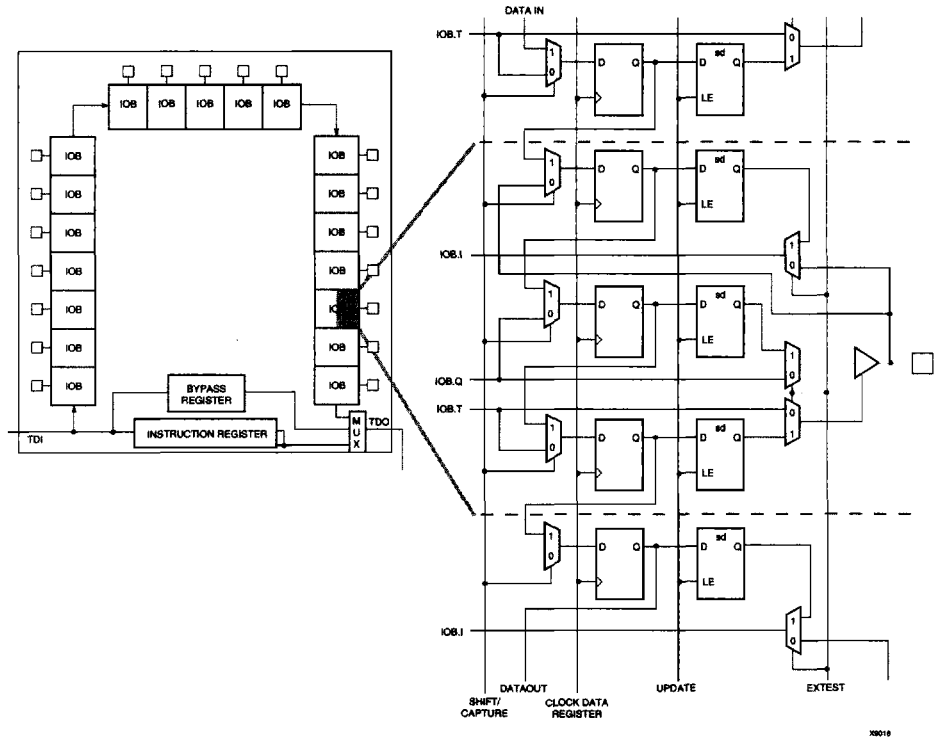


Figure 41: XC4000 Series Boundary Scan Logic

Instruction Set

The XC4000 Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 17.

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only M0 and M2 mode pins contribute only the In bit to the boundary scan I/O data register, while the output-only M1 pin contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in XDE or Epic), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 42. The device-specific pinout tables for the XC4000 Series include the boundary scan locations for each IOB pin.

BSDL (Boundary Scan Description Language) files for XC4000 Series devices are available on the Xilinx FTP site.

Including Boundary Scan in a Schematic

If boundary scan is only to be used during configuration, no special schematic elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 43.

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Table 17: Boundary Scan Instructions

Instruction I2	I1	I0	Test Selected	TDO Source	I/O Data Source
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	Reserved	—	—
1	1	1	BYPASS	Bypass Register	—

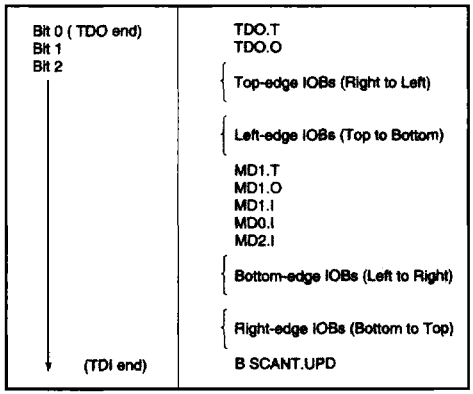


Figure 42: Boundary Scan Bit Sequence

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—don't toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note XAPP 017.001, "*Boundary Scan in XC4000E Devices.*"

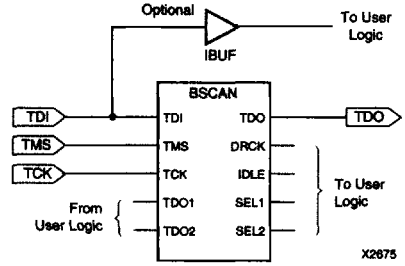


Figure 43: Boundary Scan Schematic Example

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC4000 Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT*step* development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary connections. M2 and M0 can be used as inputs, and M1 can be used as an output. The XACT*step* development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC4000 Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

XC4000E devices have six configuration modes. XC4000X devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The coding for mode selection is shown in Table 18.

Table 18: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Reserved	0	1	0	—	—
Reserved	0	0	1	—	—

Note: * Peripheral Synchronous can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 22 on page 64.

Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF (3FFFFF when 22 address lines are used), for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

Additional Address lines in XC4000 devices

The XC4000X devices have additional address lines (A18-A21) allowing the additional address space required to daisy-chain several large devices.

The extra address lines are programmable in XC4000EX devices. By default these address lines are not activated. In the default mode, the devices are compatible with existing XC4000 and XC4000E products. If desired, the extra address lines can be used by specifying the address lines option in bitgen as 22 (bitgen -g AddressLines:22). The lines (A18-A21) are driven when a master device detects, via the bitstream, that it should be using all 22 address lines. Because these pins will initially be pulled high by internal pull-ups, designers using Master Parallel Up mode should use external pull down resistors on pins A18-A21. If Master Parallel Down mode is used external resistors are not necessary.

All 22 address lines are always active in Master Parallel modes with XC4000XL devices. The additional address lines behave identically to the lower order address lines. If the Address Lines option in bitgen is set to 18, it will be ignored by the XC4000XL device.

The additional address lines (A18-A21) are not available in the PC84 package.

Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/$\overline{\text{BUSY}}$ status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 51 on page 56. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count,

is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. Figure 47 on page 51 shows the start-up timing for an XC4000 Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, and XC4000 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. The lead device must belong to the highest family in the chain. If the chain contains XC4000 Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in Figure 47 on page 51. Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of Figure 47. The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC4000 Series device, not reaching F means that readback cannot be initiated and most boundary scan instructions cannot be used.

The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using options in the bitstream generation software.

XC3000 Master with an XC4000 Series Slave

Some designers want to use an inexpensive lead device in peripheral mode and have the more precious I/O pins of the XC4000 Series devices all available for user I/O. Figure 44 provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC4000 Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.

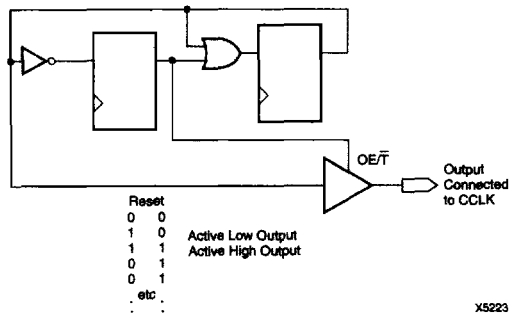


Figure 44: CCLK Generation for XC3000 Master Driving an XC4000 Series Slave

Setting CCLK Frequency

For Master modes, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for XC4000E and XC4000EX devices and from 0.6 MHz to 1.8 MHz for XC4000XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for XC4000EX devices and from 5 MHz to 15 MHz for XC4000XL devices. The frequency is selected by an option when running the bitstream generation software. If an XC4000 Series Master is driving an XC3000- or XC2000-family slave, slow CCLK mode must be used. In addition, an XC4000XL device driving a XC4000E or XC4000EX should use slow mode. Slow mode is the default.

Table 19: XC4000 Series Data Stream Formats

Data Type	All Other Modes (D0...)
Fill Byte	11111111b
Preamble Code	0010b
Length Count	COUNT(23:0)
Fill Bits	1111b
Start Field	0b
Data Frame	DATA(n-1:0)
CRC or Constant Field Check	xxxx (CRC) or 0110b
Extend Write Cycle	—
Postamble	01111111b
Start-Up Bytes	xxh

LEGEND:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Data Stream Format

The data stream ("bitstream") format is identical for all configuration modes.

The data stream formats are shown in Table 19. Bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones. This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 20 and Table 21). Each frame begins with a start field and ends with an error check. A postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling Vcc.

Table 20: XC4000E Program Data

Device	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E
Max Logic Gates	3,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLBs (Row x Col.)	100 (10 x 10)	196 (14 x 14)	256 (16 x 16)	324 (18 x 18)	400 (20 x 20)	576 (24 x 24)	784 (28 x 28)	1,024 (32 x 32)
IOBs	80	112	128	144	160	192	224	256
Flip-Flops	360	616	768	936	1,120	1,536	2,016	2,560
Horizontal Longlines	20	28	32	36	40	48	56	64
TBUFs per Longline	12	16	18	20	22	26	30	34
Bits per Frame	126	166	186	206	226	266	306	346
Frames	428	572	644	716	788	932	1,076	1,220
Program Data	53,936	94,960	119,792	147,504	178,096	247,920	329,264	422,128
PROM Size (bits)	53,984	95,008	119,840	147,552	178,144	247,968	329,312	422,176

Notes: 1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40 (header) + 8
2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.

Table 21: XC4000EX/XL Program Data

Device	XC4005	XC4010	XC4013	XC4020	XC4028	XC4036	XC4044	XC4052	XC4062	XC4085
Max Logic Gates	5,000	10,000	13,000	20,000	28,000	36,000	44,000	52,000	62,000	85,000
CLBs	196	400	576	784	1,024	1,296	1,600	1,936	2,304	3,136
(Row x Column)	14 x 14	20 x 20	24 x 24	28 x 28	32 x 32	36 x 36	40 x 40	44 x 44	48 x 48	56 x 56
IOBs	112	160	192	224	256	288	320	352	384	448
Flip-Flops	616	1,120	1,536	2,016	2,560	3,168	3,840	4,576	5,376	7,168
Bits per Frame	205	277	325	373	421	469	517	565	613	709
Frames	741	1,023	1,211	1,399	1,587	1,775	1,963	2,151	2,339	2,715
Program Data	151,910	283,376	393,580	521,832	668,132	832,480	1,014,876	1,215,320	1,433,812	1,924,940
PROM Size (bits)	151,960	283,424	393,632	521,880	668,184	832,528	1,014,928	1,215,368	1,433,864	1,924,992

Notes: 1. Bits per frame = (12 x number of rows) + 8 for the top + 16 for the bottom + 8 + 1 start bit + 4 error check bits.
Frames = (47 x number of columns) + 27 for the left edge + 52 for the right edge + 4.
Program data = (bits per frame x number of frames) + 5 postamble bits.
PROM size = (program data + 40 header bits + 8 start bits) rounded up to the nearest byte.
2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading "ones" at the beginning of the header.t

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 19. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 45. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

Configuration Sequence

There are four major steps in the XC4000 Series power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 46.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms, and up to 10% longer in the low-voltage devices. The delay is four times as long when in Master Modes (M0 Low), to allow ample time for all slaves to reach a stable Vcc. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin

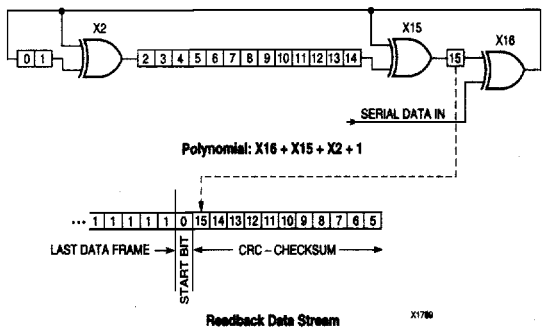


Figure 45: Circuit for Generating CRC-16

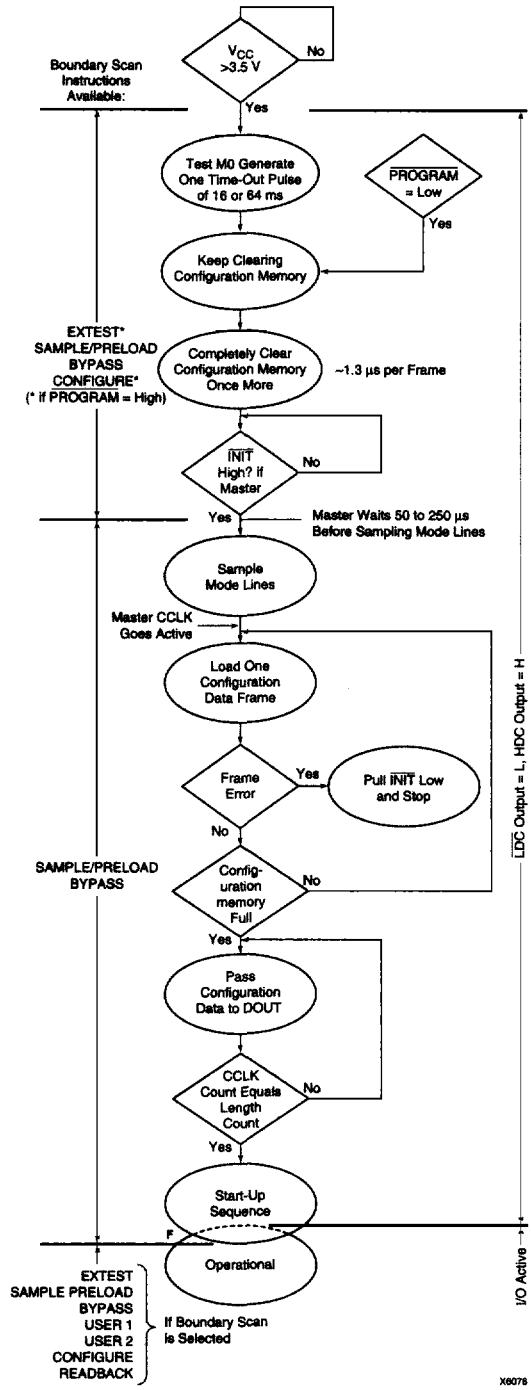


Figure 46: Power-up Configuration Sequence

Low. During this time delay, or as long as the $\overline{\text{PROGRAM}}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{\text{PROGRAM}}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{\text{INIT}}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{\text{LDC}}$, $\overline{\text{INIT}}$ and DONE provide status outputs for the system interface. The outputs $\overline{\text{LDC}}$, $\overline{\text{INIT}}$ and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain $\overline{\text{INIT}}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay of 50 to 250 µs (up to 10% longer for low-voltage devices) before a Master-mode device recognizes an inactive $\overline{\text{INIT}}$. Two internal clocks after the $\overline{\text{INIT}}$ pin is recognized as High, the FPGA samples the three mode lines to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 46 on page 48.)

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the FPGA keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the $\overline{\text{INIT}}$ input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output. The XC4000 Series $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{\text{INIT}}$ is High.

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 47 describes start-up timing for the three Xilinx families in detail. The configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the STARTUP library symbol.

Start-up Timing

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence. DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility. DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000 Series offers additional flexibility. The three events — DONE going High, the internal Set/Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in the bitstream generation software.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 47, but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

XC4000 Series offers another start-up clocking option, UCLK_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since $\overline{\text{INIT}}$ went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in Figure 48. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK_SYNC or UCLK_SYNC.

When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK_NOSYNC or UCLK_NOSYNC.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 47 show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

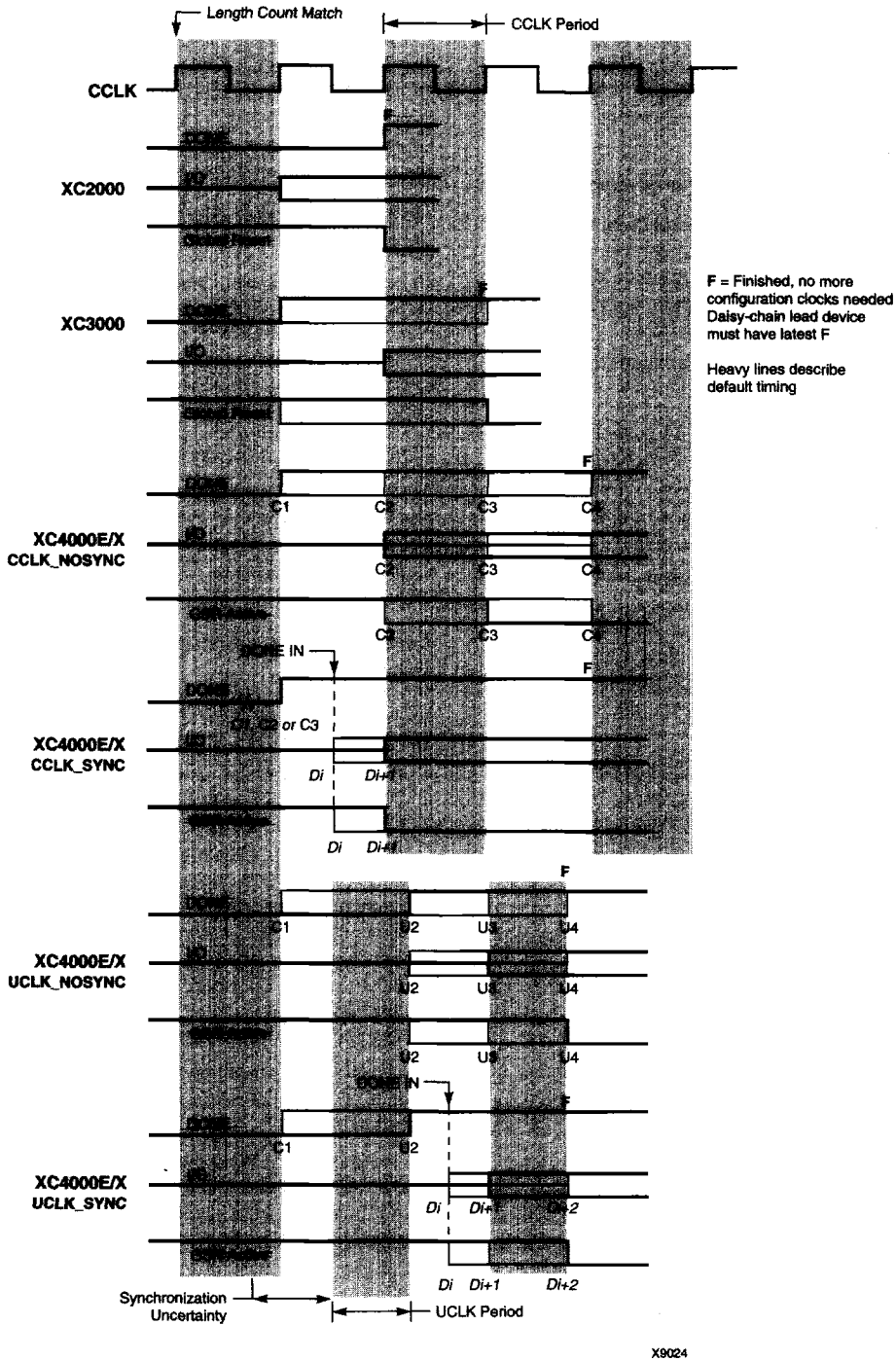


Figure 47: Start-up Timing

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

DONE Goes High to Signal End of Configuration

XC4000 Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly.*

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [2^{24} * CCLK period] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

The DONE pin for each device goes High when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

Release of User I/O After DONE Goes High

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 50 kΩ - 100 kΩ pull-up. The delay from DONE High to active user I/O is controlled by an option to the bitstream generation software.

Release of Global Set/Reset After DONE Goes High

By default, Global Set/Reset (GSR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial set or reset state. The delay from DONE High to GSR inactive is controlled by an option to the bitstream generation software.

Configuration Complete After DONE Goes High

Three full CCLK cycles are required after the DONE pin goes High, as shown in Figure 47 on page 51. If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

Configuration Through the Boundary Scan Pins

XC4000 Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with $\overline{\text{INIT}}$ held Low (or drive the $\overline{\text{PROGRAM}}$ pin Low for more than 300 ns followed by a High while holding $\overline{\text{INIT}}$ Low). Holding $\overline{\text{INIT}}$ Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold $\overline{\text{INIT}}$ Low.
- Issue the CONFIG command to the TMS input
- Wait for $\overline{\text{INIT}}$ to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, "*Boundary Scan in XC4000 Devices*." This application note also applies to XC4000E and XC4000X devices.

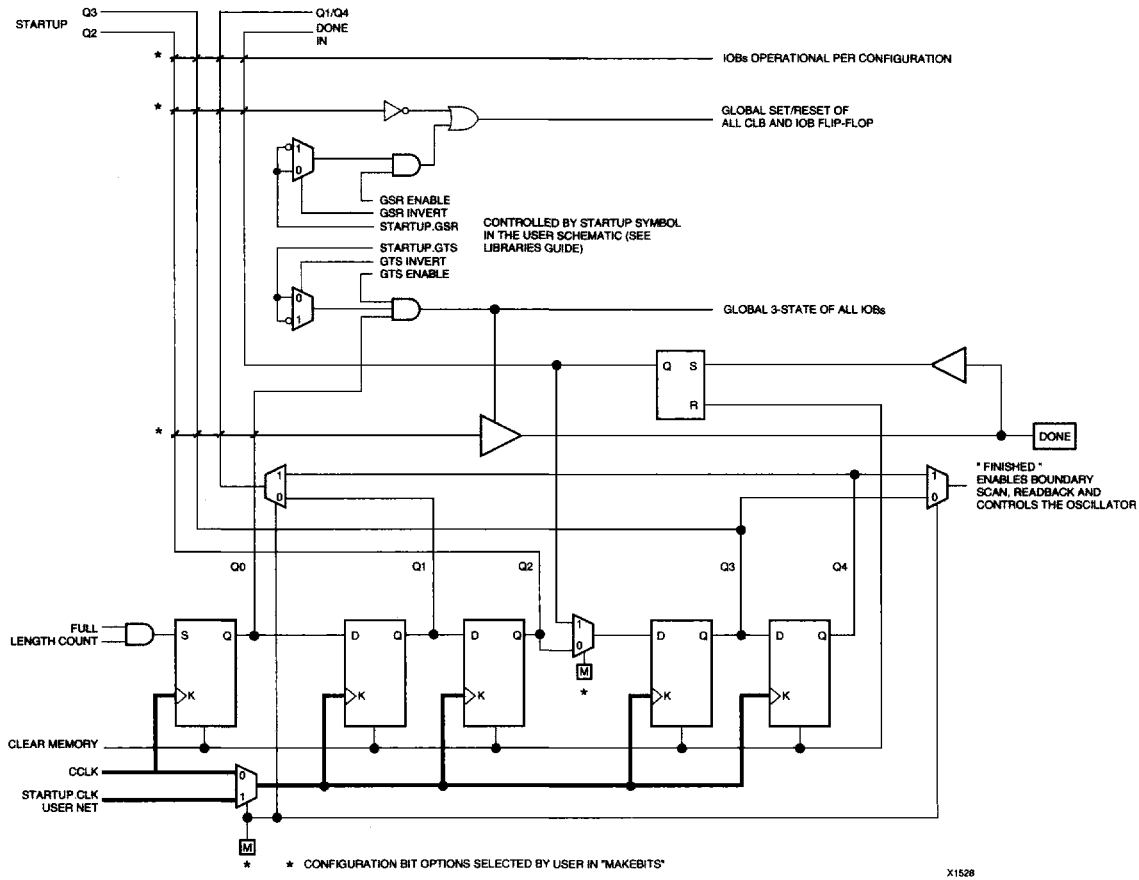


Figure 48: Start-up Logic

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000 Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

XC4000 Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 49.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

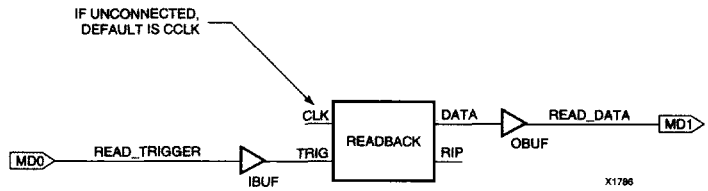


Figure 49: Readback Schematic Example

Readback Options

Readback options are: Read Capture, Read Abort, and Clock Select. They are set with the bitstream generation software.

Read Capture

When the Read Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted.

When the Read Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

RDBK.TRIG is located in the lower-left corner of the device, as shown in Figure 50.

Read Abort

When the Read Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

RDBK.CLK is located in the lower right chip corner, as shown in Figure 50.

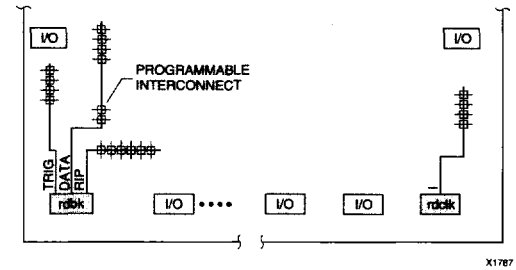


Figure 50: READBACK Symbol in Graphical Editor

Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 19, Table 20 and Table 21.

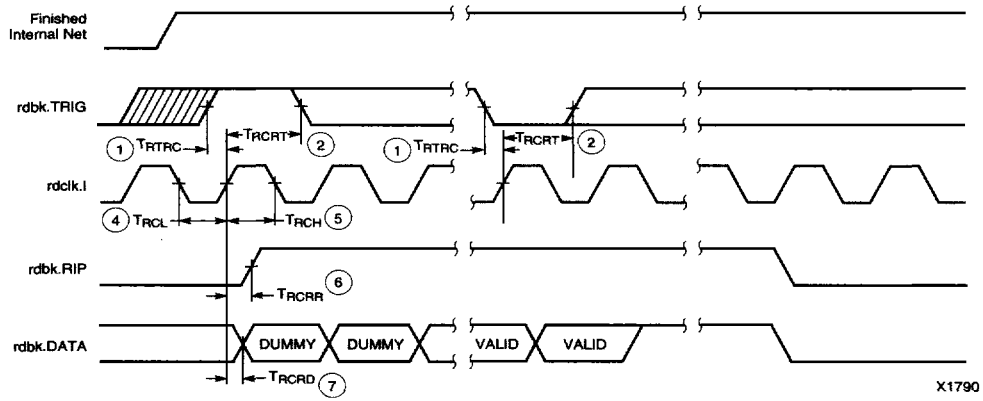
Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

XC4000E/EX/XL Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



E/EX

	Description	Symbol		Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1	T_{RTRC}	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2	T_{RCRT}	50	-	ns
rdclk.1	rdbk.DATA delay	7	T_{RCRD}	-	250	ns
	rdbk.RIP delay	6	T_{RCRR}	-	250	ns
	High time	5	T_{RCH}	250	500	ns
	Low time	4	T_{RCL}	250	500	ns

Note 1: Timing parameters apply to all speed grades.
Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

XL

	Description	Symbol		Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1	T_{RTRC}	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2	T_{RCRT}	50	-	ns
rdclk.1	rdbk.DATA delay	7	T_{RCRD}	-	250	ns
	rdbk.RIP delay	6	T_{RCRR}	-	250	ns
	High time	5	T_{RCH}	250	500	ns
	Low time	4	T_{RCL}	250	500	ns

Note 1: Timing parameters apply to all speed grades.
Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 51 shows a full master/slave system. An XC4000 Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

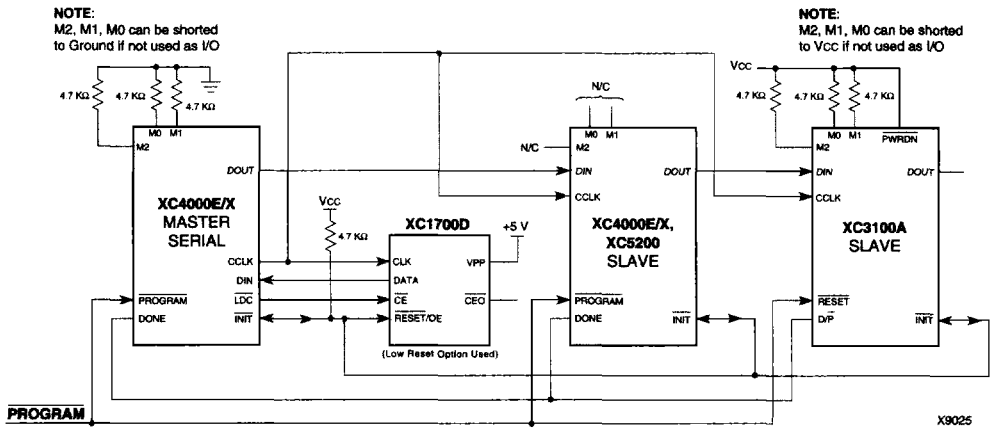
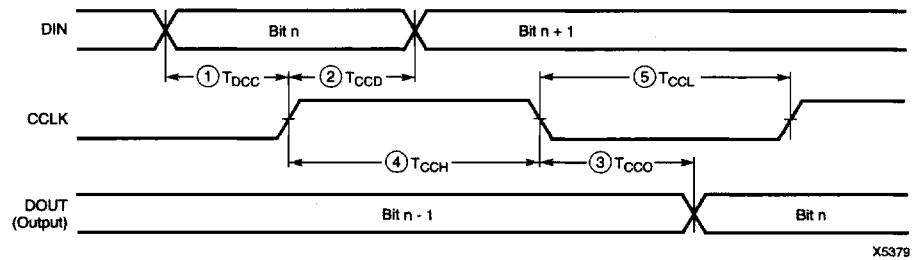


Figure 51: Master/Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 52: Slave Serial Mode Programming Switching Characteristics

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

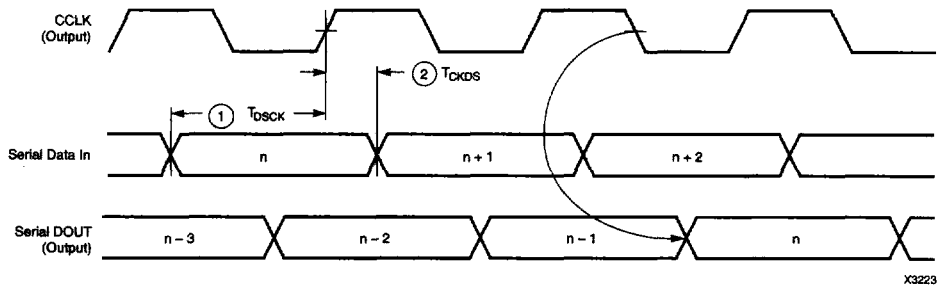
The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In the bitstream generation software, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to page 4-67. Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

Figure 51 on page 56 shows a full master/slave system. The leftmost device is in Master Serial mode.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DSCK}	20		ns
	DIN hold	2	T_{CKDS}	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{PROGRAM}$ Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 53: Master Serial Mode Programming Switching Characteristics

Master Parallel Modes

In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decrementing the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

The PROM address pins can be incremented or decremented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of microprocessors and microcontrollers. Some processors must boot from the bottom of memory (all zeros) while others must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the memory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at 3FFFF and decrement.

Additional Address lines in XC4000 devices

The XC4000X devices have additional address lines (A18-A21) allowing the additional address space required to daisy-chain several large devices.

The extra address lines are programmable in XC4000EX devices. By default these address lines are not activated. In the default mode, the devices are compatible with existing XC4000 and XC4000E products. If desired, the extra address lines can be used by specifying the address lines option in bitgen as 22 (bitgen -g AddressLines:22). The lines (A18-A21) are driven when a master device detects, via the bitstream, that it should be using all 22 address lines. Because these pins will initially be pulled high by internal pull-ups, designers using Master Parallel Up mode should use external pull down resistors on pins A18-A21. If Master Parallel Down mode is used external resistors are not necessary.

All 22 address lines are always active in Master Parallel modes with XC4000XL devices. The additional address lines behave identically to the lower order address lines. If the Address Lines option in bitgen is set to 18, it will be ignored by the XC4000XL device.

The additional address lines (A18-A21) are not available in the PC84 package.

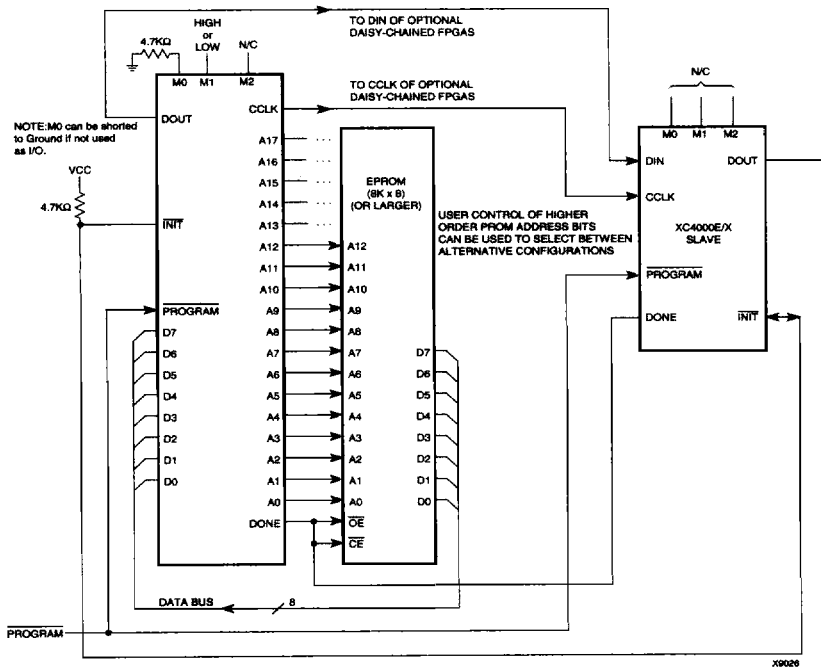
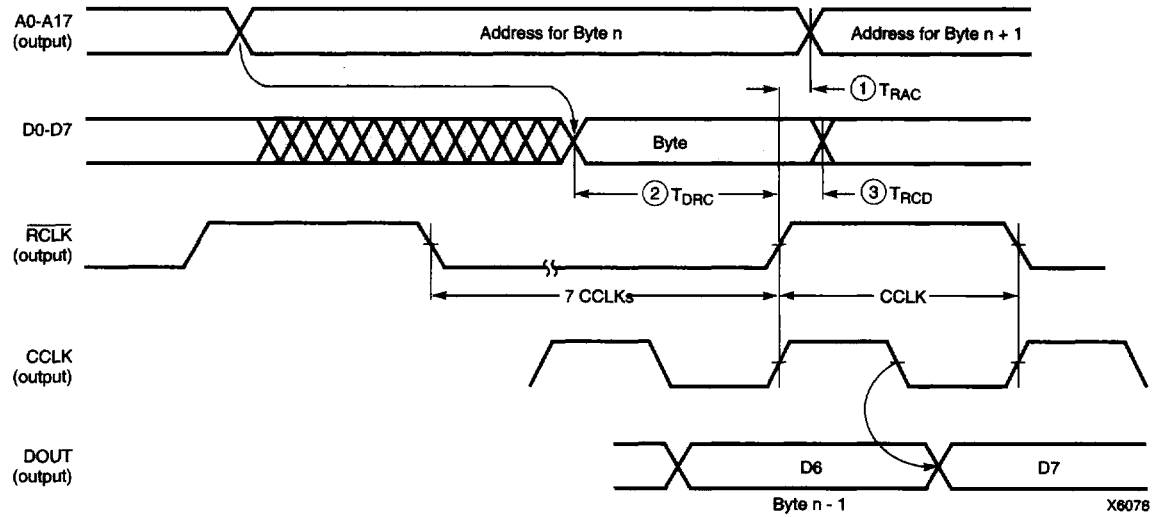


Figure 54: Master Parallel Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
RCLK	Delay to Address valid	1	T_{RAC}	0	200	ns
	Data setup time	2	T_{DRC}	60		ns
	Data hold time	3	T_{RCD}	0		ns

Notes:
1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.
2. The first Data byte is loaded and CCLK starts at the end of the first $\overline{\text{RCLK}}$ active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Figure 55: Master Parallel Mode Programming Switching Characteristics

Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/$\overline{\text{BUSY}}$ output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pullup prior to $\overline{\text{INIT}}$ going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

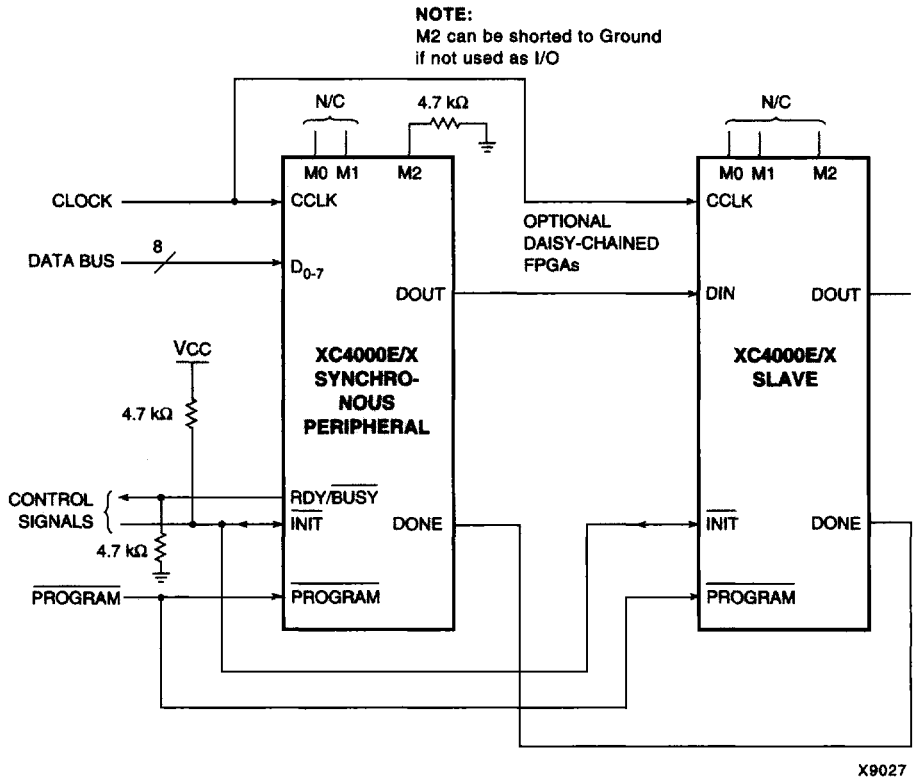
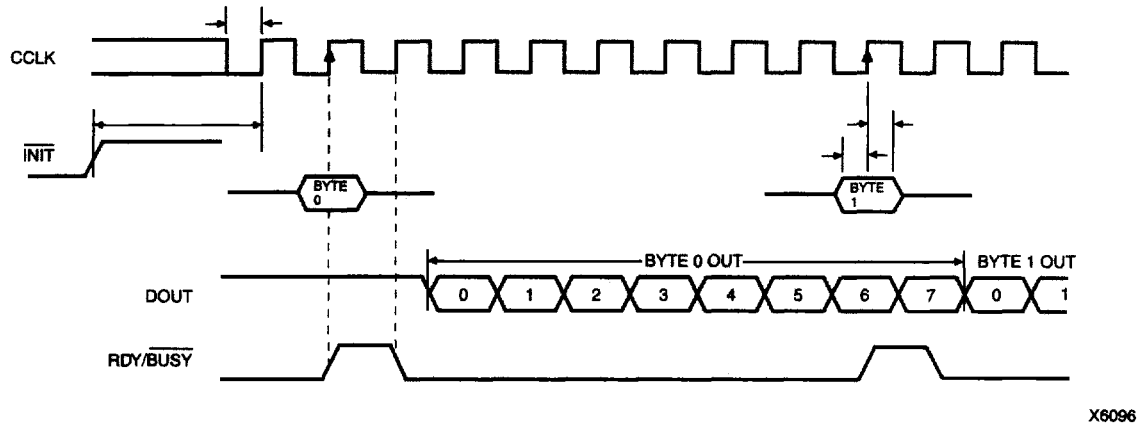


Figure 56: Synchronous Peripheral Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
CCLK	INIT (High) setup time	T_{IC}	5		µs
	D0 - D7 setup time	T_{DC}	60		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	50		ns
	CCLK Low time	T_{CCL}	60		ns
	CCLK Frequency	F_{CC}		8	MHz

Notes:
1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
2. The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
3. The pin name RDY/BUSY is a misnomer. In Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.
4. Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 57: Synchronous Peripheral Mode Programming Switching Characteristics

Asynchronous Peripheral Mode

Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of $\overline{WS}$ and $\overline{CS0}$ being Low and $\overline{RS}$ and CS1 being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its DOUT pin. The RDY/$\overline{BUSY}$ output from the lead FPGA acts as a handshake signal to the microprocessor. RDY/$\overline{BUSY}$ goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the RDY/$\overline{BUSY}$ output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until RDY/$\overline{BUSY}$ is High again for one CCLK period. Note that RDY/$\overline{BUSY}$ is pulled High with a high-impedance pull-up prior to $\overline{INIT}$ going High.

The length of the $\overline{BUSY}$ signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the $\overline{BUSY}$ signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the $\overline{BUSY}$ signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

The READY/$\overline{BUSY}$ handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

Status Read

The logic AND condition of the $\overline{CS0}$, CS1and $\overline{RS}$ inputs puts the device status on the Data bus.

- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in Figure 47 on page 51).

In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by the XACT*step* software, ensures that these problems never occur.

Although RDY/$\overline{BUSY}$ is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/$\overline{BUSY}$ status when $\overline{RS}$ is Low, $\overline{WS}$ is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).

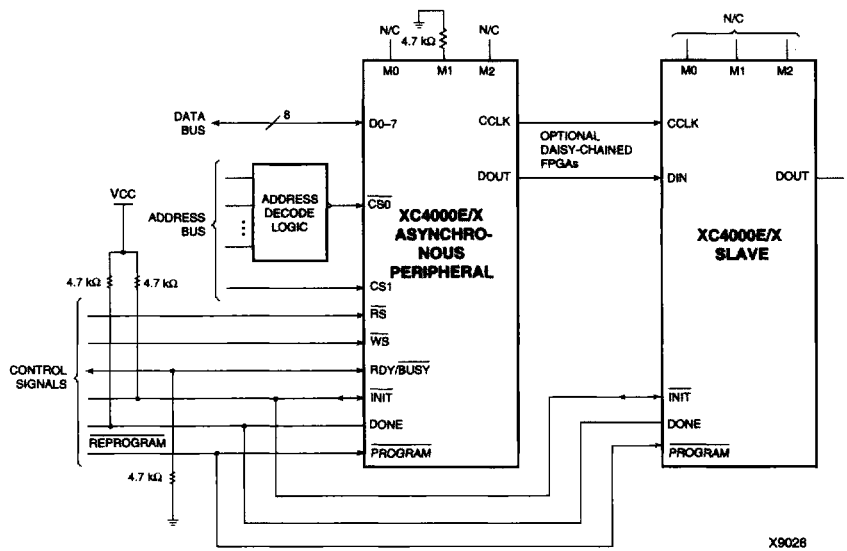
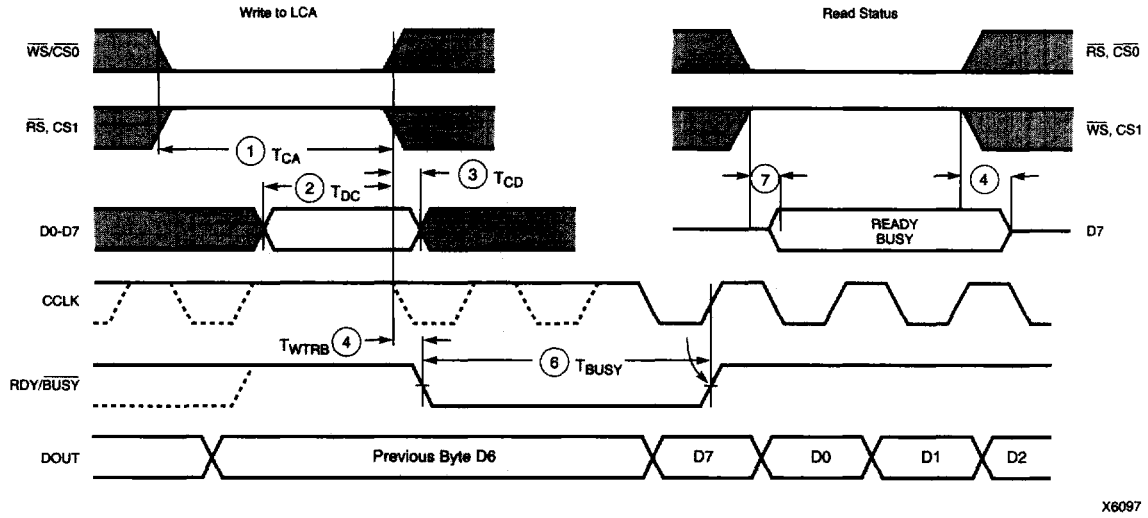


Figure 58: Asynchronous Peripheral Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
Write	Effective Write time ($\overline{CS0}$, $\overline{WS}$=Low; $\overline{RS}$, CS1=High)	1	T_{CA}	100		ns
	DIN setup time	2	T_{DC}	60		ns
	DIN hold time	3	T_{CD}	0		ns
RDY	RDY/$\overline{BUSY}$ delay after end of Write or Read	4	T_{WTRB}		60	ns
	RDY/$\overline{BUSY}$ active after beginning of Read	7			60	ns
	RDY/$\overline{BUSY}$ Low output (Note 4)	6	T_{BUSY}	2	9	CCLK periods

Notes:
1. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.
2. The time from the end of $\overline{WS}$ to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. CCLK and DOUT timing is tested in slave mode.
4. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of $\overline{WS}$. RDY/$\overline{BUSY}$ will go active within 60 ns after the end of $\overline{WS}$. A new write may be asserted immediately after RDY/$\overline{BUSY}$ goes Low, but write may not be terminated until RDY/$\overline{BUSY}$ has been High for one CCLK period.

Figure 59: Asynchronous Peripheral Mode Programming Switching Characteristics

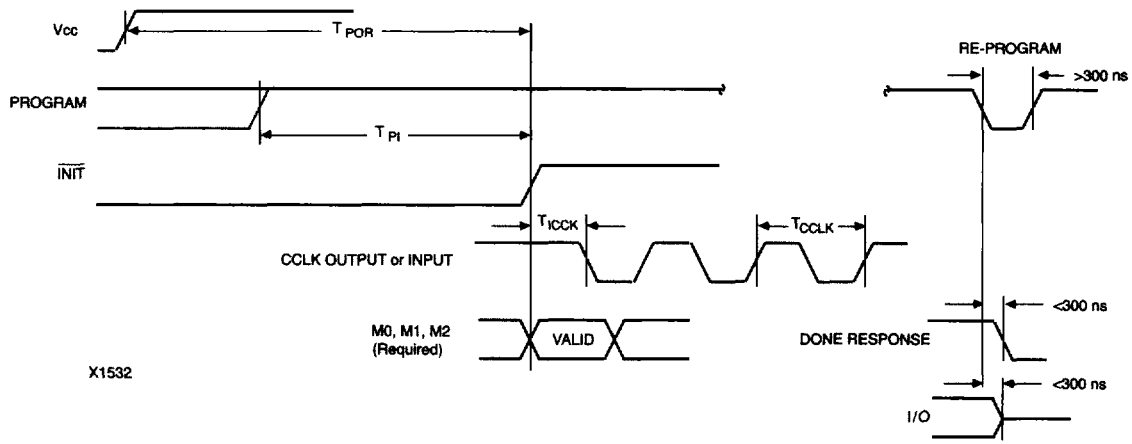
Table 22: Pin Functions During Configuration

CONFIGURATION MODE <M2:M1:M0>						
SLAVE SERIAL <1:1:1>	MASTER SERIAL <0:0:0>	SYNCH. PERIPHERAL <0:1:1>	ASYNCH. PERIPHERAL <1:0:1>	MASTER PARALLEL DOWN <1:1:0>	MASTER PARALLEL UP <1:0:0>	USER OPERATION
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (LOW) (I)	(I)
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	(O)
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	(I)
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
$\overline{LDC}$ (LOW)	$\overline{LDC}$ (LOW)	$\overline{LDC}$ (LOW)	$\overline{LDC}$ (LOW)	$\overline{LDC}$ (LOW)	$\overline{LDC}$ (LOW)	I/O
$\overline{INIT}$	$\overline{INIT}$	$\overline{INIT}$	$\overline{INIT}$	$\overline{INIT}$	$\overline{INIT}$	I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	$\overline{PROGRAM}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)
		RDY/$\overline{BUSY}$ (O)	RDY/$\overline{BUSY}$ (O)	$\overline{RCLK}$ (O)	$\overline{RCLK}$ (O)	I/O
			RS (I)			I/O
			CS0 (I)			I/O
		DATA7 (I)	DATA7 (I)	DATA7 (I)	DATA7 (I)	I/O
		DATA6 (I)	DATA6 (I)	DATA6 (I)	DATA6 (I)	I/O
		DATA5 (I)	DATA5 (I)	DATA5 (I)	DATA5 (I)	I/O
		DATA4 (I)	DATA4 (I)	DATA4 (I)	DATA4 (I)	I/O
		DATA3 (I)	DATA3 (I)	DATA3 (I)	DATA3 (I)	I/O
		DATA2 (I)	DATA2 (I)	DATA2 (I)	DATA2 (I)	I/O
		DATA1 (I)	DATA1 (I)	DATA1 (I)	DATA1 (I)	I/O
DIN (I)	DIN (I)	DATA0 (I)	DATA0 (I)	DATA0 (I)	DATA0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGCK4-GCK5-I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			WS (I)	A0	A0	I/O
				A1	A1	PGCK4-GCK6-I/O
			CS1	A2	A2	I/O
				A3	A3	I/O
				A4	A4	I/O
				A5	A5	I/O
				A6	A6	I/O
				A7	A7	I/O
				A8	A8	I/O
				A9	A9	I/O
				A10	A10	I/O
				A11	A11	I/O
				A12	A12	I/O
				A13	A13	I/O
				A14	A14	I/O
				A15	A15	SGCK1-GCK7-I/O
				A16	A16	PGCK1-GCK8-I/O
				A17	A17	I/O
				A18*	A18*	I/O
				A19*	A19*	I/O
				A20*	A20*	I/O
				A21*	A21*	I/O
						ALL OTHERS

* XC4000X only

Notes 1. A shaded table cell represents a 50 kΩ - 100 kΩ pull-up before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{INIT}$ is an open-drain output during configuration.

Configuration Switching Characteristics



Master Modes (XC4000E/EX)

Description		Symbol	Min	Max	Units
Power-On Reset	M0 = High	T_{POR}	10	40	ms
	M0 = Low	T_{POR}	40	130	ms
Program Latency		T_{PI}	30	200	µs per CLB column
CCLK (output) Delay		T_{ICCK}	40	250	µs
CCLK (output) Period, slow		T_{CCLK}	640	2000	ns
CCLK (output) Period, fast		T_{CCLK}	80	250	ns

Master Modes (XC4000XL)

Description		Symbol	Min	Max	Units
Power-On Reset	M0 = High	T_{POR}	10	40	ms
	M0 = Low	T_{POR}	40	130	ms
Program Latency		T_{PI}	30	200	µs per CLB column
CCLK (output) Delay		T_{ICCK}	40	250	µs
CCLK (output) Period, slow		T_{CCLK}	540	1600	ns
CCLK (output) Period, fast		T_{CCLK}	67	200	ns

Slave and Peripheral Modes(All)

Description	Symbol	Min	Max	Units
Power-On Reset	T_{POR}	10	33	ms
Program Latency	T_{PI}	30	200	µs per CLB column
CCLK (input) Delay (required)	T_{ICCK}	4		µs
CCLK (input) Period (required)	T_{CCLK}	100		ns

XC4000XL Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

XC4000XL Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: 1. Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000XL Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~40% of V_{CC}.

XC4000XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			5	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

XC4000XL Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
From pad through Global Low Skew buffer, to any clock K	T_{GLS}	XC4005XL	2.7	2.3	2.0	ns
		XC4010XL	3.2	2.8	2.4	ns
		XC4013XL	3.6	3.1	2.7	ns
		XC4020XL	4.0	3.5	3.0	ns
		XC4028XL	4.4	3.8	3.3	ns
		XC4036XL	4.8	4.2	3.6	ns
		XC4044XL	5.3	4.6	4.0	ns
		XC4052XL	5.7	5.0	4.3	ns
		XC4062XL	6.3	5.4	4.7	ns
		XC4085XL	7.2	6.2	5.4	ns
From pad through Global Early buffer, to any clock K in same quadrant	T_{GE}	XC4005XL	1.9	1.8	1.7	ns
		XC4010XL	2.2	1.9	1.7	ns
		XC4013XL	2.4	2.1	1.8	ns
		XC4020XL	2.6	2.2	2.1	ns
		XC4028XL	2.8	2.4	2.1	ns
		XC4036XL	3.1	2.7	2.3	ns
		XC4044XL	3.5	3.0	2.6	ns
		XC4052XL	4.0	3.5	3.0	ns
		XC4062XL	4.9	4.3	3.7	ns
		XC4085XL	5.8	5.1	4.7	ns

Note: Parameters are for BUFGE #s 1, 2, 5 and 6. Add 1.4 ns for BUFGE #s 3, 4, 7 and 8.

XC4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and expressed in nanoseconds unless otherwise noted.

	Speed Grade	-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		1.6		1.5		1.3	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		2.7		2.4		2.2	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.9		2.6		2.2	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		2.5		2.2		2.0	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		2.4		2.1		1.9	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		2.5		2.2		2.0	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		1.5		1.3		1.1	ns
CLB Fast Carry Logic								
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		2.7		2.3		2.0	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		3.3		2.9		2.5	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		2.0		1.8		1.5	ns
CIN through function generators to X/Y outputs	T_{SUM}		2.8		2.6		2.4	ns
CIN to COUT, bypass function generators	T_{BYP}		0.3		0.3		0.2	ns
Sequential Delays								
Clock K to Flip-Flop outputs Q	T_{CKO}		2.1		1.9		1.6	ns
Clock K to Latch outputs Q	T_{CKLO}		2.1		1.9		1.6	ns
Setup Time before Clock K								
F/G inputs	T_{ICK}	1.1		1.0		0.9		ns
F/G inputs via H	T_{IHCK}	2.2		1.9		1.7		ns
C inputs via H0 through H	T_{HH0CK}	2.0		1.7		1.6		ns
C inputs via H1 through H	T_{HH1CK}	1.9		1.6		1.4		ns
C inputs via H2 through H	T_{HH2CK}	2.0		1.7		1.6		ns
C inputs via DIN	T_{DICK}	0.9		0.8		0.7		ns
C inputs via EC	T_{ECCK}	1.0		0.9		0.8		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.6		0.5		0.5		ns
CIN input via F/G	T_{CCK}	2.3		2.1		1.9		ns
CIN input via F/G and H	T_{CHCK}	3.4		3.0		2.7		ns
Hold Time after Clock K								
F/G inputs	T_{CKI}	0		0		0		ns
F/G inputs via H	T_{CKIH}	0		0		0		ns
C inputs via SR/H0 through H	T_{CKHH0}	0		0		0		ns
C inputs via H1 through H	T_{CKHH1}	0		0		0		ns
C inputs via DIN/H2 through H	T_{CKHH2}	0		0		0		ns
C inputs via DIN/H2	T_{CKDI}	0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		ns
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0		ns
Clock								
Clock High time	T_{CH}	3.0		2.8		2.5		ns
Clock Low time	T_{CL}	3.0		2.8		2.5		ns
Set/Reset Direct								
Width (High)	T_{RPW}	3.0		2.8		2.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		3.7		3.2		2.8	ns
Global Set/Reset								
Minimum GSR Pulse Width	T_{MRW}		19.8		17.3		15.0	ns
Delay from GSR input to any Q Note 1	T_{MRQ}							
Toggle Frequency (MHz) (Note 2)	F_{TOG}		166		179		200	MHz

Note 1: For values per device, see Globals Set/Reset entries on page 4-82.
Note 2: Maximum flip-flop toggle rate for export control purposes.

XC4000XL CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

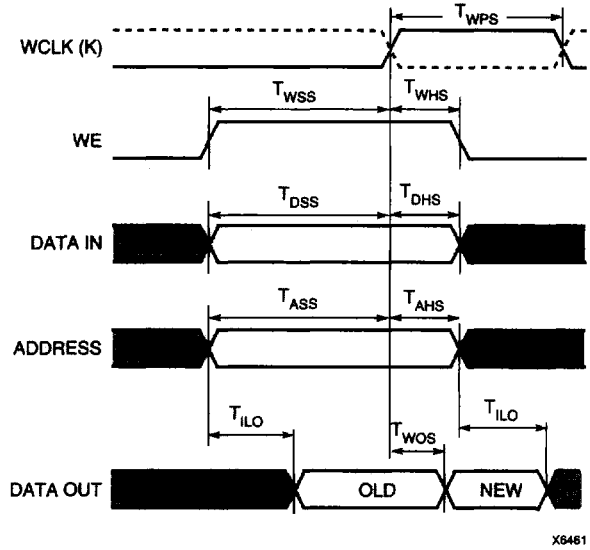
Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	Speed Grade		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x2	T_{WCS}	9.0		8.4		7.7		ns
	32x1	T_{WCTS}	9.0		8.4		7.7		ns
Clock K pulse width (active edge)	16x2	T_{WPS}	4.5		4.2		3.9		ns
	32x1	T_{WPTS}	4.5		4.2		3.9		ns
Address setup time before clock K	16x2	T_{ASS}	2.2		2.0		1.7		ns
	32x1	T_{ASTS}	2.2		2.0		1.7		ns
Address hold time after clock K	16x2	T_{AHS}	0		0		0		ns
	32x1	T_{AHTS}	0		0		0		ns
DIN setup time before clock K	16x2	T_{DSS}	2.0		1.9		1.7		ns
	32x1	T_{DSTS}	2.5		2.3		2.1		ns
DIN hold time after clock K	16x2	T_{DHS}	0		0		0		ns
	32x1	T_{DHTS}	0		0		0		ns
WE setup time before clock K	16x2	T_{WSS}	2.0		1.8		1.6		ns
	32x1	T_{WSTS}	1.8		1.7		1.5		ns
WE hold time after clock K	16x2	T_{WHS}	0		0		0		ns
	32x1	T_{WHTS}	0		0		0		ns
Data valid after clock K	16x2	T_{WOS}		6.8		6.3		5.8	ns
	32x1	T_{WOTS}		8.1		7.5		6.9	ns

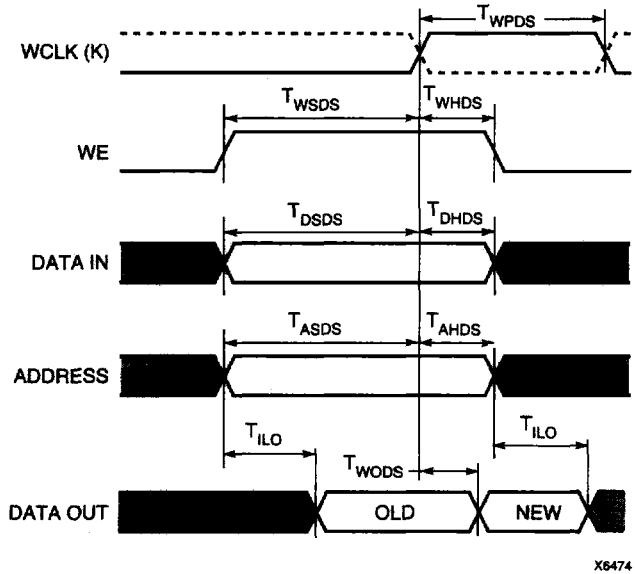
Dual Port RAM	Speed Grade		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x1	T_{WCDS}	9.0		8.4		7.7		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	4.5		4.2		3.9		ns
Address setup time before clock K	16x1	T_{ASDS}	2.5		2.0		1.7		ns
Address hold time after clock K	16x1	T_{AHDS}	0		0		0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.5		2.3		2.0		ns
DIN hold time after clock K	16x1	T_{DHDS}	0		0		0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.8		1.7		1.6		ns
WE hold time after clock K	16x1	T_{WHDS}	0		0		0		ns
Data valid after clock K	16x1	T_{WODS}		7.8		7.3		6.7	ns

Notes: Timing for the 16 x1 RAM option is identical to 16 x 2 RAM timing.Applicable Read timing specifications are identical to Asynchronous (Level Sensitive) Read timing.

XC4000XL CLB RAM Synchronous (Edge-Triggered) Write Timing



XC4000XL CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing

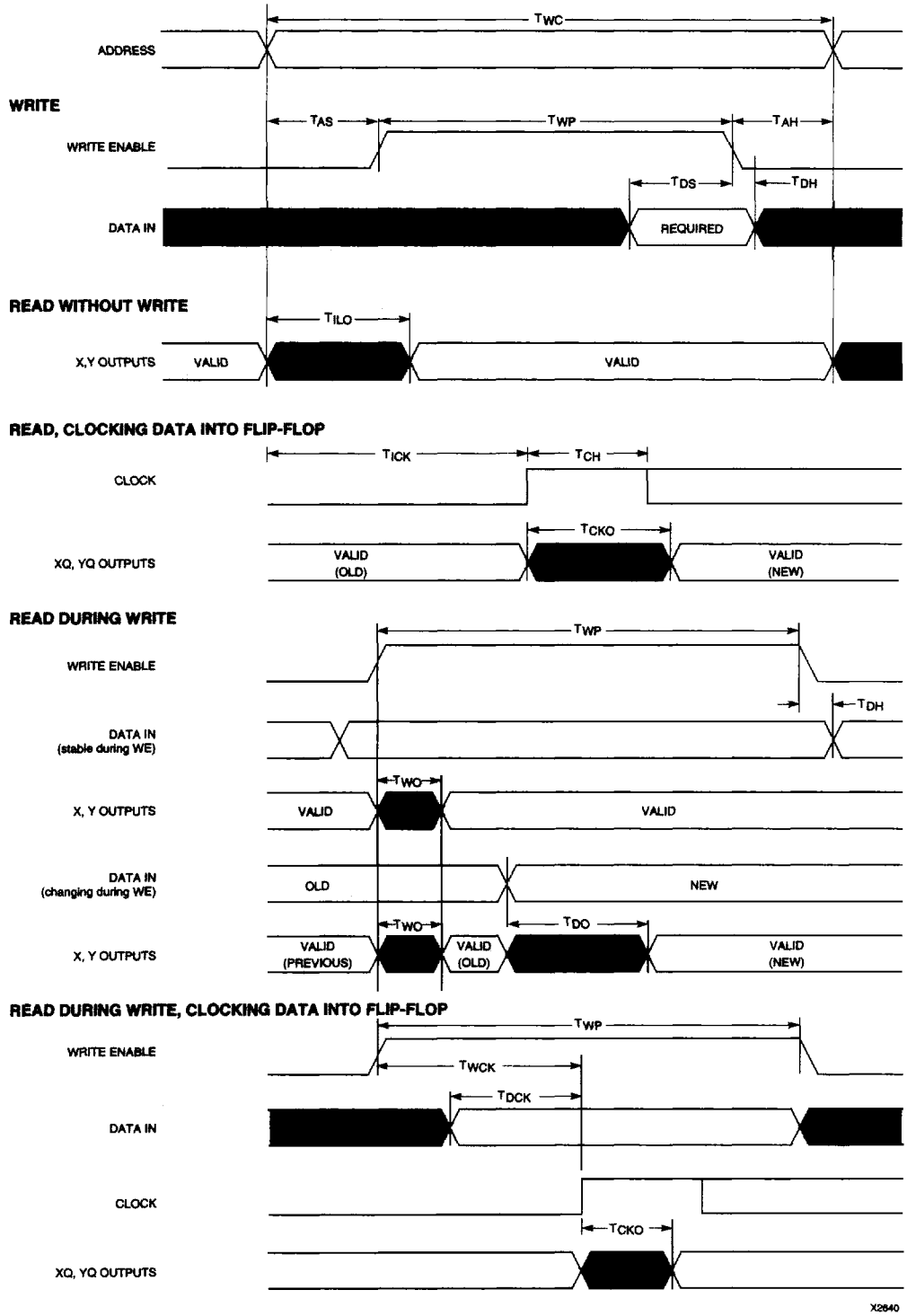


XC4000XL CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted. Synchronous RAM is recommended for new designs.

		Speed Grade	-3		-2		-1		Units
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Operation									
Address write cycle time	16x2 32x1	T_{WC} T_{WCT}	10.6 10.6		9.2 9.2		8.0 8.0		ns ns
Write Enable pulse width (High)	16x2 32x1	T_{WP} T_{WPT}	5.3 5.3		4.6 4.6		4.0 4.0		ns ns
Address setup time before WE	16x2 32x1	T_{AS} T_{AST}	2.7 2.9		2.3 2.5		2.0 2.2		ns ns
Address hold time after end of WE	16x2 32x1	T_{AH} T_{AHT}	2.7 2.7		2.3 2.3		2.0 2.0		ns ns
DIN setup time before end of WE	16x2 32x1	T_{DS} T_{DST}	1.1 1.1		0.9 0.9		0.8 0.8		ns ns
DIN hold time after end of WE	16x2 32x1	T_{DH} T_{DHT}	9.4 9.4		8.1 8.1		6.9 6.9		ns ns
Read Operation									
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	4.5 6.5		3.1 5.5		2.6 3.8		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		1.6 2.7		1.5 2.4		1.3 2.2	ns ns
Read Operation, Clocking Data into Flip-Flop									
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	1.3 2.3		1.1 2.0		1.0 1.8		ns ns
Read During Write									
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	T_{WO} T_{WOT}		6.8 7.9		5.9 6.9		5.2 6.1	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	T_{DO} T_{DOT}		7.7 8.6		6.7 7.5		5.9 6.6	ns ns
Read During Write, Clocking Data into Flip-Flop									
WE setup time before clock K	16x2 32x1	T_{WCK} T_{WCKT}	7.3 9.3		6.4 8.1		5.5 7.0		ns ns
Data setup time before clock K	16x2 32x1	T_{DCK} T_{DCKT}	6.4 8.6		5.6 7.5		4.8 6.5		ns ns

XC4000XL CLB RAM Asynchronous (Level-Sensitive) Timing Characteristics



XC4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

XC4000XL Output Flip-Flop, Clock to Out

		Speed Grade	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	
Global Low Skew Clock to Output using OFF	T_{ICKOF}	XC4005XL	7.7	6.7	5.8	ns
		XC4010XL	8.3	7.2	6.2	ns
		XC4013XL	8.6	7.5	6.5	ns
		XC4020XL	9.0	7.9	6.8	ns
		XC4028XL	9.4	8.2	7.1	ns
		XC4036XL	9.8	8.5	7.4	ns
		XC4044XL	10.3	9.0	7.8	ns
		XC4052XL	10.7	9.4	8.1	ns
		XC4062XL	11.3	9.8	8.5	ns
		XC4085XL	12.2	10.6	9.2	ns
Global Early Clock to Output using OFF Values are for BUFGE #s 1, 2, 5 and 6. Add 1.4 ns for BUFGE #s 3, 4, 7 and 8.	T_{ICKEOF}	XC4005XL	6.9	6.2	5.5	ns
		XC4010XL	7.2	6.3	5.5	ns
		XC4013XL	7.4	6.5	5.6	ns
		XC4020XL	7.6	6.6	5.9	ns
		XC4028XL	7.8	6.8	5.9	ns
		XC4036XL	8.1	7.0	6.1	ns
		XC4044XL	8.5	7.4	6.4	ns
		XC4052XL	9.0	7.9	6.8	ns
		XC4062XL	9.9	8.6	7.5	ns
		XC4085XL	10.8	9.4	8.5	ns
For output SLOW option add	T_{SLOW}	All Devices	3.0	2.5	2.0	ns

OFF = Output Flip Flop

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 35 pF external capacitive load.

XC4000XL Output MUX, Clock to Out

Description	Symbol	Speed Grade / Device	-3 Max	-2 Max	-1 Max	Units
Global Low Skew Clock to Output using OMUX	T_{PFPF}	XC4005XL	7.8	6.8	5.9	ns
		XC4010XL	8.4	7.3	6.3	ns
		XC4013XL	8.8	7.6	6.6	ns
		XC4020XL	9.2	8.0	6.9	ns
		XC4028XL	9.6	8.3	7.2	ns
		XC4036XL	10.0	8.7	7.5	ns
		XC4044XL	10.5	9.1	7.9	ns
		XC4052XL	10.9	9.5	8.2	ns
		XC4062XL	11.4	9.9	8.6	ns
		XC4085XL	12.3	10.7	9.3	ns
Global Early Clock to Output using OMUX Values are for BUFGE #s 1, 2, 5 and 6. Add 1.4 ns for BUFGE #s 3, 4, 7 and 8.	T_{PEFPF}	XC4005XL	7.1	6.3	5.6	ns
		XC4010XL	7.3	6.4	5.6	ns
		XC4013XL	7.6	6.6	5.7	ns
		XC4020XL	7.7	6.7	6.0	ns
		XC4028XL	8.0	6.9	6.0	ns
		XC4036XL	8.2	7.2	6.2	ns
		XC4044XL	8.6	7.5	6.5	ns
		XC4052XL	9.2	8.0	6.9	ns
		XC4062XL	10.0	8.8	7.6	ns
		XC4085XL	11.0	9.6	8.6	ns
For output SLOW option add	T_{SLOW}	All Devices	3.0	2.5	2.0	ns

OMUX = Output MUX

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 35 pF external capacitive load.

XC4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

XC4000XL Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-3	-2	-1	Units
Description	Symbol	Device	Min	Min	Min	
Input Setup Time, using Global Low Skew clock and IFF (full delay)	T_{PSD}	XC4005XL	8.8	7.6	6.6	ns
		XC4010XL	9.0	7.8	6.8	ns
		XC4013XL	6.4	6.0	5.6	ns
		XC4020XL	8.8	7.6	6.6	ns
		XC4028XL	9.8	8.5	7.4	ns
		XC4036XL	6.6	6.2	5.8	ns
		XC4044XL	10.6	9.2	8.0	ns
		XC4052XL	11.2	9.7	8.4	ns
		XC4062XL	6.8	6.4	6.0	ns
		XC4085XL	12.7	11.0	9.6	ns
Input Hold Time, using Global Low Skew clock and IFF (full delay)	T_{PHD}	XC4005XL	0	0	0	ns
		XC4010XL	0	0	0	ns
		XC4013XL	0	0	0	ns
		XC4020XL	0	0	0	ns
		XC4028XL	0	0	0	ns
		XC4036XL	0	0	0	ns
		XC4044XL	0	0	0	ns
		XC4052XL	0	0	0	ns
		XC4062XL	0	0	0	ns
		XC4085XL	0	0	0	ns

IFF = Input Flip-Flop or Latch

Note: Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

XC4000XL BUFGE #s 3, 4, 7, and 8 Global Early Clock, Set-Up and Hold for IFF and FCL

Description	Symbol	Speed Grade / Device	-3 Min	-2 Min	-1 Min	Units
Input Setup Time		XC4005XL	8.4	7.9	7.4	ns
Global Early clock and IFF (partial delay)	T_{PSEP}	XC4010XL	10.3	9.0	7.8	ns
Global Early clock and FCL (partial delay)	T_{PFSEP}	XC4013XL	5.4	4.9	4.4	ns
		XC4020XL	9.8	9.3	8.8	ns
		XC4028XL	12.7	11.0	9.6	ns
		XC4036XL	6.4	5.9	5.4	ns
		XC4044XL	13.8	12.0	10.4	ns
		XC4052XL	14.5	12.7	11.0	ns
		XC4062XL	8.4	7.9	7.4	ns
		XC4085XL	14.5	12.7	11.0	ns
Input Hold Time		XC4005XL	0	0	0	ns
Global Early clock and IFF (partial delay)	T_{PHEP}	XC4010XL	0	0	0	ns
Global Early clock and FCL (partial delay)	T_{PFHEP}	XC4013XL	0	0	0	ns
		XC4020XL	0	0	0	ns
		XC4028XL	0	0	0	ns
		XC4036XL	0.8	0.8	0.8	ns
		XC4044XL	0	0	0	ns
		XC4052XL	0	0	0	ns
		XC4062XL	1.5	1.5	1.5	ns
		XC4085XL	0	0	0	ns

IFF = Input Flip-Flop or Latch

XC4000XL BUFGE #s 1, 2, 5, and 6 Global Early Clock, Set-Up and Hold for IFF and FCL

Description	Symbol	Speed Grade / Device	-3 Min	-2 Min	-1 Min	Units
Input Setup Time		XC4005XL	9.0	8.5	8.0	ns
Global Early clock and IFF (partial delay)	T_{PSEP}	XC4010XL	11.9	10.4	9.0	ns
Global Early clock and FCL (partial delay)	T_{PFSEP}	XC4013XL	6.4	5.9	5.4	ns
		XC4020XL	10.8	10.3	9.8	ns
		XC4028XL	14.0	12.2	10.6	ns
		XC4036XL	7.0	6.6	6.2	ns
		XC4044XL	14.6	12.7	11.0	ns
		XC4052XL	16.4	14.3	12.4	ns
		XC4062XL	9.0	8.6	8.2	ns
		XC4085XL	16.7	14.5	12.6	ns
Input Hold Time		XC4005XL	0	0	0	ns
Global Early clock and IFF (partial delay)	T_{PHEP}	XC4010XL	0	0	0	ns
Global Early clock and FCL (partial delay)	T_{PFHEP}	XC4013XL	0	0	0	ns
		XC4020XL	0	0	0	ns
		XC4028XL	0	0	0	ns
		XC4036XL	0	0	0	ns
		XC4044XL	0	0	0	ns
		XC4052XL	0	0	0	ns
		XC4062XL	0.8	0.8	0.8	ns
		XC4085XL	0	0	0	ns

FCL = Fast Capture Latch

Notes: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

XC4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Description	Symbol	Speed Grade / Device	-3 Min	-2 Min	-1 Min	Units
Clocks						
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All devices	1.7	1.5	1.3	ns
Propagation Delays			**Max**	**Max**	**Max**	
Pad to I1, I2	T_{PID}	All devices	1.6	1.4	1.2	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices	2.6	2.2	1.9	ns
Pad to I1, I2 via transparent input latch, partial delay	T_{PPLI}	XC4005XL	13.7	11.9	10.4	ns
		XC4010XL	9.3	8.1	7.0	ns
		XC4013XL	9.2	8.0	7.0	ns
		XC4020XL	16.9	14.7	12.8	ns
		XC4028XL	17.0	14.8	12.9	ns
		XC4036XL	9.8	8.6	7.4	ns
		XC4044XL	16.9	14.7	12.8	ns
		XC4052XL	17.8	15.5	13.5	ns
		XC4062XL	10.2	9.0	8.4	ns
		XC4085XL	20.2	17.5	15.3	ns
Pad to I1, I2 via transparent input latch, full delay	T_{PDLI}	XC4005XL	11.0	9.6	8.4	ns
		XC4010XL	10.8	9.4	8.2	ns
		XC4013XL	11.0	9.6	8.4	ns
		XC4020XL	14.9	12.9	11.3	ns
		XC4028XL	14.0	12.2	10.6	ns
		XC4036XL	11.9	10.4	9.0	ns
		XC4044XL	14.1	12.3	10.7	ns
		XC4052XL	14.3	12.5	10.9	ns
		XC4062XL	12.7	11.0	10.3	ns
		XC4085XL	19.6	17.1	14.9	ns

FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch

XC4000XL IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
Propagation Delays						
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All devices	3.1	2.7	2.4	ns
Pad to I1, I2 via transparent FCL and input latch, partial delay	T_{PPFLI}	XC4005XL	13.7	11.9	10.4	ns
		XC4010XL	9.3	8.1	7.0	ns
		XC4013XL	9.2	8.0	7.0	ns
		XC4020XL	17.0	14.8	12.9	ns
		XC4028XL	16.5	14.3	12.5	ns
		XC4036XL	9.8	8.6	7.4	ns
		XC4044XL	16.9	14.7	12.8	ns
		XC4052XL	17.8	15.5	13.5	ns
		XC4062XL	10.2	8.9	8.4	ns
		XC4085XL	20.2	17.5	15.3	ns
Propagation Delays						
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices	1.8	1.5	1.3	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices	1.9	1.7	1.4	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All devices	3.6	3.1	2.7	ns
Global Set/Reset						
Minimum GSR Pulse Width	T_{MRW}	All devices	19.8	17.3	15.0	ns
Delay from GSR input to any Q	T_{RRI}	XC4005XL	11.3	9.8	8.5	ns
		XC4010XL	13.9	12.1	10.5	ns
		XC4013XL	15.9	13.8	12.0	ns
		XC4020XL	18.6	16.1	14.0	ns
		XC4028XL	20.5	17.9	15.5	ns
		XC4036XL	22.5	19.6	17.0	ns
		XC4044XL	25.1	21.9	19.0	ns
		XC4052XL	27.2	23.6	20.5	ns
		XC4062XL	29.1	25.3	22.0	ns
		XC4085XL	34.4	29.9	26.0	ns

FCL = Fast Capture Latch

XC4000XL IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Description	Symbol	Device	-3 Min	-2 Min	-1 Min	Units
Setup Times						
Pad to Clock (IK), no delay	T_{PICK}	All devices	1.7	1.5	1.3	ns
Pad to Clock (IK), partial delay	T_{PICKP}	XC4005XL	12.3	13.1	9.3	ns
		XC4010XL	7.9	6.9	6.0	ns
		XC4013XL	7.8	6.9	5.9	ns
		XC4020XL	7.8	13.5	11.7	ns
		XC4028XL	15.6	13.6	11.8	ns
		XC4036XL	8.4	7.3	6.3	ns
		XC4044XL	15.5	13.5	11.8	ns
		XC4052XL	16.4	14.3	12.4	ns
		XC4062XL	8.9	7.7	7.3	ns
		XC4085XL	18.8	16.3	14.2	ns
Pad to Clock (IK), full delay	T_{PICKD}	XC4005XL	9.7	8.4	7.3	ns
		XC4010XL	9.4	8.2	7.1	ns
		XC4013XL	9.7	8.4	7.3	ns
		XC4020XL	13.5	11.7	10.2	ns
		XC4028XL	12.6	10.9	9.5	ns
		XC4036XL	10.5	9.1	7.9	ns
		XC4044XL	12.7	11.0	9.6	ns
		XC4052XL	12.9	11.3	9.8	ns
		XC4062XL	11.3	9.8	9.2	ns
		XC4085XL	18.2	15.9	13.8	ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	All devices	2.4	2.1	1.8	ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	T_{PICKFP}	XC4005XL	12.9	11.2	9.8	ns
		XC4010XL	8.5	7.4	6.4	ns
		XC4013XL	8.4	7.3	6.4	ns
		XC4020XL	16.1	14.0	12.2	ns
		XC4028XL	16.3	14.2	12.3	ns
		XC4036XL	9.0	7.9	6.8	ns
		XC4044XL	16.2	14.1	12.2	ns
		XC4052XL	17.0	14.8	12.9	ns
		XC4062XL	9.6	8.3	7.8	ns
		XC4085XL	19.4	16.8	14.7	ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All devices	0.7	0.6	0.5	ns
Setup Times						
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All devices	0.3	0.2	0.2	ns
Hold Times						
All Hold Times		All devices	0	0	0	ns

Note: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on pages 4-79 and 4-80.

XC4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

Description	Speed Grade / Symbol	-3 Min	-3 Max	-2 Min	-2 Max	-1 Min	-1 Max	Units
Propagation Delays								
Clock (OK) to Pad	T_{OKPOF}		5.0		4.4		3.8	ns
Output (O) to Pad	T_{OPF}		4.1		3.6		3.1	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		4.4		3.8		3.3	ns
3-state to Pad active and valid	T_{TSONF}		4.1		3.6		3.1	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}		5.5		4.8		4.2	ns
Setup and Hold Times								
Output (O) to clock (OK) setup time	T_{OOK}	0.5		0.4		0.3		ns
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0		ns
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	0		0		0		ns
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	0.3		0.2		0.1		ns
Clock								
Clock High	T_{CH}	3.0		2.8		2.5		ns
Clock Low	T_{CL}	3.0		2.8		2.5		ns
Global Set/Reset								
Minimum GSR pulse width	T_{MRW}		19.8		17.3		15.0	ns
Delay from GSR input to any Pad	T_{RPO}							
XC4005XL		15.9		13.8		12.0		ns
XC4010XL		18.5		16.1		14.0		ns
XC4013XL		20.5		17.8		15.5		ns
XC4020XL		23.2		20.1		17.5		ns
XC4028XL		25.1		21.9		19.0		ns
XC4036XL		27.1		23.6		20.5		ns
XC4044XL		29.7		25.9		22.5		ns
XC4052XL		31.7		27.6		24.0		ns
XC4062XL		33.7		29.3		25.5		ns
XC4085XL		39.0		33.9		29.5		ns
Slew Rate Adjustment								
For output SLOW option add	T_{SLOW}		3.0		2.5		2.0	ns

Note : Output timing is measured at ~50% V_{CC} threshold, with 35 pF external capacitive loads.
Note 2: For PCI applications, based on a 50 pF external capacitive load, add 400 ps to the propagation delay values.

XC4000XL Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
TBUF driving a Horizontal Longline						
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{IO1}	XC4005XL	4.9	4.3	3.7	ns
		XC4010XL	6.8	5.9	5.1	ns
		XC4013XL	7.7	6.7	5.8	ns
		XC4020XL	8.7	7.6	6.6	ns
		XC4028XL	9.8	8.5	7.4	ns
		XC4036XL	11.6	10.1	8.8	ns
		XC4044XL	12.3	10.7	9.3	ns
		XC4052XL	13.6	11.8	10.3	ns
		XC4062XL	14.9	13.0	11.3	ns
		XC4085XL	18.0	15.6	13.6	ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{ON}	XC4005XL	5.6	4.9	4.2	ns
		XC4010XL	7.4	6.5	5.6	ns
		XC4013XL	8.4	7.3	6.3	ns
		XC4020XL	9.4	8.2	7.1	ns
		XC4028XL	10.5	9.1	7.9	ns
		XC4036XL	12.3	10.7	9.3	ns
		XC4044XL	13.0	11.3	9.8	ns
		XC4052XL	14.3	12.5	10.8	ns
		XC4062XL	15.6	13.6	11.8	ns
		XC4085XL	18.6	16.3	14.1	ns
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. (Note 1)	T_{PU2}	XC4005XL	6.6	5.8	5.0	ns
		XC4010XL	10.5	9.1	7.9	ns
		XC4013XL	7.9	6.9	6.0	ns
		XC4020XL	9.0	7.8	6.8	ns
		XC4028XL	14.6	12.7	11.1	ns
		XC4036XL	14.4	12.5	10.9	ns
		XC4044XL	17.4	15.1	13.2	ns
		XC4052XL	18.8	16.3	14.2	ns
		XC4062XL	17.9	15.6	13.5	ns
		XC4085XL	22.9	19.9	17.3	ns
			Preliminary			

Note 1: These values are for a minimum load with the driver paced as far as possible from the active pullup(s). Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XC4000XL Horizontal Longline Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
TBUF driving half a Horizontal Longline						
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{HIO1}	XC4005XL	3.2	2.8	2.4	ns
		XC4010XL	3.6	3.1	2.7	ns
		XC4013XL	3.8	3.3	2.9	ns
		XC4020XL	4.1	3.6	3.1	ns
		XC4028XL	4.4	3.8	3.3	ns
		XC4036XL	4.8	4.2	3.6	ns
		XC4044XL	5.0	4.4	3.8	ns
		XC4052XL	5.3	4.6	4.0	ns
		XC4062XL	5.6	4.9	4.2	ns
		XC4085XL	6.3	5.5	4.8	ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{HON}	XC4005XL	3.8	3.3	2.9	ns
		XC4010XL	4.2	3.7	3.2	ns
		XC4013XL	4.5	3.9	3.4	ns
		XC4020XL	4.8	4.2	3.6	ns
		XC4028XL	5.0	4.4	3.8	ns
		XC4036XL	5.4	4.7	4.1	ns
		XC4044XL	5.7	5.0	4.3	ns
		XC4052XL	6.0	5.2	4.5	ns
		XC4062XL	6.2	5.4	4.7	ns
		XC4085XL	7.0	6.1	5.3	ns
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. (Note 1)	T_{HPU4}	XC4005XL	4.1	3.6	3.1	ns
		XC4010XL	5.2	4.5	3.9	ns
		XC4013XL	4.3	3.7	3.2	ns
		XC4020XL	4.8	4.1	3.6	ns
		XC4028XL	6.6	5.8	5.0	ns
		XC4036XL	5.3	4.6	4.0	ns
		XC4044XL	7.6	6.6	5.8	ns
		XC4052XL	8.1	7.0	6.1	ns
		XC4062XL	6.5	5.7	4.9	ns
		XC4085XL	9.5	8.3	7.2	ns

Note: These values include a minimum load of one output, spaced as far as possible from the active pullup(s). Use the static timing analyzer to determine the delay for each destination.

Note 1: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XC4000XL Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
Full length, two pull-ups, inputs from IOB I-pins	T_{WAF2}	XC4005XL	7.0	6.1	5.3	ns
		XC4010XL	10.6	9.2	8.0	ns
		XC4013XL	9.1	7.9	6.9	ns
		XC4020XL	8.7	7.6	6.6	ns
		XC4028XL	14.0	12.2	10.6	ns
		XC4036XL	11.6	10.1	8.8	ns
		XC4044XL	16.3	14.2	12.3	ns
		XC4052XL	17.4	15.2	13.2	ns
		XC4062XL	19.6	17.1	14.8	ns
		XC4085XL	21.5	18.7	16.3	ns
Half length, two pull-ups, inputs from IOB I-pins	T_{WAO2}	XC4005XL	5.4	4.7	4.1	ns
		XC4010XL	7.3	6.4	5.5	ns
		XC4013XL	6.5	5.7	4.9	ns
		XC4020XL	6.2	5.4	4.7	ns
		XC4028XL	9.0	7.9	6.8	ns
		XC4036XL	8.0	6.9	6.0	ns
		XC4044XL	10.2	8.8	7.7	ns
		XC4052XL	10.7	9.3	8.1	ns
		XC4062XL	11.7	10.2	8.8	ns
		XC4085XL	12.5	10.8	9.4	ns
			Preliminary			

Notes: These delays are specified from the decoder input to the decoder output.
Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XC4000EX Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

XC4000EX Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 4 V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: 1. Maximum DC overshoot or undershoot

above V_{cc} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000EX Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V.
All timing parameters are specified for Commercial temperature range only.

XC4000EX DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0 mA	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		3.0		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			25	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 5.5 V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND.

XC4000EX Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	
From pad through Global Low Skew buffer, to any clock K	T_{GLS}	XC4028EX	9.2	7.5	6.4		ns
		XC4036EX	9.8	7.9	7.1		ns
From pad through Global Early buffer, to any clock K in same quadrant	T_{GE}	XC4028EX	5.7	4.4	4.2		ns
		XC4036EX	5.9	4.6	4.4		ns

XC4000EX Longline and Wide Decoder Timing Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted. Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XC4000EX Horizontal Longline Switching Characteristic Guidelines

		Speed Grade	-4	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	
TBUF driving a Horizontal Longline							
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{IO1}	XC4028EX XC4036EX	13.7 16.5	11.3 13.6	10.9 13.2		ns ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{ON}	XC4028EX XC4036EX	14.7 17.4	12.1 14.4	11.7 14.0		ns ns
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. (Note 1)	T_{PU2}	XC4028EX XC4036EX					ns ns
TBUF driving Half a Horizontal Longline							
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T_{HIO1}	XC4028EX XC4036EX	6.3 7.3	5.6 6.0	4.6 5.7		ns ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T_{HON}	XC4028EX XC4036EX	7.2 8.2	6.4 6.8	5.4 6.5		ns ns
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. (Note 1)	T_{HPU4}	XC4028EX XC4036EX					ns ns

Note: These values include a minimum load of one output, spaced as far as possible from the activated pullup(s). Use the static timing analyzer to determine the delay for each destination.

XC4000EX Wide Decoder Switching Characteristic Guidelines

		Speed Grade	-4	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	
Full length, two pull-ups, inputs from IOB I-pins	T_{WAF2}	XC4028EX XC4036EX					ns ns
Full length, two pull-ups, inputs from internal logic	T_{WAF2L}	XC4028EX XC4036EX					ns ns
Half length, two pull-ups, inputs from IOB I-pins	T_{WAO2}	XC4028EX XC4036EX					ns ns
Half length, two pull-ups, inputs from internal logic	T_{WAO2L}	XC4028EX XC4036EX					ns ns

Notes: These delays are specified from the decoder input to the decoder output.

XC4000EX CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

	Speed Grade	-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays										
F/G inputs to X/Y outputs	T_{ILO}		2.2		1.8		1.5			ns
F/G inputs via H' to X/Y outputs	T_{IHO}		3.8		3.2		2.7			ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		3.2		2.7		2.5			ns
C inputs via SR/H0 via H' to X/Y outputs	T_{HH0O}		3.6		3.0		2.5			ns
C inputs via H1 via H' to X/Y outputs	T_{HH1O}		3.0		2.5		2.3			ns
C inputs via DIN/H2 via H' to X/Y outputs	T_{HH2O}		3.6		3.0		2.5			ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		2.0		1.6		1.4			ns
CLB Fast Carry Logic										
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		4.7		3.9		3.0			ns
Add/Subtract input (F3) to COUT	T_{ASCY}		4.5		3.7		3.7			ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		*3.0*		*2.5*		*2.5*			ns
CIN through function generators to X/Y outputs	T_{SUM}		4.7		3.9		3.0			ns
CIN to COUT, bypass function generators	T_{BYP}		0.5		0.4		0.1			ns
Sequential Delays										
Clock K to Flip-Flop outputs Q	T_{CKO}		2.2		1.9		1.7			ns
Clock K to Latch outputs Q	T_{CKLO}		2.2		1.9		1.7			ns
Setup Time before Clock K										
F/G inputs	T_{ICK}	1.3		1.1		1.1				ns
F/G inputs via H'	T_{IHCK}	3.0		2.5		2.2				ns
C inputs via H0 through H'	T_{HH0CK}	2.8		2.3		2.0				ns
C inputs via H1 through H'	T_{HH1CK}	2.2		1.8		1.8				ns
C inputs via H2 through H'	T_{HH2CK}	2.8		2.3		2.0				ns
C inputs via DIN	T_{DICK}	1.2		0.9		0.9				ns
C inputs via EC	T_{ECCK}	1.2		1.0		0.9				ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.8		0.7		0.6				ns
CIN input via F'/G'	T_{CCK}	2.2		1.8		2.1				ns
CIN input via F'/G' and H'	T_{CHCK}	3.9		3.2		3.2				ns
Hold Time after Clock K										
F/G inputs	T_{CKI}	0		0		0				ns
F/G inputs via H'	T_{CKIH}	0		0		0				ns
C inputs via SR/H0 through H'	T_{CKHH0}	0		0		0				ns
C inputs via H1 through H'	T_{CKHH1}	0		0		0				ns
C inputs via DIN/H2 through H'	T_{CKHH2}	0		0		0				ns
C inputs via DIN/H2	T_{CKDI}	0		0		0				ns
C inputs via EC	T_{CKEC}	0		0		0				ns
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0				ns
Clock										
Clock High time	T_{CH}	3.5		3.0		3.0				ns
Clock Low time	T_{CL}	3.5		3.0		3.0				ns
Set/Reset Direct										
Width (High)	T_{RPW}	3.5		3.0		3.0				ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		4.5		3.8		3.6			ns
Global Set/Reset										
Minimum GSR Pulse Width	T_{MRW}		13.0		11.5		11.5			ns
Delay from GSR input to any Q (XC4028EX)	T_{MRQ}		22.8		19.0		19.0			ns
Delay from GSR input to any Q (XC4036EX)	T_{MRQ}		24.0		21.0		21.0			ns
Toggle Frequency (Note 1)	F_{TOG}		143		166		166			MHz
		PRELIMINARY								

Note 1: Maximum flip-flop toggle rate for export control purposes.

XC4000EX CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

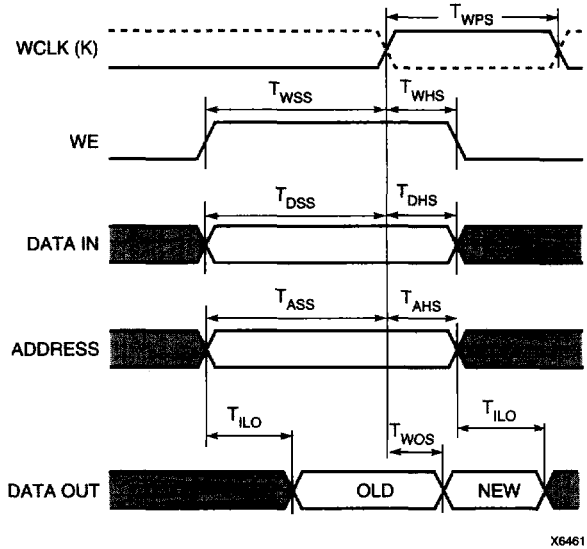
Single Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x2	T_{WCS}	11.0		9.0		9.0				ns
	32x1	T_{WCTS}	11.0		9.0		9.0				ns
Clock K pulse width (active edge)	16x2	T_{WPS}	5.5		4.5		4.5				ns
	32x1	T_{WPTS}	5.5		4.5		4.5				ns
Address setup time before clock K	16x2	T_{ASS}	2.7		2.3		2.2				ns
	32x1	T_{ASTS}	2.6		2.2		2.2				ns
Address hold time after clock K	16x2	T_{AHS}	0		0		0				ns
	32x1	T_{AHTS}	0		0		0				ns
DIN setup time before clock K	16x2	T_{DSS}	2.4		2.0		2.0				ns
	32x1	T_{DSTS}	2.9		2.5		2.5				ns
DIN hold time after clock K	16x2	T_{DHS}	0		0		0				ns
	32x1	T_{DHTS}	0		0		0				ns
WE setup time before clock K	16x2	T_{WSS}	2.3		2.0		2.0				ns
	32x1	T_{WSTS}	2.1		1.8		1.8				ns
WE hold time after clock K	16x2	T_{WHS}	0		0		0				ns
	32x1	T_{WHTS}	0		0		0				ns
Data valid after clock K	16x2	T_{WOS}		8.2		6.8		6.8			ns
	32x1	T_{WOTS}		10.1		8.4		8.2			ns

Notes: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Applicable Read timing specifications are identical to Level-Sensitive Read timing.

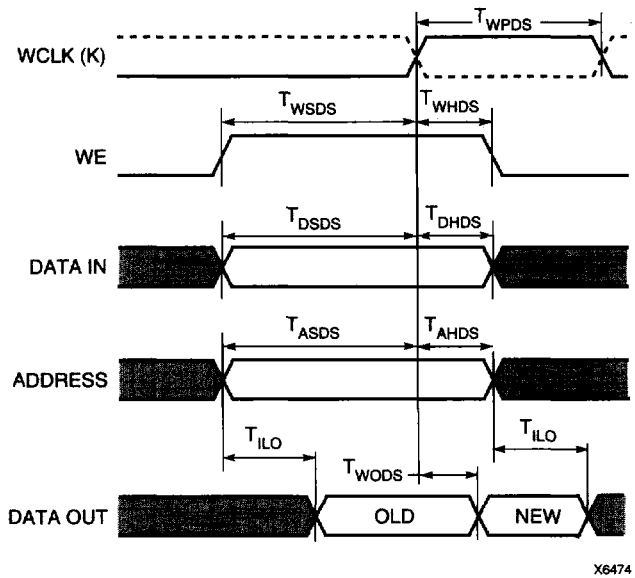
Dual-Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x1	T_{WCDS}	11.0		9.0		9.0				ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	5.5		4.5		4.5				ns
Address setup time before clock K	16x1	T_{ASDS}	3.1		2.6		2.5				ns
Address hold time after clock K	16x1	T_{AHDS}	0		0		0				ns
DIN setup time before clock K	16x1	T_{DSDS}	2.9		2.5		2.5				ns
DIN hold time after clock K	16x1	T_{DHDS}	0		0		0				ns
WE setup time before clock K	16x1	T_{WSDS}	2.1		1.8		1.8				ns
WE hold time after clock K	16x1	T_{WHDS}	0		0		0				ns
Data valid after clock K	16x1	T_{WODS}		9.4		7.8		7.8			ns

Note: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XC4000EX CLB RAM Synchronous (Edge-Triggered) Write Timing



XC4000EX CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



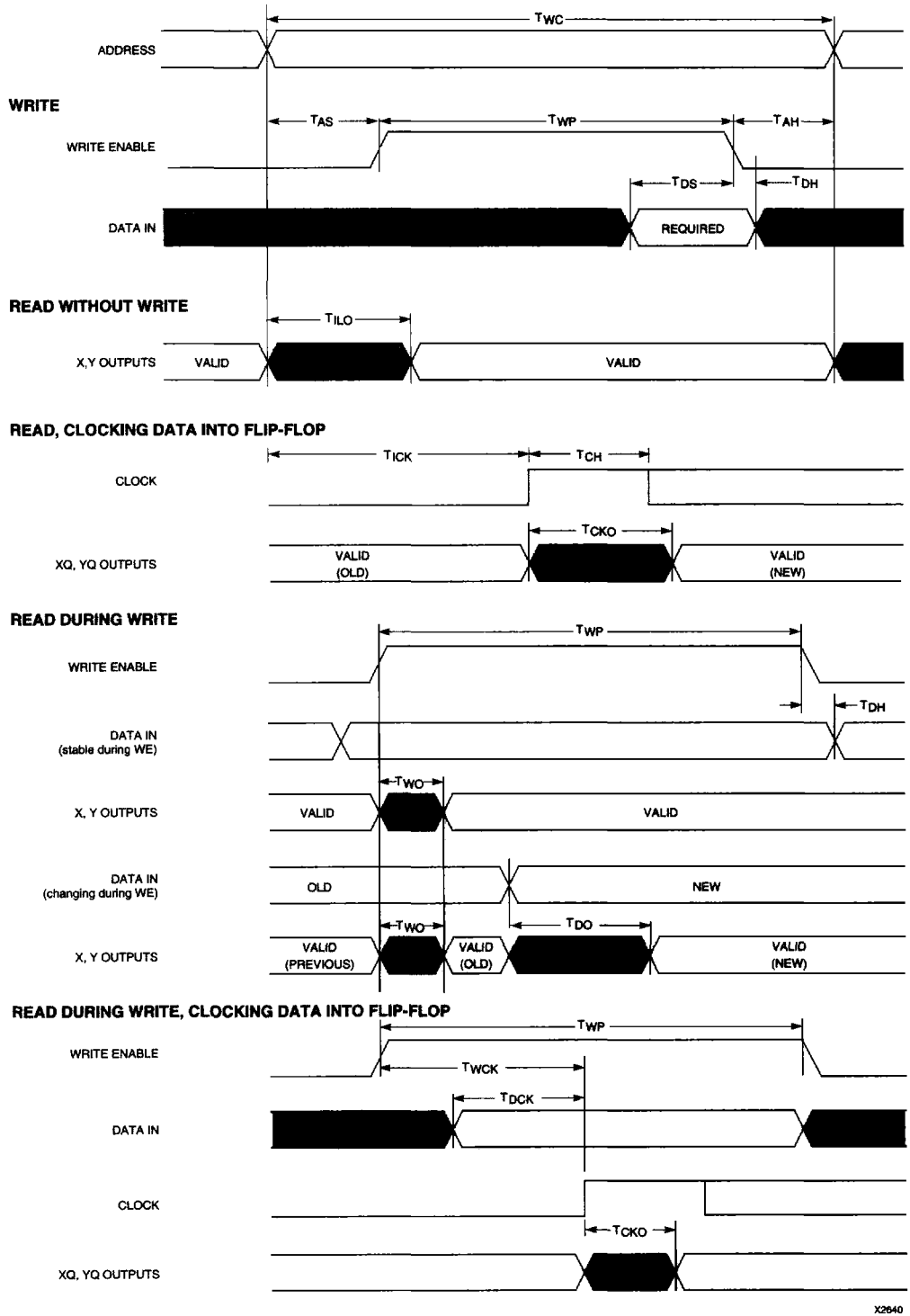
XC4000EX CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

	Speed Grade		-4		-3		-2		-1		Units
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Operation											
Address write cycle time	16x2	T_{WC}	10.6		9.2		8.0				ns
	32x1	T_{WCT}	10.6		9.2		8.0				ns
Write Enable pulse width (High)	16x2	T_{WP}	5.3		4.6		4.0				ns
	32x1	T_{WPT}	5.3		4.6		4.0				ns
Address setup time before WE	16x2	T_{AS}	2.8		2.4		2.0				ns
	32x1	T_{AST}	2.9		2.5		2.0				ns
Address hold time after end of WE	16x2	T_{AH}	1.7		1.4		1.4				ns
	32x1	T_{AHT}	1.7		1.4		1.4				ns
DIN setup time before end of WE	16x2	T_{DS}	1.1		0.9		0.8				ns
	32x1	T_{DST}	1.1		0.9		0.8				ns
DIN hold time after end of WE	16x2	T_{DH}	6.6		5.7		5.0				ns
	32x1	T_{DHT}	6.6		5.7		5.0				ns
Read Operation											
Address read cycle time	16x2	T_{RC}	4.5		3.1		3.1				ns
	32x1	T_{RCT}	6.5		5.5		5.5				ns
Data valid after address change (no Write Enable)	16x2	T_{ILO}		2.2		1.8		1.5			ns
	32x1	T_{IHO}		3.8		3.2		2.7			ns
Read Operation, Clocking Data into Flip-Flop											
Address setup time before clock K	16x2	T_{ICK}	1.5		1.2		1.2				ns
	32x1	T_{IHCK}	3.2		2.6		2.6				ns
Read During Write											
Data valid after WE goes active (DIN stable before WE)	16x2	T_{WO}		6.5		5.7		4.9			ns
	32x1	T_{WOT}		7.4		6.5		5.6			ns
Data valid after DIN (DIN changes during WE)	16x2	T_{DO}		7.7		6.7		5.8			ns
	32x1	T_{DOT}		8.2		7.2		6.2			ns
Read During Write, Clocking Data into Flip-Flop											
WE setup time before clock K	16x2	T_{WCK}	7.1		6.2		5.5				ns
	32x1	T_{WCKT}	9.2		8.1		7.0				ns
Data setup time before clock K	16x2	T_{DCK}	5.9		5.2		4.6				ns
	32x1	T_{DCKT}	8.4		7.4		6.4				ns
			Preliminary								

Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XC4000EX CLB RAM Asynchronous (Level-Sensitive) Timing Characteristics



XC4000EX Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted.

XC4000EX Output Flip-Flop, Clock to Out

		Speed Grade	-4	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	
Global Low Skew Clock to TTL Output (fast) using OFF	T_{ICKOF}	XC4028EX	16.6	13.7	12.4		ns
		XC4036EX	17.2	14.1	13.1		ns
Global Early Clock to TTL Output (fast) using OFF	T_{ICKEOF}	XC4028EX	13.1	10.6	10.2		ns
		XC4036EX	13.3	10.8	10.4		ns

OFF = Output Flip Flop

XC4000EX Output MUX, Clock to Out

		Speed Grade	-4	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	
Global Low Skew Clock to TTL Output (fast) using OMUX	T_{PFPF}	XC4028EX	15.9	13.1	11.8		ns
		XC4036EX	16.5	13.5	12.5		ns
Global Early Clock to TTL Output (fast) using OMUX	T_{PEFPF}	XC4028EX	12.4	10.0	9.6		ns
		XC4036EX	12.6	10.2	9.8		ns

OMUX = Output MUX

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at TTL threshold with 35 pF external capacitive load.
Set-up time is measured with the fastest route and the lightest load. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

XC4000EX Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

	Speed Grade		-4	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	
For TTL output FAST add	T_{TTLOF}	All Devices	0	0	0		ns
For TTL output SLOW add	T_{TTLO}	All Devices	2.9	2.4	2.4		ns
For CMOS FAST output add	T_{CMOSOF}	All Devices	1.0	0.8	0.8		ns
For CMOS SLOW output add	T_{CMOSO}	All Devices	3.6	3.0	3.0		ns

XC4000EX Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted

XC4000EX Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-4	-3	-2	-1	Units
Description	Symbol	Device	Min	Min	Min	Min	
Input Setup Time, using Global Low Skew clock and IFF (full delay)	T_{PSD}	XC4028EX	8.0	6.8	6.8		ns
		XC4036EX	8.0	6.8	6.8		ns
Input Hold Time, using Global Low Skew clock and IFF (full delay)	T_{PHD}	XC4028EX	0	0	0		ns
		XC4036EX	0	0	0		ns

IFF = Flip-Flop or Latch

Preliminary

XC4000EX Global Early Clock, Set-Up and Hold for IFF

		Speed Grade	-4	-3	-2	-1	Units
Description	Symbol	Device	Min	Min	Min	Min	
Input Setup Time, using Global Early clock and IFF (partial delay)	T_{PSEP}	XC4028EX	6.5	5.4	5.4		ns
		XC4036EX	6.5	5.4	5.4		ns
Input Hold Time, using Global Early clock and IFF (partial delay)	T_{PHEP}	XC4028EX	0	0	0		ns
		XC4036EX	0	0	0		ns

IFF = Flip-Flop or Latch

Preliminary

Note: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

XC4000EX Global Early Clock, Set-Up and Hold for FCL

		Speed Grade	-4	-3	-2	-1	Units
Description	Symbol	Device	Min	Min	Min	Min	
Input Setup Time, using Global Early clock and FCL (partial delay)	T_{PFSEP}	XC4028EX	3.4	3.4	3.4		ns
		XC4036EX	4.4	4.2	4.2		ns
Input Hold Time, using Global Early clock and FCL (partial delay)	T_{PFHEP}	XC4028EX	0	0	0		ns
		XC4036EX	0	0	0		ns

FCL = Fast Capture Latch

Preliminary

Notes: For CMOS output levels, see the Output Level and Slew Rate Adjustments tables on page 10.
Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.
Note:Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

XC4000EX Input Threshold and Slew Rate Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

	Speed Grade		-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	
For TTL input add	T_{TTLI}	All Devices	0	0	0		ns
For CMOS input add	T_{CMOSI}	All Devices	0.3	0.2	0.2		ns

Preliminary

XC4000EX IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

		Speed Grade	-4	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	**Min**	
Clocks							
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All devices	3.2	2.6	2.6		ns
Propagation Delays			**Max**	**Max**	**Max**	**Max**	
Pad to I1, I2	T_{PID}	All devices	2.2	1.9	1.8		ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices	3.8	3.2	3.0		ns
Pad to I1, I2 via transparent input latch, partial delay	T_{PPLI}	XC4028EX	13.3	11.1	10.9		ns
		XC4036EX	14.5	12.1	11.9		ns
Pad to I1, I2 via transparent input latch, full delay	T_{PDLI}	XC4028EX	18.2	15.2	14.9		ns
		XC4036EX	19.4	16.2	15.9		ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All devices	5.3	4.4	4.2		ns
Pad to I1, I2 via transparent FCL and input latch, partial delay	T_{PPFLI}	XC4028EX	13.6	11.3	11.1		ns
		XC4036EX	14.8	12.3	12.1		ns
Propagation Delays							
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices	3.0	2.5	2.4		ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices	3.2	2.7	2.6		ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All devices	6.2	5.2	5.0		ns
Global Set/Reset							
Minimum GSR Pulse Width	T_{MRW}	All devices	13.0	11.5	11.5		ns
Delay from GSR input to any Q	T_{RRI}	XC4028EX	22.8	19.0	19.0		ns
Delay from GSR input to any Q	T_{RRI}	XC4036EX	24.0	21.0	21.0		ns

FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch

Notes: For CMOS output levels, see the Output Level and Slew Rate Adjustments table on page 10.
For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 11.

XC4000EX IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

		Speed Grade	-4	-3	-2	-1	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	**Min**	
Setup Times							
Pad to Clock (IK), no delay	T_{PICK}	All devices	2.5	2.0	2.0		ns
Pad to Clock (IK), partial delay	T_{PICKP}	XC4028EX	10.8	9.0	9.0		ns
		XC4036EX	12.0	10.0	10.0		ns
Pad to Clock (IK), full delay	T_{PICKD}	XC4028EX	15.7	13.1	13.1		ns
		XC4036EX	16.9	14.1	14.1		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	All devices	3.9	3.3	3.3		ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	T_{PICKFP}	XC4028EX	12.3	10.2	10.2		ns
		XC4036EX	13.5	11.2	11.2		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All devices	0.8	0.7	0.7		ns
Pad to Fast Capture Latch Enable (OK), partial delay	T_{POCKP}	XC4028EX	9.1	7.6	7.6		ns
		XC4036EX	10.3	8.6	8.6		ns
Setup Times (TTL or CMOS Inputs)							
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All devices	0.3	0.2	0.2		ns
Hold Times							
Pad to Clock (IK),							
no delay	T_{IKPI}	All devices	0	0	0		ns
partial delay	T_{IKPIP}	All devices	0	0	0		ns
full delay	T_{IKPID}	All devices	0	0	0		ns
Pad to Clock (IK) via transparent Fast Capture Latch,							
no delay	T_{IKFPI}	All devices	0	0	0		ns
partial delay	T_{IKFPIP}	All devices	0	0	0		ns
full delay	T_{IKFPID}	All devices	0	0	0		ns
Clock Enable (EC) to Clock (IK),							
no delay	T_{IKEC}	All devices	0	0	0		ns
partial delay	T_{IKECP}	All devices	0	0	0		ns
full delay	T_{IKECD}	All devices	0	0	0		ns
Pad to Fast Capture Latch Enable (OK),							
no delay	T_{OKPI}	All devices	0	0	0		ns
partial delay	T_{OKPIP}	All devices	0	0	0		ns

Notes: For CMOS output levels, see the Output Level and Slew Rate Adjustments table on page 10.
For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 11.

XC4000EX IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000EX devices unless otherwise noted.

Description	Symbol	-4 Min	-4 Max	-3 Min	-3 Max	-2 Min	-2 Max	-1 Min	-1 Max	Units
Propagation Delays										
Clock (OK) to Pad	T_{OKPOF}		7.4		6.2		6.0			ns
Output (O) to Pad	T_{OPF}		6.2		5.2		5.0			ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		4.9		4.1		4.1			ns
3-state to Pad active and valid	T_{TSONF}		6.2		5.2		5.0			ns
Output MUX Select (OK) to Pad	T_{OKFPF}		6.7		5.6		5.4			ns
Fast Path Output MUX Input (EC) to Pad	T_{CEFPF}		6.2		5.1		5.0			ns
Slowest Path Output MUX Input (O) to Pad	T_{OFPF}		7.3		6.0		5.9			ns
Setup and Hold Times										
Output (O) to clock (OK) setup time	T_{OOK}	0.6		0.5		0.5				ns
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0				ns
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	0		0		0				ns
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	0		0		0				ns
Clock										
Clock High	T_{CH}	3.5		3.0		3.0				ns
Clock Low	T_{CL}	3.5		3.0		3.0				ns
Global Set/Reset										
Minimum GSR pulse width	T_{MRW}	13.0		11.5		11.5				ns
Delay from GSR input to any Pad (XC4028EX)	T_{RPO}	**30.2**		**25.2**		**25.0**				ns
Delay from GSR input to any Pad (XC4036EX)	T_{RPO}	**31.4**		**27.2**		**27.0**				ns

Notes: Output timing is measured at TTL threshold, with 35pF external capacitive loads.
For CMOS output levels, see the Output Level and Slew Rate Adjustments table on page 10

XC4000E Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC4000E Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000E Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Military	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Note: At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output Measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	Commercial		3.0	mA
		Industrial		6.0	mA
		Military		6.0	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}*	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		-0.02	-0.25	mA
I_{RLL}*	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a MakeBits Tie option.
* Characterized Only.

XC4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

		Speed Grade	-4	-3	-2	-1	
Description	Symbol	Device	Max	Max	Max	Max	Units
From pad through Primary buffer, to any clock K	T_{PG}	XC4003E	7.0	4.7	4.0	3.5	ns
		XC4005E	7.0	4.7	4.3	3.8	ns
		XC4006E	7.5	5.3	5.2	4.6	ns
		XC4008E	8.0	6.1	5.2	4.6	ns
		XC4010E	11.0	6.3	5.4	4.8	ns
		XC4013E	11.5	6.8	5.8	5.2	ns
		XC4020E	12.0	7.0	6.4	6.0	ns
		XC4025E	12.5	7.2	6.9	–	ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4003E	7.5	5.2	4.4	4.0	ns
		XC4005E	7.5	5.2	4.7	4.3	ns
		XC4006E	8.0	5.8	5.6	5.1	ns
		XC4008E	8.5	6.6	5.6	5.1	ns
		XC4010E	11.5	6.8	5.8	5.3	ns
		XC4013E	12.0	7.3	6.2	5.7	ns
		XC4020E	12.5	7.5	6.7	6.5	ns
		XC4025E	13.0	7.7	7.2	–	ns

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	-1	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (LL):							
I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4003E	5.0	4.2	3.4	2.9	ns
		XC4005E	5.0	5.0	4.0	3.4	ns
		XC4006E	6.0	5.9	4.7	4.0	ns
		XC4008E	7.0	6.3	5.0	4.3	ns
		XC4010E	8.0	6.4	5.1	4.4	ns
		XC4013E	9.0	7.2	5.7	4.9	ns
		XC4020E	10.0	8.2	7.3	5.6	ns
		XC4025E	11.0	9.1	7.3	–	ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4003E	5.0	4.2	3.6	3.1	ns
		XC4005E	6.0	5.3	4.5	3.8	ns
		XC4006E	7.8	6.4	5.4	4.6	ns
		XC4008E	8.1	6.8	5.8	4.9	ns
		XC4010E	10.5	6.9	5.9	5.0	ns
		XC4013E	11.0	7.7	6.5	5.5	ns
		XC4020E	12.0	8.7	8.7	7.4	ns
		XC4025E	12.0	9.6	9.6	–	ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4003E	5.5	4.6	3.9	3.5	ns
		XC4005E	7.0	6.0	5.7	4.7	ns
		XC4006E	7.5	6.7	5.7	4.9	ns
		XC4008E	8.0	7.1	6.0	5.2	ns
		XC4010E	8.5	7.3	6.2	5.4	ns
		XC4013E	8.7	7.5	7.0	6.2	ns
		XC4020E	11.0	8.4	7.1	6.3	ns
		XC4025E	11.0	8.4	7.1	–	ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices	1.8	1.5	1.3	1.1	ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 1)	T_{PUS}	XC4003E	20.0	14.0	14.0	12.0	ns
		XC4005E	23.0	16.0	16.0	14.0	ns
		XC4006E	25.0	18.0	18.0	16.0	ns
		XC4008E	27.0	20.0	20.0	16.0	ns
		XC4010E	29.0	22.0	22.0	18.0	ns
		XC4013E	32.0	26.0	26.0	21.0	ns
		XC4020E	35.0	32.5	32.5	26.0	ns
		XC4025E	42.0	39.1	39.1	–	ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4003E	9.0	7.0	6.0	5.4	ns
		XC4005E	10.0	8.0	6.8	5.8	ns
		XC4006E	11.5	9.0	7.7	6.5	ns
		XC4008E	12.5	10.0	8.5	7.5	ns
		XC4010E	13.5	11.0	9.4	8.0	ns
		XC4013E	15.0	13.0	11.7	9.4	ns
		XC4020E	16.0	14.8	14.8	10.5	ns
		XC4025E	18.0	16.5	16.5	–	ns

Preliminary

Note 1: These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

XC4000E Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	-1	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4003E	9.2	5.0	5.0	4.3	ns
		XC4005E	9.5	6.0	6.0	5.1	ns
		XC4006E	12.0	7.0	7.0	6.0	ns
		XC4008E	12.5	8.0	8.0	6.5	ns
		XC4010E	15.0	9.0	9.0	7.5	ns
		XC4013E	16.0	11.0	11.0	8.6	ns
		XC4020E	17.0	13.9	13.9	10.1	ns
		XC4025E	18.0	16.9	16.9	–	ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XC4003E	12.0	7.0	7.0	5.5	ns
		XC4005E	12.5	8.0	8.0	6.4	ns
		XC4006E	14.0	9.0	9.0	7.0	ns
		XC4008E	16.0	10.0	10.0	7.5	ns
		XC4010E	18.0	11.0	11.0	8.5	ns
		XC4013E	19.0	13.0	13.0	10.0	ns
		XC4020E	20.0	15.5	15.5	11.8	ns
		XC4025E	21.0	18.9	18.9	–	ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XC4003E	10.5	6.0	6.0	5.1	ns
		XC4005E	10.5	7.0	7.0	6.0	ns
		XC4006E	13.5	8.0	8.0	6.5	ns
		XC4008E	14.0	9.0	9.0	7.0	ns
		XC4010E	16.0	10.0	10.0	7.5	ns
		XC4013E	17.0	12.0	12.0	10.0	ns
		XC4020E	18.0	15.0	15.0	11.8	ns
		XC4025E	19.0	17.6	17.6	–	ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XC4003E	12.0	8.0	8.0	6.0	ns
		XC4005E	12.5	9.0	9.0	7.0	ns
		XC4006E	14.0	10.0	10.0	7.6	ns
		XC4008E	16.0	11.0	11.0	8.4	ns
		XC4010E	18.0	12.0	12.0	9.2	ns
		XC4013E	19.0	14.0	14.0	10.8	ns
		XC4020E	20.0	16.8	16.8	12.6	ns
		XC4025E	21.0	19.6	19.6	–	ns

Notes: These delays are specified from the decoder input to the decoder output.
Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XC4000E CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays										
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6		1.3	ns
F/G inputs via H to X/Y outputs	T_{IHO}		4.7		4.3		2.7		2.2	ns
C inputs via SR through H to X/Y outputs	T_{HH0O}		4.1		3.3		2.4		1.9	ns
C inputs via H to X/Y outputs	T_{HH1O}		3.7		3.6		2.2		1.6	ns
C inputs via DIN through H to X/Y outputs	T_{HH2O}		4.5		3.6		2.6		1.9	ns
CLB Fast Carry Logic										
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1		1.7	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7		2.5	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4		1.2	ns
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6		1.8	ns
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6		0.5	ns
Sequential Delays										
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8		1.9	ns
Setup Time before Clock K										
F/G inputs	T_{ICK}	4.0		3.0		2.4		1.8		ns
F/G inputs via H	T_{IHCK}	6.1		4.6		3.9		2.8		ns
C inputs via H0 through H	T_{HH0CK}	4.5		3.6		3.5		2.4		ns
C inputs via H1 through H	T_{HH1CK}	5.0		4.1		3.3		2.1		ns
C inputs via H2 through H	T_{HH2CK}	4.8		3.8		3.7		2.5		ns
C inputs via DIN	T_{DICK}	3.0		2.4		2.0		1.0		ns
C inputs via EC	T_{ECCK}	4.0		3.0		2.6		2.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0		1.5		ns
C_{IN} input via F/G	T_{CCK}	2.5		2.1						ns
C_{IN} input via F/G and H	T_{CHCK}	4.2		3.5						ns

XC4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Hold Time after Clock K										
F/G inputs	T_{CKI}	0		0		0		0		ns
F/G inputs via H	T_{CKIH}	0		0		0		0		ns
C inputs via H0 through H	T_{CKHH0}	0		0		0		0		ns
C inputs via H1 through H	T_{CKHH1}	0		0		0		0		ns
C inputs via H2 through H	T_{CKHH2}	0		0		0		0		ns
C inputs via DIN	T_{CKDI}	0		0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		0		ns
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0		0		ns
Clock										
Clock High time	T_{CH}	4.5		4.0		4.0		3.0		ns
Clock Low time	T_{CL}	4.5		4.0		4.0		3.0		ns
Set/Reset Direct										
Width (High)	T_{RPW}	5.5		4.0		4.0		3.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		6.5		4.0		4.0		3.0	ns
Master Set/Reset (Note 1)										
Width (High or Low)	T_{MRW}	13.0		11.5		11.5		10.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		23.0		18.7		17.4		15.0	ns
Global Set/Reset inactive to first active clock K edge	T_{MRK}									
Toggle Frequency (Note 2)	F_{TOG}		111		125		125		166	MHz

Note 1: Timing is based on the XC4005E. For other devices see the XACT timing calculator.
Note 2: Export Control Max. flip-flop toggle rate.

XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

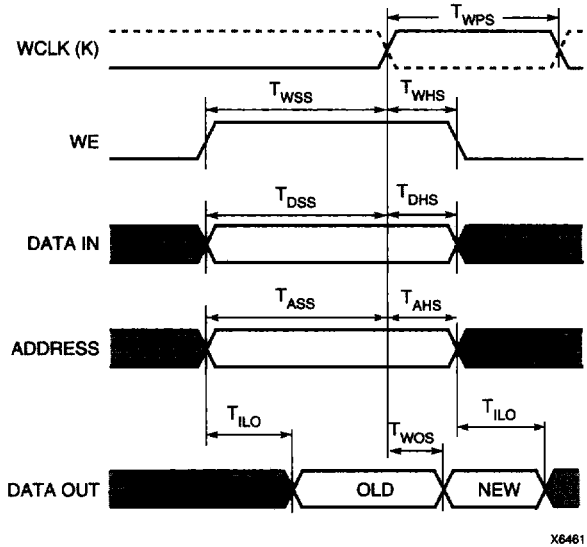
Single Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x2	T_{WCS}	15.0		14.4		11.6		8.0		ns
	32x1	T_{WCTS}	15.0		14.4		11.6		8.0		ns
Clock K pulse width (active edge)	16x2	T_{WPS}	7.5	1 ms	7.2	1 ms	5.8	1 ms	4.0		ns
	32x1	T_{WPTS}	7.5	1 ms	7.2	1 ms	5.8	1 ms	4.0		ns
Address setup time before clock K	16x2	T_{ASS}	2.8		2.4		2.0		1.5		ns
	32x1	T_{ASTS}	2.8		2.4		2.0		1.5		ns
Address hold time after clock K	16x2	T_{AHS}	0		0		0		0		ns
	32x1	T_{AHTS}	0		0		0		0		ns
DIN setup time before clock K	16x2	T_{DSS}	3.5		3.2		2.7		1.5		ns
	32x1	T_{DSTS}	2.5		1.9		1.7		1.5		ns
DIN hold time after clock K	16x2	T_{DHS}	0		0		0		0		ns
	32x1	T_{DHTS}	0		0		0		0		ns
WE setup time before clock K	16x2	T_{WSS}	2.2		2.0		1.6		1.5		ns
	32x1	T_{WSTS}	2.2		2.0		1.6		1.5		ns
WE hold time after clock K	16x2	T_{WHS}	0		0		0		0		ns
	32x1	T_{WHTS}	0		0		0		0		ns
Data valid after clock K	16x2	T_{WOS}		10.3		8.8		7.9		6.5	ns
	32x1	T_{WOTS}		11.6		10.3		9.3		7.0	ns

Notes: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Applicable Read timing specifications are identical to Level-Sensitive Read timing.

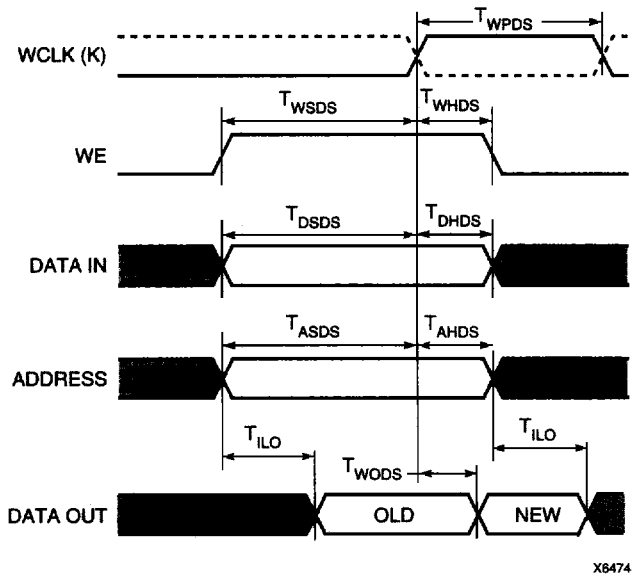
Dual-Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x1	T_{WCDS}	15.0		9.0		11.6		8.0		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}		1 ms	4.5	1 ms	5.8	1 ms	4.0		ns
Address setup time before clock K	16x1	T_{ASDS}	7.5		2.5		2.1		1.5		ns
Address hold time after clock K	16x1	T_{AHDS}	2.8		0		0		0		ns
DIN setup time before clock K	16x1	T_{DSDS}	0		2.5		1.6		1.5		ns
DIN hold time after clock K	16x1	T_{DHDS}	2.2		0		0		0		ns
WE setup time before clock K	16x1	T_{WSDS}	0		1.8		1.6		1.5		ns
WE hold time after clock K	16x1	T_{WHDS}	2.2		0		0		0		ns
Data valid after clock K	16x1	T_{WODS}	0.3	10.0		7.8		7.0		6.5	ns

Note: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XC4000E CLB RAM Synchronous (Edge-Triggered) Write Timing



XC4000E CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



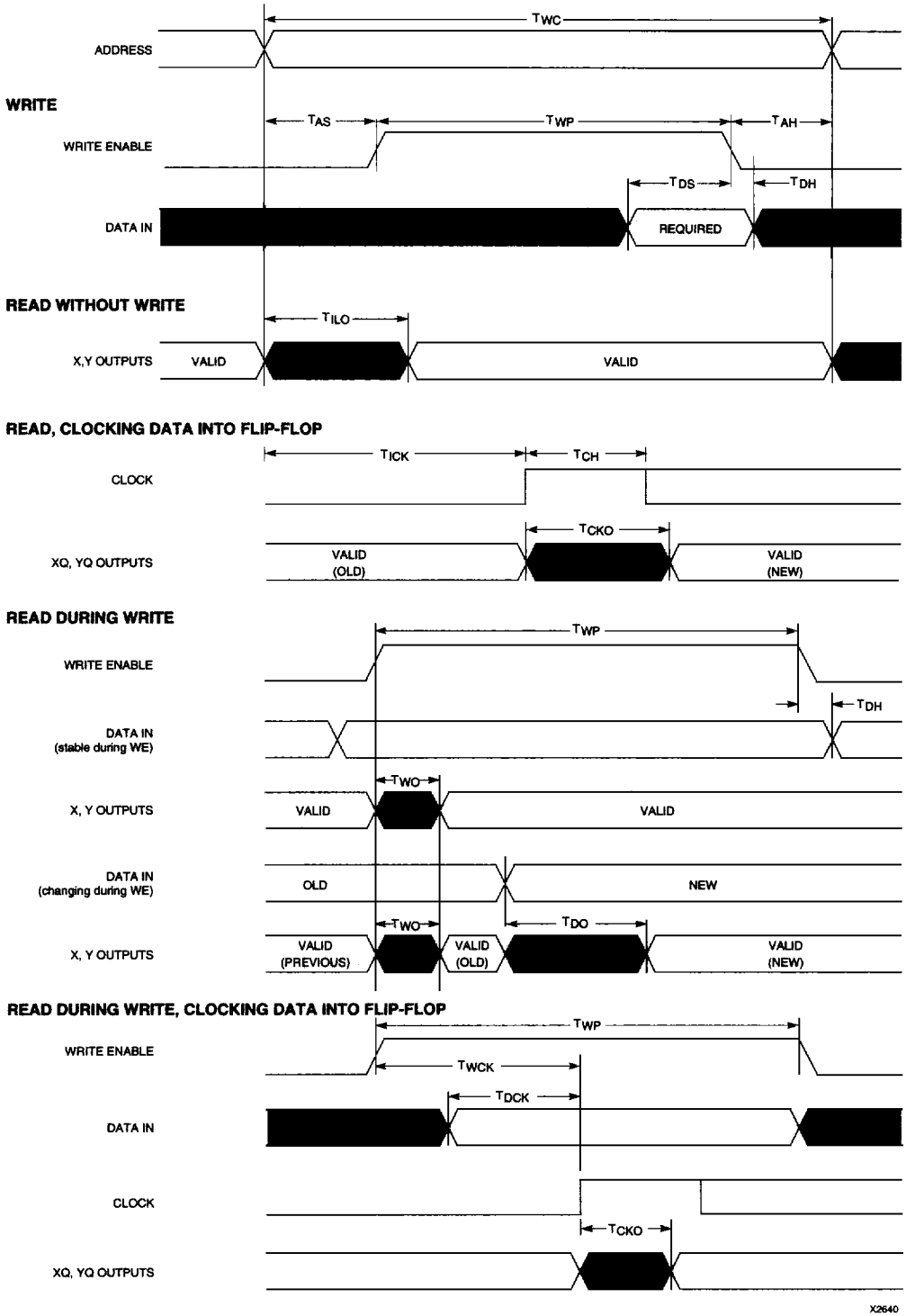
XC4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2		-1		Units
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Operation											
Address write cycle time	16x2	T_{WC}	8.0		8.0		8.0		8.0		ns
	32x1	T_{WCT}	8.0		8.0		8.0		8.0		ns
Write Enable pulse width (High)	16x2	T_{WP}	4.0		4.0		4.0		4.0		ns
	32x1	T_{WPT}	4.0		4.0		4.0		4.0		ns
Address setup time before WE	16x2	T_{AS}	2.0		2.0		2.0		2.0		ns
	32x1	T_{AST}	2.0		2.0		2.0		2.0		ns
Address hold time after end of WE	16x2	T_{AH}	2.5		2.0		2.0		2.0		ns
	32x1	T_{AHT}	2.0		2.0		2.0		2.0		ns
DIN setup time before end of WE	16x2	T_{DS}	4.0		2.2		0.8		0.8		ns
	32x1	T_{DST}	5.0		2.2		0.8		0.8		ns
DIN hold time after end of WE	16x2	T_{DH}	2.0		2.0		2.0		2.0		ns
	32x1	T_{DHT}	2.0		2.0		2.0		2.0		ns
Read Operation											
Address read cycle time	16x2	T_{RC}	4.5		3.1		2.6		2.6		ns
	32x1	T_{RCT}	6.5		5.5		3.8		3.8		ns
Data valid after address change (no Write Enable)	16x2	T_{ILO}		2.7		1.8		1.6		1.6	ns
	32x1	T_{IHO}		4.7		3.2		2.7		2.7	ns
Read Operation, Clocking Data into Flip-Flop											
Address setup time before clock K	16x2	T_{ICK}	4.0		3.0		2.4		2.4		ns
	32x1	T_{IHCK}	6.1		4.6		3.9		3.9		ns
Read During Write											
Data valid after WE goes active (DIN stable before WE)	16x2	T_{WO}		10.0		6.0		4.9		4.9	ns
	32x1	T_{WOT}		12.0		7.3		5.6		5.6	ns
Data valid after DIN (DIN changes during WE)	16x2	T_{DO}		9.0		6.6		5.8		5.8	ns
	32x1	T_{DOT}		11.0		7.6		6.2		6.2	ns
Read During Write, Clocking Data into Flip-Flop											
WE setup time before clock K	16x2	T_{WCK}	8.0		6.0		5.1		5.1		ns
	32x1	T_{WCKT}	9.6		6.8		5.8		5.8		ns
Data setup time before clock K	16x2	T_{DCK}	7.0		5.2		4.4		4.4		ns
	32x1	T_{DCKT}	8.0		6.2		5.3		5.3		ns

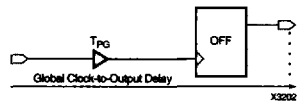
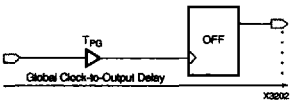
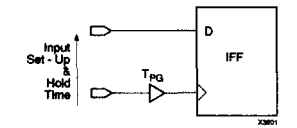
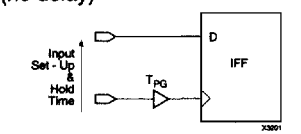
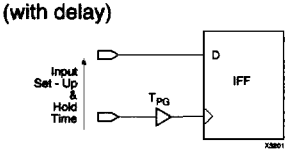
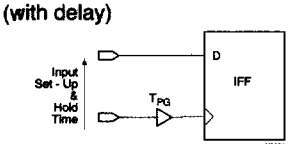
Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XC4000E CLB Level-Sensitive RAM Timing Characteristics



XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

Description	Symbol	Device	Speed Grade -4	-3	-2	-1	Units
Global Clock to Output (fast) using OFF	T_{ICKOF}	XC4003E	12.5	10.2	8.7	5.8	ns
		XC4005E	14.0	10.7	9.1	6.2	ns
		XC4006E	14.5	10.7	9.1	6.4	ns
		XC4008E	15.0	10.8	9.2	6.6	ns
	(Max)	XC4010E	16.0	10.9	9.3	6.8	ns
		XC4013E	16.5	11.0	9.4	7.2	ns
		XC4020E	17.0	11.0	10.2	7.4	ns
		XC4025E	17.0	12.6	10.8	–	ns
Global Clock to Output (slew-limited) using OFF	T_{ICKO}	XC4003E	16.5	14.0	11.5	7.8	ns
		XC4005E	18.0	14.7	12.0	8.2	ns
		XC4006E	18.5	14.7	12.0	8.4	ns
		XC4008E	19.0	14.8	12.1	8.6	ns
	(Max)	XC4010E	20.0	14.9	12.2	8.8	ns
		XC4013E	20.5	15.0	12.8	9.2	ns
		XC4020E	21.0	15.1	12.8	9.4	ns
		XC4025E	21.0	15.3	13.0	–	ns
Input Setup Time, using IFF (no delay)	T_{PSUF}	XC4003E	2.5	2.3	2.3	1.5	ns
		XC4005E	2.0	1.2	1.2	0.8	ns
		XC4006E	1.9	1.0	1.0	0.6	ns
		XC4008E	1.4	0.6	0.6	0.2	ns
	(Min)	XC4010E	1.0	0.2	0.2	0	ns
		XC4013E	0.5	0	0	0	ns
		XC4020E	0	0	0	0	ns
		XC4025E	0	0	0	–	ns
Input Hold Time, using IFF (no delay)	T_{PHF}	XC4003E	4.0	4.0	4.0	1.5	ns
		XC4005E	4.6	4.5	4.5	2.0	ns
		XC4006E	5.0	4.7	4.7	2.0	ns
		XC4008E	6.0	5.1	5.1	2.5	ns
	(Min)	XC4010E	6.0	5.5	5.5	2.5	ns
		XC4013E	7.0	6.5	5.5	3.0	ns
		XC4020E	7.5	6.7	5.7	3.5	ns
		XC4025E	8.0	7.0	5.9	–	ns
Input Setup Time, using IFF (with delay)	T_{PSU}	XC4003E	8.5	7.0	6.0	5.0	ns
		XC4005E	8.5	7.0	6.0	5.0	ns
		XC4006E	8.5	7.0	6.0	5.0	ns
		XC4008E	8.5	7.0	6.0	5.0	ns
	(Min)	XC4010E	8.5	7.0	6.0	5.0	ns
		XC4013E	8.5	7.0	6.0	5.0	ns
		XC4020E	9.5	7.0	6.8	5.0	ns
		XC4025E	9.5	7.6	6.8	–	ns
Input Hold Time, using IFF (with delay)	T_{PH}	XC4003E	0	0	0	0	ns
		XC4005E	0	0	0	0	ns
		XC4006E	0	0	0	0	ns
		XC4008E	0	0	0	0	ns
	(Min)	XC4010E	0	0	0	0	ns
		XC4013E	0	0	0	0	ns
		XC4020E	0	0	0	0	ns
		XC4025E	0	0	0	–	ns

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch

XC4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (TTL Inputs)											
Pad to I1, I2											
Pad to I1, I2 via transparent	T_{PID}	All devices		3.0		2.5		2.0		1.4	ns
latch, no delay											
with delay	T_{PLI}	All devices		4.8		3.6		3.6		2.8	ns
	T_{PDLI}	XC4003E		10.4		9.3		6.9		6.4	ns
		XC4005E		10.8		9.6		7.4		6.5	ns
		XC4006E		10.8		10.2		8.1		6.9	ns
		XC4008E		10.8		10.6		8.2		7.0	ns
		XC4010E		11.0		10.8		8.3		7.3	ns
		XC4013E		11.4		11.2		9.8		8.4	ns
		XC4020E		13.8		12.4		11.5		9.0	ns
		XC4025E		13.8		13.7		12.4		–	ns
Propagation Delays (CMOS Inputs)											
Pad to I1, I2	T_{PIDC}	All devices		5.5		4.1		3.7		1.9	ns
Pad to I1, I2 via transparent											
latch, no delay	T_{PLIC}	All devices		8.8		6.8		6.2		3.3	ns
with delay	T_{PDLIC}	XC4003E		16.5		12.4		11.0		6.9	ns
		XC4005E		16.5		13.2		11.9		7.0	ns
		XC4006E		16.8		13.4		12.1		7.4	ns
		XC4008E		17.3		13.8		12.4		7.4	ns
		XC4010E		17.5		14.0		12.6		7.8	ns
		XC4013E		18.0		14.4		13.0		9.0	ns
		XC4020E		20.8		15.6		14.0		9.5	ns
		XC4025E		20.8		15.6		14.0		–	ns
Propagation Delays											
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		5.6		2.8		2.8		2.7	ns
Clock (IK) to I1, I2											
(latch enable, active Low)	T_{IKLI}	All devices		6.2		4.0		3.9		3.2	ns
Hold Times (Note 1)											
Pad to Clock (IK), no delay	T_{IKPI}	All devices	0		0		0		0		ns
with delay	T_{IKPID}	All devices	0		0		0		0		ns
Clock Enable (EC) to Clock (IK),											
no delay	T_{IKEC}	All devices	1.5		1.5		0.9		0		ns
with delay	T_{IKECD}	All devices	0		0		0		0		ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Description	Speed Grade Symbol	Device	-4 Min	-4 Max	-3 Min	-3 Max	-2 Min	-2 Max	-1 Min	-1 Max	Units
Setup Times (TTL Inputs)											
Pad to Clock (IK), no delay	T_{PICK}	All devices	4.0		2.6		2.0		1.5		ns
with delay	T_{PICKD}	XC4003E	10.9		8.2		6.0		4.8		ns
		XC4005E	10.9		8.7		6.1		5.1		ns
		XC4006E	10.9		9.2		6.2		5.8		ns
		XC4008E	11.1		9.6		6.3		5.8		ns
		XC4010E	11.3		9.8		6.4		6.0		ns
		XC4013E	11.8		10.2		7.9		7.6		ns
		XC4020E	14.0		11.4		9.4		8.2		ns
		XC4025E	14.0		11.4		10.0		–		ns
Setup Time (CMOS Inputs)											
Pad to Clock (IK), no delay	T_{PICKC}	All devices	6.0		3.3		2.4		2.4		ns
with delay	T_{PICKDC}	XC4003E	12.0		8.8		6.9		5.3		ns
		XC4005E	12.0		9.7		8.0		5.6		ns
		XC4006E	12.3		9.9		8.1		6.3		ns
		XC4008E	12.8		10.3		8.2		6.3		ns
		XC4010E	13.0		10.5		8.3		6.5		ns
		XC4013E	13.5		10.9		10.0		7.9		ns
		XC4020E	16.0		12.1		12.1		8.1		ns
		XC4025E	16.0		12.1		12.1		–		ns
(TTL or CMOS)											
Clock Enable (EC) to Clock (IK), no delay	T_{ECIK}	All devices	3.5		2.5		2.1		1.5		ns
with delay	T_{ECIKD}	XC4003E	10.4		8.1		4.3		4.3		ns
		XC4005E	10.4		8.5		5.6		5.0		ns
		XC4006E	10.4		9.1		6.7		6.0		ns
		XC4008E	10.4		9.5		6.9		6.0		ns
		XC4010E	10.7		9.7		7.1		6.5		ns
		XC4013E	11.1		10.1		9.0		8.0		ns
		XC4020E	14.0		11.3		10.6		9.0		ns
		XC4025E	14.0		11.3		11.0		–		ns
Global Set/Reset (Note 3)											
Delay from GSR net through Q to I1, I2	T_{RRI}			12.0		7.8		6.8		6.8	ns
GSR width	T_{MRW}		13.0		11.5		11.5		10.0		ns
GSR inactive to first active Clock (IK) edge	T_{MRI}										

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (TTL Output Levels)										
Clock (OK) to Pad, fast	T_{OKPOF}		7.5		6.5		4.5		3.0	ns
slew-rate limited	T_{OKPOS}		11.5		9.5		7.0		5.0	ns
Output (O) to Pad, fast	T_{OPF}		8.0		5.5		4.8		3.2	ns
slew-rate limited	T_{OPS}		12.0		8.5		7.3		5.2	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		5.0		4.2		3.8		3.0	ns
3-state to Pad active and valid, fast	T_{TSONF}		9.7		8.1		7.3		6.8	ns
slew-rate limited	T_{TSONS}		13.7		11.1		9.8		8.8	ns
Propagation Delays (CMOS Output Levels)										
Clock (OK) to Pad, fast	T_{OKPOFC}		9.5		7.8		7.0		4.0	ns
slew-rate limited	T_{OKPOSC}		13.5		11.6		10.4		7.0	ns
Output (O) to Pad, fast	T_{OPFC}		10.0		9.7		8.7		4.0	ns
slew-rate limited	T_{OPSC}		14.0		13.4		12.1		6.0	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZC}		5.2		4.3		3.9		3.9	ns
3-state to Pad active and valid, fast	T_{TSONFC}		9.1		7.6		6.8		6.8	ns
slew-rate limited	T_{TSONSC}		13.1		11.4		10.2		8.8	ns

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Setup and Hold										
Output (O) to clock (OK) setup time	T_{OOK}	5.0		4.6		3.8		2.3		ns
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0		0		ns
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	4.8		3.5		2.7		2.0		ns
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	1.2		1.2		0.5		0		ns
Clock										
Clock High	T_{CH}	4.5		4.0		4.0			3.0	ns
Clock Low	T_{CL}	4.5		4.0		4.0			3.0	ns
Global Set/Reset (Note 3)										
Delay from GSR net to Pad	T_{RPO}		15.0		11.8		8.7		7.0	ns
GSR width	T_{MRW}	13.0		11.5		11.5				ns
GSR inactive to first active clock (OK) edge	T_{MRO}									

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Setup and Hold										
Input (TDI) to clock (TCK) setup time	T_{TDITCK}	30.0		30.0		30.0		20.0		ns
Input (TDI) to clock (TCK) hold time	T_{TCKTDI}	0		0		0		0		ns
Input (TMS) to clock (TCK) setup time	T_{TMSTCK}	15.0		15.0		15.0		10.0		ns
Input (TMS) to clock (TCK) hold time	T_{TCKTMS}	0		0		0		0		ns
Propagation Delay										
Clock (TCK) to Pad (TDO)	T_{TCKPO}		30.0		30.0		30.0		20.0	ns
Clock										
Clock (TCK) High	T_{TCKH}	5.0		5.0		5.0		4.0		ns
Clock (TCK) Low	T_{TCKL}	5.0		5.0		5.0		4.0		ns
F_{MAX} (MHz)	F_{MAX}		15.0		15.0		15.0		25.0	ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Device-Specific Pinout Tables

Device-specific tables include all packages for each XC4000 and XC4000X Series device. They follow the pad locations around the die, and include boundary scan register locations..

Pin Locations for XC4003E Devices

XC4003E Pad Name	PC84	PQ100	VQ100	PG120	Bndry Scan
VCC	P2	P92	P89	G3	-
I/O (A8)	P3	P93	P90	G1	32
I/O (A9)	P4	P94	P91	F1	35
I/O	-	P95	P92	E1	38
I/O	-	P96	P93	F2	41
I/O (A10)	P5	P97	P94	F3	44
I/O (A11)	P6	P98	P95	D1	47
I/O (A12)	P7	P99	P96	C1	50
I/O (A13)	P8	P100	P97	D2	53
I/O (A14)	P9	P1	P98	C2	56
I/O, SGCK1 (A15)	P10	P2	P99	D3	59
VCC	P11	P3	P100	C3	-
GND	P12	P4	P1	C4	-
I/O, PGCK1 (A16)	P13	P5	P2	B2	62
I/O (A17)	P14	P6	P3	B3	65
I/O, TDI	P15	P7	P4	C5	68
I/O, TCK	P16	P8	P5	B4	71
I/O, TMS	P17	P9	P6	B5	74
I/O	P18	P10	P7	A4	77
I/O	-	-	-	C6	80
I/O	-	P11	P8	A5	83
I/O	P19	P12	P9	B6	86
I/O	P20	P13	P10	A6	89
GND	P21	P14	P11	B7	-
VCC	P22	P15	P12	C7	-
I/O	P23	P16	P13	A7	92
I/O	P24	P17	P14	A8	95
I/O	-	P18	P15	A9	98
I/O	-	-	-	B8	101
I/O	P25	P19	P16	C8	104
I/O	P26	P20	P17	A10	107
I/O	P27	P21	P18	B9	110
I/O	-	P22	P19	A11	113
I/O	P28	P23	P20	C9	116
I/O, SCGK2	P29	P24	P21	A12	119
O (M1)	P30	P25	P22	B11	122
GND	P31	P26	P23	C10	-
I (M0)	P32	P27	P24	C11	125
VCC	P33	P28	P25	D11	-
I (M2)	P34	P29	P26	B12	126
I/O, PGCK2	P35	P30	P27	C12	127
I/O (HDC)	P36	P31	P28	A13	130
I/O	-	P32	P29	D12	133
I/O ($\overline{LDC}$)	P37	P33	P30	C13	136
I/O	P38	P34	P31	E12	139
I/O	P39	P35	P32	D13	142
I/O	-	P36	P33	F11	145
I/O	-	P37	P34	E13	148
I/O	P40	P38	P35	F12	151
I/O ($\overline{INIT}$)	P41	P39	P36	F13	154
VCC	P42	P40	P37	G12	-
GND	P43	P41	P38	G11	-
I/O	P44	P42	P39	G13	157
I/O	P45	P43	P40	H13	160
I/O	-	P44	P41	J13	163
I/O	-	P45	P42	H12	166
I/O	P46	P46	P43	H11	169
I/O	P47	P47	P44	K13	172
I/O	P48	P48	P45	J12	175
I/O	P49	P49	P46	L13	178
I/O	P50	P50	P47	M13	181
I/O, SGCK3	P51	P51	P48	L12	184
GND	P52	P52	P49	K11	-
DONE	P53	P53	P50	L11	-
VCC	P54	P54	P51	L10	-
$\overline{PROGRAM}$	P55	P55	P52	M12	-
I/O (D7)	P56	P56	P53	M11	187
I/O, PGCK3	P57	P57	P54	N13	190
I/O (D6)	P58	P58	P55	M10	193
I/O	-	P59	P56	N11	196
I/O (D5)	P59	P60	P57	M9	199
I/O ($\overline{CS0}$)	P60	P61	P58	N10	202
I/O	-	P62	P59	L8	205
I/O	-	P63	P60	N9	208
I/O (D4)	P61	P64	P61	M8	211
I/O	P62	P65	P62	N8	214
VCC	P63	P66	P63	M7	-
GND	P64	P67	P64	L7	-
I/O (D3)	P65	P68	P65	N7	217
I/O ($\overline{RS}$)	P66	P69	P66	N6	220
I/O	-	P70	P67	N5	223
I/O	-	-	-	M6	226
I/O (D2)	P67	P71	P68	L6	229
I/O	P68	P72	P69	N4	232
I/O (D1)	P69	P73	P70	M5	235
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P70	P74	P71	N3	238
I/O (D0, DIN)	P71	P75	P72	N2	241
I/O, SGCK4 (DOUT)	P72	P76	P73	M3	244
CCLK	P73	P77	P74	L4	-
VCC	P74	P78	P75	L3	-
O, TDO	P75	P79	P76	M2	0
GND	P76	P80	P77	K3	-
I/O (A0, $\overline{WS}$)	P77	P81	P78	L2	2
I/O, PGCK4 (A1)	P78	P82	P79	N1	5
I/O (CS1, A2)	P79	P83	P80	K2	8
I/O (A3)	P80	P84	P81	L1	11
I/O (A4)	P81	P85	P82	J2	14
I/O (A5)	P82	P86	P83	K1	17
I/O	-	P87	P84	H3	20
I/O	-	P88	P85	J1	23
I/O (A6)	P83	P89	P86	H2	26
I/O (A7)	P84	P90	P87	H1	29
GND	P1	P91	P88	G2	-

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Additional XC4003E Package Pins

PG120

N.C. Pins					
A1	A2	A3	B1	B10	B13
E2	E3	E11	J3	J11	K12
L5	L9	M1	M4	N12	-

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Pin Locations for XC4005E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4005E/XL Pad Name	PC 84	PQ 100	VQ 100††	TQ 144	PG 156†	PQ 160	PQ 208	Bndry Scan
VCC	P2	P92	P89	P128	H3	P142	P183	-
I/O (A8)	P3	P93	P90	P129	H1	P143	P184	44
I/O (A9)	P4	P94	P91	P130	G1	P144	P185	47
I/O (A19) ††	-	P95	P92	P131	G2	P145	P186	50
I/O (A18) ††	-	P96	P93	P132	G3	P146	P187	53
I/O (A10)	P5	P97	P94	P133	F1	P147	P190	56
I/O (A11)	P6	P98	P95	P134	F2	P148	P191	59
I/O	-	-	-	P135	E1	P149	P192	62
I/O	-	-	-	P136	E2	P150	P193	65
GND	-	-	-	P137	F3	P151	P194	-
I/O (A12)	P7	P99	P96	P138	E3	P154	P199	68
I/O (A13)	P8	P100	P97	P139	C1	P155	P200	71
I/O	-	-	-	P140	C2	P156	P201	74
I/O	-	-	-	P141	D3	P157	P202	77
I/O (A14)	P9	P1	P98	P142	B1	P158	P203	80
I/O, SGCK1 †, GCK8 †† (A15)	P10	P2	P99	P143	B2	P159	P204	83
VCC	P11	P3	P100	P144	C3	P160	P205	-
GND	P12	P4	P1	P1	C4	P1	P2	-
I/O, PGCK1†, GCK1†† (A16)	P13	P5	P2	P2	B3	P2	P4	86
I/O (A17)	P14	P6	P3	P3	A1	P3	P5	89
I/O	-	-	-	P4	A2	P4	P6	92
I/O	-	-	-	P5	C5	P5	P7	95
I/O, TDI	P15	P7	P4	P6	B4	P6	P8	98
I/O, TCK	P16	P8	P5	P7	A3	P7	P9	101
GND	-	-	-	P8	C6	P10	P14	-
I/O	-	-	-	P9	B5	P11	P15	104
I/O	-	-	-	P10	B6	P12	P16	107
I/O, TMS	P17	P9	P6	P11	A5	P13	P17	110
I/O	P18	P10	P7	P12	C7	P14	P18	113
I/O	-	-	-	P13	B7	P15	P21	116
I/O	-	P11	P8	P14	A6	P16	P22	119
I/O	P19	P12	P9	P15	A7	P17	P23	122
I/O	P20	P13	P10	P16	A8	P18	P24	125
GND	P21	P14	P11	P17	C8	P19	P25	-
VCC	P22	P15	P12	P18	B8	P20	P26	-
I/O	P23	P16	P13	P19	C9	P21	P27	128
I/O	P24	P17	P14	P20	B9	P22	P28	131
I/O	-	P18	P15	P21	A9	P23	P29	134
I/O	-	-	-	P22	B10	P24	P30	137
I/O	P25	P19	P16	P23	C10	P25	P33	140
I/O	P26	P20	P17	P24	A10	P26	P34	143
I/O	-	-	-	P25	A11	P27	P35	146
I/O	-	-	-	P26	B11	P28	P36	149
GND	-	-	-	P27	C11	P29	P37	-
I/O	P27	P21	P18	P28	B12	P32	P42	152
I/O	-	P22	P19	P29	A13	P33	P43	155
I/O	-	-	-	P30	A14	P34	P44	158
I/O	-	-	-	P31	C12	P35	P45	161
I/O	P28	P23	P20	P32	B13	P36	P46	164
I/O, SCGK2 †, GCK2 ††	P29	P24	P21	P33	B14	P37	P47	167
O (M1)	P30	P25	P22	P34	A15	P38	P48	170
GND	P31	P26	P23	P35	C13	P39	P49	-
I (M0)	P32	P27	P24	P36	A16	P40	P50	173
VCC	P33	P28	P25	P37	C14	P41	P55	-
I (M2)	P34	P29	P26	P38	B15	P42	P56	174
I/O, PGCK2 †, GCK3 ††	P35	P30	P27	P39	B16	P43	P57	175
I/O (HDC)	P36	P31	P28	P40	D14	P44	P58	178
I/O	-	-	-	P41	C15	P45	P59	181
I/O	-	-	-	P42	D15	P46	P60	184
I/O	-	P32	P29	P43	E14	P47	P61	187
I/O (LDC)	P37	P33	P30	P44	C16	P48	P62	190

XC4005E/XL Pad Name	PC 84	PQ 100	VQ 100††	TQ 144	PG 156†	PQ 160	PQ 208	Bndry Scan
GND	-	-	-	P45	F14	P51	P67	-
I/O	-	-	-	P46	F15	P52	P68	193
I/O	-	-	-	P47	E16	P53	P69	196
I/O	P38	P34	P31	P48	F16	P54	P70	199
I/O	P39	P35	P32	P49	G14	P55	P71	202
I/O	-	P36	P33	P50	G15	P56	P74	205
I/O	-	P37	P34	P51	G16	P57	P75	208
I/O	P40	P38	P35	P52	H16	P58	P76	211
I/O ($\overline{\text{INIT}}$)	P41	P39	P36	P53	H15	P59	P77	214
VCC	P42	P40	P37	P54	H14	P60	P78	-
GND	P43	P41	P38	P55	J14	P61	P79	-
I/O	P44	P42	P39	P56	J15	P62	P80	217
I/O	P45	P43	P40	P57	J16	P63	P81	220
I/O	-	P44	P41	P58	K16	P64	P82	223
I/O	-	P45	P42	P59	K15	P65	P83	226
I/O	P46	P46	P43	P60	K14	P66	P86	229
I/O	P47	P47	P44	P61	L16	P67	P87	232
I/O	-	-	-	P62	M16	P68	P88	235
I/O	-	-	-	P63	L15	P69	P89	238
GND	-	-	-	P64	L14	P70	P90	-
I/O	P48	P48	P45	P65	P16	P73	P95	241
I/O	P49	P49	P46	P66	M14	P74	P96	244
I/O	-	-	-	P67	N15	P75	P97	247
I/O	-	-	-	P68	P15	P76	P98	250
I/O	P50	P50	P47	P69	N14	P77	P99	253
I/O, SGCK3 †, GCK4 ††	P51	P51	P48	P70	R16	P78	P100	256
GND	P52	P52	P49	P71	P14	P79	P101	-
DONE	P53	P53	P50	P72	R15	P80	P103	-
VCC	P54	P54	P51	P73	P13	P81	P106	-
$\overline{\text{PROGRAM}}$	P55	P55	P52	P74	R14	P82	P108	-
I/O (D7)	P56	P56	P53	P75	T16	P83	P109	259
I/O, PGCK3†, GCK5††	P57	P57	P54	P76	T15	P84	P110	262
I/O	-	-	-	P77	R13	P85	P111	265
I/O	-	-	-	P78	P12	P86	P112	268
I/O (D6)	P58	P58	P55	P79	T14	P87	P113	271
I/O	-	P59	P56	P80	T13	P88	P114	274
GND	-	-	-	P81	P11	P91	P119	-
I/O	-	-	-	P82	R11	P92	P120	277
I/O	-	-	-	P83	T11	P93	P121	280
I/O (D5)	P59	P60	P57	P84	T10	P94	P122	283
I/O ($\overline{\text{CS0}}$)	P60	P61	P58	P85	P10	P95	P123	286
I/O	-	P62	P59	P86	R10	P96	P126	289
I/O	-	P63	P60	P87	T9	P97	P127	292
I/O (D4)	P61	P64	P61	P88	R9	P98	P128	295
I/O	P62	P65	P62	P89	P9	P99	P129	298
VCC	P63	P66	P63	P90	R8	P100	P130	-
GND	P64	P67	P64	P91	P8	P101	P131	-
I/O (D3)	P65	P68	P65	P92	T8	P102	P132	301
I/O ($\overline{\text{RS}}$)	P66	P69	P66	P93	T7	P103	P133	304
I/O	-	P70	P67	P94	T6	P104	P134	307
I/O	-	-	-	P95	R7	P105	P135	310
I/O (D2)	P67	P71	P68	P96	P7	P106	P138	313
I/O	P68	P72	P69	P97	T5	P107	P139	316
I/O	-	-	-	P98	R6	P108	P140	319
I/O	-	-	-	P99	T4	P109	P141	322
GND	-	-	-	P100	P6	P110	P142	-
I/O (D1)	P69	P73	P70	P101	T3	P113	P147	325
I/O ($\overline{\text{RCLK}}$, $\overline{\text{RDY}}$/$\overline{\text{BUSY}}$)	P70	P74	P71	P102	P5	P114	P148	328
I/O	-	-	-	P103	R4	P115	P149	331
I/O	-	-	-	P104	R3	P116	P150	334
I/O (D0, DIN)	P71	P75	P72	P105	P4	P117	P151	337

XC4005E/XL Pad Name	PC 84	PQ 100	VQ 100††	TQ 144	PG 156†	PQ 160	PQ 208	Bndry Scan
I/O, SGCK4 †, GCK6 †† (DOUT)	P72	P76	P73	P106	T2	P118	P152	340
CCLK	P73	P77	P74	P107	R2	P119	P153	-
VCC	P74	P78	P75	P108	P3	P120	P154	-
O, TDO	P75	P79	P76	P109	T1	P121	P159	0
GND	P76	P80	P77	P110	N3	P122	P160	-
I/O (A0, $\overline{WS}$)	P77	P81	P78	P111	R1	P123	P161	2
I/O, PGCK4 †, GCK7 †† (A1)	P78	P82	P79	P112	P2	P124	P162	5
I/O	-	-	-	P113	N2	P125	P163	8
I/O	-	-	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P83	P80	P115	P1	P127	P165	14
I/O (A3)	P80	P84	P81	P116	N1	P128	P166	17
GND	-	-	-	P118	L3	P131	P171	-
I/O	-	-	-	P119	L2	P132	P172	20
I/O	-	-	-	P120	L1	P133	P173	23
I/O (A4)	P81	P85	P82	P121	K3	P134	P174	26
I/O (A5)	P82	P86	P83	P122	K2	P135	P175	29
I/O (A21) ††	-	P87	P84	P123	K1	P137	P178	32
I/O (A20) ††	-	P88	P85	P124	J1	P138	P179	35
I/O (A6)	P83	P89	P86	P125	J2	P139	P180	38
I/O (A7)	P84	P90	P87	P126	J3	P140	P181	41
GND	P1	P91	P88	P127	H2	P141	P182	-

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† = E only
†† = XL only

Additional XC4005E/XL Package Pins

TQ144

N.C. Pins					
P117	-	-	-	-	-

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PG156

N.C. Pins					
A4	A12	D1	D2	D16	E15
M1	M2	M15	N16	R5	R12
T12	-	-	-	-	-

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PQ160

N.C. Pins					
P8	P9	P30	P31	P49	P50
P71	P72	P89	P90	P111	P112
P129	P130	P136	P152	P153	-

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PQ208

N.C. Pins					
P1	P3	P10	P11	P12	P13
P19	P20	P31	P32	P38	P39
P40	P41	P51	P52	P53	P54
P63	P64	P65	P66	P72	P73
P84	P85	P91	P92	P93	P94
P102	P104	P105	P107	P115	P116
P117	P118	P124	P125	P136	P137
P143	P144	P145	P146	P155	P156
P157	P158	P167	P168	P169	P170
P176	P177	P188	P189	P195	P196
P197	P198	P206	P207	P208	-

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Pin Locations for XC4006E Devices

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
VCC	P2	P128	H3	P142	P183	-
I/O (A8)	P3	P129	H1	P143	P184	50
I/O (A9)	P4	P130	G1	P144	P185	53
I/O	-	P131	G2	P145	P186	56
I/O	-	P132	G3	P146	P187	59
I/O (A10)	P5	P133	F1	P147	P190	62
I/O (A11)	P6	P134	F2	P148	P191	65
I/O	-	P135	E1	P149	P192	68
I/O	-	P136	E2	P150	P193	71
GND	-	P137	F3	P151	P194	-
I/O	-	-	D1	P152	P197	74
I/O	-	-	D2	P153	P198	77
I/O (A12)	P7	P138	E3	P154	P199	80
I/O (A13)	P8	P139	C1	P155	P200	83
I/O	-	P140	C2	P156	P201	86
I/O	-	P141	D3	P157	P202	89
I/O (A14)	P9	P142	B1	P158	P203	92
I/O, SGCK1 (A15)	P10	P143	B2	P159	P204	95
VCC	P11	P144	C3	P160	P205	-
GND	P12	P1	C4	P1	P2	-
I/O, PGCK1 (A16)	P13	P2	B3	P2	P4	98
I/O (A17)	P14	P3	A1	P3	P5	101
I/O	-	P4	A2	P4	P6	104
I/O	-	P5	C5	P5	P7	107
I/O, TDI	P15	P6	B4	P6	P8	110
I/O, TCK	P16	P7	A3	P7	P9	113
I/O	-	-	A4	P8	P10	116
I/O	-	-	-	P9	P11	119
GND	-	P8	C6	P10	P14	-

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
I/O	-	P9	B5	P11	P15	122
I/O	-	P10	B6	P12	P16	125
I/O, TMS	P17	P11	A5	P13	P17	128
I/O	P18	P12	C7	P14	P18	131
I/O	-	P13	B7	P15	P21	134
I/O	-	P14	A6	P16	P22	137
I/O	P19	P15	A7	P17	P23	140
I/O	P20	P16	A8	P18	P24	143
GND	P21	P17	C8	P19	P25	-
VCC	P22	P18	B8	P20	P26	-
I/O	P23	P19	C9	P21	P27	146
I/O	P24	P20	B9	P22	P28	149
I/O	-	P21	A9	P23	P29	152
I/O	-	P22	B10	P24	P30	155
I/O	P25	P23	C10	P25	P33	158
I/O	P26	P24	A10	P26	P34	161
I/O	-	P25	A11	P27	P35	164
I/O	-	P26	B11	P28	P36	167
GND	-	P27	C11	P29	P37	-
I/O	-	-	A12	P30	P40	170
I/O	-	-	-	P31	P41	173
I/O	P27	P28	B12	P32	P42	176
I/O	-	P29	A13	P33	P43	179
I/O	-	P30	A14	P34	P44	182
I/O	-	P31	C12	P35	P45	185
I/O	P28	P32	B13	P36	P46	188
I/O, SCGK2	P29	P33	B14	P37	P47	191
O (M1)	P30	P34	A15	P38	P48	194
GND	P31	P35	C13	P39	P49	-

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
I (M0)	P32	P36	A16	P40	P50	197
VCC	P33	P37	C14	P41	P55	-
I (M2)	P34	P38	B15	P42	P56	198
I/O, PGCK2	P35	P39	B16	P43	P57	199
I/O (HDC)	P36	P40	D14	P44	P58	202
I/O	-	P41	C15	P45	P59	205
I/O	-	P42	D15	P46	P60	208
I/O	-	P43	E14	P47	P61	211
I/O (LDC)	P37	P44	C16	P48	P62	214
I/O	-	-	E15	P49	P63	217
I/O	-	-	D16	P50	P64	220
GND	-	P45	F14	P51	P67	-
I/O	-	P46	F15	P52	P68	223
I/O	-	P47	E16	P53	P69	226
I/O	P38	P48	F16	P54	P70	229
I/O	P39	P49	G14	P55	P71	232
I/O	-	P50	G15	P56	P74	235
I/O	-	P51	G16	P57	P75	238
I/O	P40	P52	H16	P58	P76	241
I/O (INIT)	P41	P53	H15	P59	P77	244
VCC	P42	P54	H14	P60	P78	-
GND	P43	P55	J14	P61	P79	-
I/O	P44	P56	J15	P62	P80	247
I/O	P45	P57	J16	P63	P81	250
I/O	-	P58	K16	P64	P82	253
I/O	-	P59	K15	P65	P83	256
I/O	P46	P60	K14	P66	P86	259
I/O	P47	P61	L16	P67	P87	262
I/O	-	P62	M16	P68	P88	265
I/O	-	P63	L15	P69	P89	268
GND	-	P64	L14	P70	P90	-
I/O	-	-	N16	P71	P93	271
I/O	-	-	M15	P72	P94	274
I/O	P48	P65	P16	P73	P95	277
I/O	P49	P66	M14	P74	P96	280
I/O	-	P67	N15	P75	P97	283
I/O	-	P68	P15	P76	P98	286
I/O	P50	P69	N14	P77	P99	289
I/O, SGCK3	P51	P70	R16	P78	P100	292
GND	P52	P71	P14	P79	P101	-
DONE	P53	P72	R15	P80	P103	-
VCC	P54	P73	P13	P81	P106	-
PROGRAM	P55	P74	R14	P82	P108	-
I/O (D7)	P56	P75	T16	P83	P109	295
I/O, PGCK3	P57	P76	T15	P84	P110	298
I/O	-	P77	R13	P85	P111	301
I/O	-	P78	P12	P86	P112	304
I/O (D6)	P58	P79	T14	P87	P113	307
I/O	-	P80	T13	P88	P114	310
I/O	-	-	R12	P89	P115	313
I/O	-	-	T12	P90	P116	316
GND	-	P81	P11	P91	P119	-
I/O	-	P82	R11	P92	P120	319
I/O	-	P83	T11	P93	P121	322
I/O (D5)	P59	P84	T10	P94	P122	325
I/O (CS0)	P60	P85	P10	P95	P123	328
I/O	-	P86	R10	P96	P126	331
I/O	-	P87	T9	P97	P127	334
I/O (D4)	P61	P88	R9	P98	P128	337
I/O	P62	P89	P9	P99	P129	340
VCC	P63	P90	R8	P100	P130	-
GND	P64	P91	P8	P101	P131	-
I/O (D3)	P65	P92	T8	P102	P132	343
I/O (RS)	P66	P93	T7	P103	P133	346
I/O	-	P94	T6	P104	P134	349
I/O	-	P95	R7	P105	P135	352
I/O (D2)	P67	P96	P7	P106	P138	355
I/O	P68	P97	T5	P107	P139	358
I/O	-	P98	R6	P108	P140	361
I/O	-	P99	T4	P109	P141	364
GND	-	P100	P6	P110	P142	-
I/O	-	-	R5	P111	P145	367
I/O	-	-	-	P112	P146	370
I/O (D1)	P69	P101	T3	P113	P147	373
I/O (RCLK, RDY/BUSY)	P70	P102	P5	P114	P148	376
I/O	-	P103	R4	P115	P149	379
I/O	-	P104	R3	P116	P150	382
I/O (D0, DIN)	P71	P105	P4	P117	P151	385
I/O, SGCK4 (DOUT)	P72	P106	T2	P118	P152	388
CCLK	P73	P107	R2	P119	P153	-
VCC	P74	P108	P3	P120	P154	-
O, TDO	P75	P109	T1	P121	P159	0
GND	P76	P110	N3	P122	P160	-
I/O (A0, WS)	P77	P111	R1	P123	P161	2
I/O, PGCK4 (A1)	P78	P112	P2	P124	P162	5
I/O	-	P113	N2	P125	P163	8
I/O	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P115	P1	P127	P165	14
I/O (A3)	P80	P116	N1	P128	P166	17
I/O	-	P117	M2	P129	P167	20
I/O	-	-	M1	P130	P168	23
GND	-	P118	L3	P131	P171	-
I/O	-	P119	L2	P132	P172	26
I/O	-	P120	L1	P133	P173	29
I/O (A4)	P81	P121	K3	P134	P174	32
I/O (A5)	P82	P122	K2	P135	P175	35
I/O	-	P123	K1	P137	P178	38
I/O	-	P124	J1	P138	P179	41
I/O (A6)	P83	P125	J2	P139	P180	44
I/O (A7)	P84	P126	J3	P140	P181	47
GND	P1	P127	H2	P141	P182	-

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Additional XC4006E Package Pins

PQ160

N.C. Pins				
P136	-	-	-	-

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PQ208

N.C. Pins				
P1	P3	P12	P13	P19
P20	P31	P32	P38	P39
P51	P52	P53	P54	P65
P66	P72	P73	P84	P85
P91	P92	P102	P104	P105
P107	P117	P118	P124	P125
P136	P137	P143	P144	P155
P156	P157	P158	P169	P170
P176	P177	P188	P189	P195
P196	P206	P207	P208	-

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Pin Locations for XC4008E Devices

XC4008E Pad Name	PC84	PQ160	PG191	PQ208	Bndry Scan
VCC	P2	P142	J4	P183	-
I/O (A8)	P3	P143	J3	P184	56
I/O (A9)	P4	P144	J2	P185	59
I/O	-	P145	J1	P186	62
I/O	-	P146	H1	P187	65
I/O	-	-	H2	P188	68
I/O	-	-	H3	P189	71
I/O (A10)	P5	P147	G1	P190	74
I/O (A11)	P6	P148	G2	P191	77
I/O	-	P149	F1	P192	80
I/O	-	P150	E1	P193	83
GND	-	P151	G3	P194	-
I/O	-	P152	C1	P197	86
I/O	-	P153	E2	P198	89
I/O (A12)	P7	P154	F3	P199	92
I/O (A13)	P8	P155	D2	P200	95
I/O	-	P156	B1	P201	98
I/O	-	P157	E3	P202	101
I/O (A14)	P9	P158	C2	P203	104
I/O, SGCK1 (A15)	P10	P159	B2	P204	107
VCC	P11	P160	D3	P205	-
GND	P12	P1	D4	P2	-
I/O, PGCK1 (A16)	P13	P2	C3	P4	110
I/O (A17)	P14	P3	C4	P5	113
I/O	-	P4	B3	P6	116
I/O	-	P5	C5	P7	119
I/O, TDI	P15	P6	A2	P8	122
I/O, TCK	P16	P7	B4	P9	125
I/O	-	P8	C6	P10	128
I/O	-	P9	A3	P11	131
GND	-	P10	C7	P14	-
I/O	-	P11	A4	P15	134
I/O	-	P12	A5	P16	137
I/O, TMS	P17	P13	B7	P17	140
I/O	P18	P14	A6	P18	143
I/O	-	-	C8	P19	146
I/O	-	-	A7	P20	149
I/O	-	P15	B8	P21	152
I/O	-	P16	A8	P22	155
I/O	P19	P17	B9	P23	158
I/O	P20	P18	C9	P24	161
GND	P21	P19	D9	P25	-
VCC	P22	P20	D10	P26	-
I/O	P23	P21	C10	P27	164
I/O	P24	P22	B10	P28	167
I/O	-	P23	A9	P29	170
I/O	-	P24	A10	P30	173
I/O	-	-	A11	P31	176
I/O	-	-	C11	P32	179
I/O	P25	P25	B11	P33	182
I/O	P26	P26	A12	P34	185
I/O	-	P27	B12	P35	188
I/O	-	P28	A13	P36	191
GND	-	P29	C12	P37	-
I/O	-	P30	A15	P40	194
I/O	-	P31	C13	P41	197
I/O	P27	P32	B14	P42	200
I/O	-	P33	A16	P43	203
I/O	-	P34	B15	P44	206
I/O	-	P35	C14	P45	209
I/O	P28	P36	A17	P46	212
I/O, SCGK2	P29	P37	B16	P47	215
O (M1)	P30	P38	C15	P48	218
GND	P31	P39	D15	P49	-
I (M0)	P32	P40	A18	P50	221
VCC	P33	P41	D16	P55	-
I (M2)	P34	P42	C16	P56	222
I/O, PGCK2	P35	P43	B17	P57	223

XC4008E Pad Name	PC84	PQ160	PG191	PQ208	Bndry Scan
I/O (HDC)	P36	P44	E16	P58	226
I/O	-	P45	C17	P59	229
I/O	-	P46	D17	P60	232
I/O	-	P47	B18	P61	235
I/O ($\overline{\text{LDC}}$)	P37	P48	E17	P62	238
I/O	-	P49	F16	P63	241
I/O	-	P50	C18	P64	244
GND	-	P51	G16	P67	-
I/O	-	P52	E18	P68	247
I/O	-	P53	F18	P69	250
I/O	P38	P54	G17	P70	253
I/O	P39	P55	G18	P71	256
I/O	-	-	H16	P72	259
I/O	-	-	H17	P73	262
I/O	-	P56	H18	P74	265
I/O	-	P57	J18	P75	268
I/O	P40	P58	J17	P76	271
I/O ($\overline{\text{INIT}}$)	P41	P59	J16	P77	274
VCC	P42	P60	J15	P78	-
GND	P43	P61	K15	P79	-
I/O	P44	P62	K16	P80	277
I/O	P45	P63	K17	P81	280
I/O	-	P64	K18	P82	283
I/O	-	P65	L18	P83	286
I/O	-	-	L17	P84	289
I/O	-	-	L16	P85	292
I/O	P46	P66	M18	P86	295
I/O	P47	P67	M17	P87	298
I/O	-	P68	N18	P88	301
I/O	-	P69	P18	P89	304
GND	-	P70	M16	P90	-
I/O	-	P71	T18	P93	307
I/O	-	P72	P17	P94	310
I/O	P48	P73	N16	P95	313
I/O	P49	P74	T17	P96	316
I/O	-	P75	R17	P97	319
I/O	-	P76	P16	P98	322
I/O	P50	P77	U18	P99	325
I/O, SGCK3	P51	P78	T16	P100	328
GND	P52	P79	R16	P101	-
DONE	P53	P80	U17	P103	-
VCC	P54	P81	R15	P106	-
$\overline{\text{PROGRAM}}$	P55	P82	V18	P108	-
I/O (D7)	P56	P83	T15	P109	331
I/O, PGCK3	P57	P84	U16	P110	334
I/O	-	P85	T14	P111	337
I/O	-	P86	U15	P112	340
I/O (D6)	P58	P87	V17	P113	343
I/O	-	P88	V16	P114	346
I/O	-	P89	T13	P115	349
I/O	-	P90	U14	P116	352
GND	-	P91	T12	P119	-
I/O	-	P92	U13	P120	355
I/O	-	P93	V13	P121	358
I/O (D5)	P59	P94	U12	P122	361
I/O ($\overline{\text{CS0}}$)	P60	P95	V12	P123	364
I/O	-	-	T11	P124	367
I/O	-	-	U11	P125	370
I/O	-	P96	V11	P126	373
I/O	-	P97	V10	P127	376
I/O (D4)	P61	P98	U10	P128	379
I/O	P62	P99	T10	P129	382
VCC	P63	P100	R10	P130	-
GND	P64	P101	R9	P131	-
I/O (D3)	P65	P102	T9	P132	385
I/O ($\overline{\text{RS}}$)	P66	P103	U9	P133	388
I/O	-	P104	V9	P134	391
I/O	-	P105	V8	P135	394
I/O	-	-	U8	P136	397

XC4008E Pad Name	PC84	PQ160	PG191	PQ208	Bndry Scan
I/O	-	-	T8	P137	400
I/O (D2)	P67	P106	V7	P138	403
I/O	P68	P107	U7	P139	406
I/O	-	P108	V6	P140	409
I/O	-	P109	U6	P141	412
GND	-	P110	T7	P142	-
I/O	-	P111	U5	P145	415
I/O	-	P112	T6	P146	418
I/O (D1)	P69	P113	V3	P147	421
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P70	P114	V2	P148	424
I/O	-	P115	U4	P149	427
I/O	-	P116	T5	P150	430
I/O (D0, DIN)	P71	P117	U3	P151	433
I/O, SGCK4 (DOUT)	P72	P118	T4	P152	436
CCLK	P73	P119	V1	P153	-
VCC	P74	P120	R4	P154	-
O, TDO	P75	P121	U2	P159	0
GND	P76	P122	R3	P160	-
I/O (A0, $\overline{WS}$)	P77	P123	T3	P161	2
I/O, PGCK4 (A1)	P78	P124	U1	P162	5
I/O	-	P125	P3	P163	8
I/O	-	P126	R2	P164	11
I/O (CS1, A2)	P79	P127	T2	P165	14
I/O (A3)	P80	P128	N3	P166	17
I/O	-	P129	P2	P167	20
I/O	-	P130	T1	P168	23
GND	-	P131	M3	P171	-
I/O	-	P132	P1	P172	26
I/O	-	P133	N1	P173	29
I/O (A4)	P81	P134	M2	P174	32
I/O (A5)	P82	P135	M1	P175	35
I/O	-	-	L3	P176	38
I/O	-	P136	L2	P177	41
I/O	-	P137	L1	P178	44
I/O	-	P138	K1	P179	47
I/O (A6)	P83	P139	K2	P180	50
I/O (A7)	P84	P140	K3	P181	53
GND	P1	P141	K4	P182	-

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Additional XC4008E Package Pins

PG191

N.C. Pins					
A14	B5	B6	B13	D1	D18
F2	F17	N2	N17	R1	R18
V4	V5	V14	V15	-	-

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PQ208

N.C. Pins					
P1	P3	P12	P13	P38	P39
P51	P52	P53	P54	P65	P66
P91	P92	P102	P104	P105	P107
P117	P118	P143	P144	P155	P156
P157	P158	P169	P170	P195	P196
P206	P207	P208	-	-	-

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Pin Locations for XC4010E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/ HQ 208	BG 225†	BG 256††	Bndry Scan
VCC	P2	P92	P128	P142	P155	VCC*	P183	VCC*	VCC*	-
I/O (A8)	P3	P93	P129	P143	P156	J3	P184	E8	C10	62
I/O (A9)	P4	P94	P130	P144	P157	J2	P185	B7	D10	65
I/O (19)	-	P95	P131	P145	P158	J1	P186	A7	A9	68
I/O (18)	-	P96	P132	P146	P159	H1	P187	C7	B9	71
I/O	-	-	-	-	P160	H2	P188	D7	C9	74
I/O	-	-	-	-	P161	H3	P189	E7	D9	77
I/O (A10)	P5	P97	P133	P147	P162	G1	P190	A6	A8	80
I/O (A11)	P6	P98	P134	P148	P163	G2	P191	B6	B8	83
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	-	-	P135	P149	P164	F1	P192	A5	B6	86
I/O	-	-	P136	P150	P165	E1	P193	B5	A5	89
GND	-	-	P137	P151	P166	GND*	P194	GND*	GND*	-
I/O	-	-	-	-	-	F2	P195	D6	C6	92
I/O	-	-	-	-	P167	D1	P196	C5	B5	95
I/O	-	-	-	P152	P168	C1	P197	A4	A4	98
I/O	-	-	-	P153	P169	E2	P198	E6	C5	101
I/O (A12)	P7	P99	P138	P154	P170	F3	P199	B4	B4	104
I/O (A13)	P8	P100	P139	P155	P171	D2	P200	D5	A3	107
I/O	-	-	P140	P156	P172	B1	P201	B3	B3	110
I/O	-	-	P141	P157	P173	E3	P202	F6	B2	113
I/O (A14)	P9	P1	P142	P158	P174	C2	P203	A2	A2	116
I/O, SGCK1 †, GCK8 †† (A15)	P10	P2	P143	P159	P175	B2	P204	C3	C3	119
VCC	P11	P3	P144	P160	P176	VCC*	P205	VCC*	VCC*	-
GND	P12	P4	P1	P1	P1	GND*	P2	GND*	GND*	-
I/O, PGCK1†, GCK1†† (A16)	P13	P5	P2	P2	P2	C3	P4	D4	B1	122
I/O (A17)	P14	P6	P3	P3	P3	C4	P5	B1	C2	125

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/ HQ 208	BG 225†	BG 256††	Bndry Scan
I/O	-	-	P4	P4	P4	B3	P6	C2	D2	128
I/O	-	-	P5	P5	P5	C5	P7	E5	D3	131
I/O, TDI	P15	P7	P6	P6	P6	A2	P8	D3	E4	134
I/O, TCK	P16	P8	P7	P7	P7	B4	P9	C1	C1	137
I/O	-	-	-	P8	P8	C6	P10	D2	D1	140
I/O	-	-	-	P9	P9	A3	P11	G6	E3	143
I/O	-	-	-	-	-	B5	P12	E4	E2	146
I/O	-	-	-	-	-	B6	P13	D1	E1	149
GND	-	-	P8	P10	P10	GND*	P14	GND*	GND*	-
I/O	-	-	P9	P11	P11	A4	P15	F5	G3	152
I/O	-	-	P10	P12	P12	A5	P16	E1	G2	155
I/O, TMS	P17	P9	P11	P13	P13	B7	P17	F4	G1	158
I/O	P18	P10	P12	P14	P14	A6	P18	F3	H3	161
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	-	-	-	-	P15	C8	P19	G4	J2	164
I/O	-	-	-	-	P16	A7	P20	G3	J1	167
I/O	-	-	P13	P15	P17	B8	P21	G2	K2	170
I/O	-	P11	P14	P16	P18	A8	P22	G1	K3	173
I/O	P19	P12	P15	P17	P19	B9	P23	G5	K1	176
I/O	P20	P13	P16	P18	P20	C9	P24	H3	L1	179
GND	P21	P14	P17	P19	P21	GND*	P25	GND*	GND*	-
VCC	P22	P15	P18	P20	P22	VCC*	P26	VCC*	VCC*	-
I/O	P23	P16	P19	P21	P23	C10	P27	H4	L2	182
I/O	P24	P17	P20	P22	P24	B10	P28	H5	L3	185
I/O	-	P18	P21	P23	P25	A9	P29	J2	L4	188
I/O	-	-	P22	P24	P26	A10	P30	J1	M1	191
I/O	-	-	-	-	P27	A11	P31	J3	M2	194
I/O	-	-	-	-	P28	C11	P32	J4	M3	197
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	P25	P19	P23	P25	P29	B11	P33	K2	P1	200
I/O	P26	P20	P24	P26	P30	A12	P34	K3	P2	203

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/ HQ 208	BG 225†	BG 256††	Bndry Scan
I/O	-	-	P25	P27	P31	B12	P35	J6	R1	206
I/O	-	-	P26	P28	P32	A13	P36	L1	P3	209
GND	-	-	P27	P29	P33	GND*	P37	GND*	GND*	-
I/O	-	-	-	-	-	B13	P38	L3	T2	212
I/O	-	-	-	-	-	A14	P39	M1	U1	215
I/O	-	-	-	P30	P34	A15	P40	K5	T3	218
I/O	-	-	-	P31	P35	C13	P41	M2	U2	221
I/O	P27	P21	P28	P32	P36	B14	P42	L4	V1	224
I/O	-	P22	P29	P33	P37	A16	P43	N1	T4	227
I/O	-	-	P30	P34	P38	B15	P44	M3	U3	230
I/O	-	-	P31	P35	P39	C14	P45	N2	V2	233
I/O	P28	P23	P32	P36	P40	A17	P46	K6	W1	236
I/O, SCGK2 †, GCK2 ††	P29	P24	P33	P37	P41	B16	P47	P1	V3	239
O (M1)	P30	P25	P34	P38	P42	C15	P48	N3	W2	242
GND	P31	P26	P35	P39	P43	GND*	P49	GND*	GND*	-
I (M0)	P32	P27	P36	P40	P44	A18	P50	P2	Y1	245
VCC	P33	P28	P37	P41	P45	VCC*	P55	VCC*	VCC*	-
I (M2)	P34	P29	P38	P42	P46	C16	P56	M4	W3	246
I/O, PGCK2 †, GCK3 ††	P35	P30	P39	P43	P47	B17	P57	R2	Y2	247
I/O (HDC)	P36	P31	P40	P44	P48	E16	P58	P3	W4	250
I/O	-	-	P41	P45	P49	C17	P59	L5	V4	253
I/O	-	-	P42	P46	P50	D17	P60	N4	U5	256
I/O	-	P32	P43	P47	P51	B18	P61	R3	Y3	259
I/O ($\overline{LDC}$)	P37	P33	P44	P48	P52	E17	P62	P4	Y4	262
I/O	-	-	-	P49	P53	F16	P63	K7	V5	265
I/O	-	-	-	P50	P54	C18	P64	M5	W5	268
I/O	-	-	-	-	-	D18	P65	R4	Y5	271
I/O	-	-	-	-	-	F17	P66	N5	V6	274
GND	-	-	P45	P51	P55	GND*	P67	GND*	GND*	-
I/O	-	-	P46	P52	P56	E18	P68	R5	W7	277
I/O	-	-	P47	P53	P57	F18	P69	M6	Y7	280
I/O	P38	P34	P48	P54	P58	G17	P70	N6	V8	283
I/O	P39	P35	P49	P55	P59	G18	P71	P6	W8	286
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	-	-	-	-	P60	H16	P72	R6	Y8	289
I/O	-	-	-	-	P61	H17	P73	M7	U9	292
I/O	-	P36	P50	P56	P62	H18	P74	R7	V10	295
I/O	-	P37	P51	P57	P63	J18	P75	L7	Y10	298
I/O	P40	P38	P52	P58	P64	J17	P76	N8	Y11	301
I/O ($\overline{INIT}$)	P41	P39	P53	P59	P65	J16	P77	P8	W11	304
VCC	P42	P40	P54	P60	P66	VCC*	P78	VCC*	VCC*	-
GND	P43	P41	P55	P61	P67	GND*	P79	GND*	GND*	-
I/O	P44	P42	P56	P62	P68	K16	P80	L8	V11	307
I/O	P45	P43	P57	P63	P69	K17	P81	P9	U11	310
I/O	-	P44	P58	P64	P70	K18	P82	R9	Y12	313
I/O	-	P45	P59	P65	P71	L18	P83	N9	W12	316
I/O	-	-	-	-	P72	L17	P84	M9	V12	319
I/O	-	-	-	-	P73	L16	P85	L9	U12	322
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	P46	P46	P60	P66	P74	M18	P86	N10	Y15	325
I/O	P47	P47	P61	P67	P75	M17	P87	K9	V14	328
I/O	-	-	P62	P68	P76	N18	P88	R11	W15	331
I/O	-	-	P63	P69	P77	P18	P89	P11	Y16	334
GND	-	-	P64	P70	P78	GND*	P90	GND*	GND*	-
I/O	-	-	-	-	-	N17	P91	R12	Y17	337
I/O	-	-	-	-	-	R18	P92	L10	V16	340
I/O	-	-	-	P71	P79	T18	P93	P12	W17	343
I/O	-	-	-	P72	P80	P17	P94	M11	Y18	346
I/O	P48	P48	P65	P73	P81	N16	P95	R13	U16	349
I/O	P49	P49	P66	P74	P82	T17	P96	N12	V17	352
I/O	-	-	P67	P75	P83	R17	P97	P13	W18	355
I/O	-	-	P68	P76	P84	P16	P98	K10	Y19	358
I/O	P50	P50	P69	P77	P85	U18	P99	R14	V18	361
I/O, SGCK3 †, GCK4 ††	P51	P51	P70	P78	P86	T16	P100	N13	W19	364
GND	P52	P52	P71	P79	P87	GND*	P101	GND*	GND*	-
DONE	P53	P53	P72	P80	P88	U17	P103	P14	Y20	-
VCC	P54	P54	P73	P81	P89	VCC*	P106	VCC*	VCC*	-
$\overline{PROGRAM}$	P55	P55	P74	P82	P90	V18	P108	M12	V19	-
I/O (D7)	P56	P56	P75	P83	P91	T15	P109	P15	U19	367
I/O, PGCK3 †, GCK5 ††	P57	P57	P76	P84	P92	U16	P110	N14	U18	370

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/ HQ 208	BG 225†	BG 256††	Bndry Scan
I/O	-	-	P77	P85	P93	T14	P111	L11	T17	373
I/O	-	-	P78	P86	P94	U15	P112	M13	V20	376
I/O (D6)	P58	P58	P79	P87	P95	V17	P113	J10	T19	379
I/O	-	P59	P80	P88	P96	V16	P114	L12	T20	382
I/O	-	-	-	P89	P97	T13	P115	M15	R18	385
I/O	-	-	-	P90	P98	U14	P116	L13	R19	388
I/O	-	-	-	-	-	V15	P117	L14	R20	391
I/O	-	-	-	-	-	V14	P118	K11	P18	394
GND	-	-	P81	P91	P99	GND*	P119	GND*	GND*	-
I/O	-	-	P82	P92	P100	U13	P120	K13	N19	397
I/O	-	-	P83	P93	P101	V13	P121	K14	N20	400
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O (D5)	P59	P60	P84	P94	P102	U12	P122	K15	M17	403
I/O ($\overline{CS0}$)	P60	P61	P85	P95	P103	V12	P123	J12	M18	406
I/O	-	-	-	-	P104	T11	P124	J13	M20	409
I/O	-	-	-	-	P105	U11	P125	J14	L19	412
I/O	-	P62	P86	P96	P106	V11	P126	J15	L18	415
I/O	-	P63	P87	P97	P107	V10	P127	J11	L20	418
I/O (D4)	P61	P64	P88	P98	P108	U10	P128	H13	K20	421
I/O	P62	P65	P89	P99	P109	T10	P129	H14	K19	424
VCC	P63	P66	P90	P100	P110	VCC*	P130	VCC*	VCC*	-
GND	P64	P67	P91	P101	P111	GND*	P131	GND*	GND*	-
I/O (D3)	P65	P68	P92	P102	P112	T9	P132	H12	K18	427
I/O ($\overline{RS}$)	P66	P69	P93	P103	P113	U9	P133	H11	K17	430
I/O	-	P70	P94	P104	P114	V9	P134	G14	J20	433
I/O	-	-	P95	P105	P115	V8	P135	G15	J19	436
I/O	-	-	-	-	P116	U8	P136	G13	J18	439
I/O	-	-	-	-	P117	T8	P137	G12	J17	442
I/O (D2)	P67	P71	P96	P106	P118	V7	P138	G11	H19	445
I/O	P68	P72	P97	P107	P119	U7	P139	F15	H18	448
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	-	-	P98	P108	P120	V6	P140	F14	G19	451
I/O	-	-	P99	P109	P121	U6	P141	F13	F20	454
GND	-	-	P100	P110	P122	GND*	P142	GND*	GND*	-
I/O	-	-	-	-	-	V5	P143	E13	D20	457
I/O	-	-	-	-	-	V4	P144	D15	E18	460
I/O	-	-	-	P111	P123	U5	P145	F11	D19	463
I/O	-	-	-	P112	P124	T6	P146	D14	C20	466
I/O (D1)	P69	P73	P101	P113	P125	V3	P147	E12	E17	469
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P70	P74	P102	P114	P126	V2	P148	C15	D18	472
I/O	-	-	P103	P115	P127	U4	P149	D13	C19	475
I/O	-	-	P104	P116	P128	T5	P150	C14	B20	478
I/O (D0, DIN)	P71	P75	P105	P117	P129	U3	P151	F10	C18	481
I/O, SGCK4 †, GCK6 †† (DOUT)	P72	P76	P106	P118	P130	T4	P152	B15	B19	484
CCLK	P73	P77	P107	P119	P131	V1	P153	C13	A20	-
VCC	P74	P78	P108	P120	P132	VCC*	P154	VCC*	VCC*	-
O, TDO	P75	P79	P109	P121	P133	U2	P159	A15	A19	0
GND	P76	P80	P110	P122	P134	GND*	P160	GND*	GND*	-
I/O (A0, $\overline{WS}$)	P77	P81	P111	P123	P135	T3	P161	A14	B18	2
I/O, PGCK4 †, GCK7 †† (A1)	P78	P82	P112	P124	P136	U1	P162	B13	B17	5
I/O	-	-	P113	P125	P137	P3	P163	E11	C17	8
I/O	-	-	P114	P126	P138	R2	P164	C12	D16	11
I/O (CS1, A2)	P79	P83	P115	P127	P139	T2	P165	A13	A18	14
I/O (A3)	P80	P84	P116	P128	P140	N3	P166	B12	A17	17
I/O	-	-	P117	P129	P141	P2	P167	A12	A16	20
I/O	-	-	-	P130	P142	T1	P168	C11	C15	23
I/O	-	-	-	-	-	R1	P169	B11	B15	26
I/O	-	-	-	-	-	N2	P170	E10	A15	29
GND	-	-	P118	P131	P143	GND*	P171	GND*	GND*	-
I/O	-	-	P119	P132	P144	P1	P172	A11	B14	32
I/O	-	-	P120	P133	P145	N1	P173	D10	A14	35
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O (A4)	P81	P85	P121	P134	P146	M2	P174	A10	C12	38
I/O (A5)	P82	P86	P122	P135	P147	M1	P175	D9	B12	41
I/O	-	-	-	-	P148	L3	P176	C9	A12	44
I/O	-	-	-	P136	P149	L2	P177	B9	B11	47
I/O (A21)††	-	P87	P123	P137	P150	L1	P178	A9	C11	50
I/O (A20)††	-	P88	P124	P138	P151	K1	P179	E9	A11	53
I/O (A6)	P83	P89	P125	P139	P152	K2	P180	C8	A10	56
I/O (A7)	P84	P90	P126	P140	P153	K3	P181	B8	B10	59

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/ HQ 208	BG 225†	BG 256††	Bndry Scan
GND	P1	P91	P127	P141	P154	GND*	P182	GND*	GND*	-

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* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
† = E only
†† = XL only

Additional XC4010E/XL Package Pins

PQ/HQ208

N.C. Pins						
P1	P3	P51	P52	P53	P54	P102
P104	P105	P107	P155	P156	P157	P158
P206	P207	P208	-	-	-	-

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PG191

VCC Pins						
D3	D10	D16	J4	J15	R4	R10
R15	-	-	-	-	-	-
GND Pins						
C7	C12	D4	D9	D15	G3	G16
K4	K15	M3	M16	R3	R9	R16
T7	T12	-	-	-	-	-

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BG225

VCC Pins						
B2	B14	D8	H1	H15	R1	R8
R15	-	-	-	-	-	-
GND Pins						
A1	A8	D12	F8	G7	G8	G9
H2	H6	H7	H8	H9	H10	J7
J8	J9	K8	M8	-	-	-
N.C. Pins						
A3	B10	C4	C6	C10	D11	E2
E3	E14	E15	F1	F2	F7	F9
F12	G10	J5	K1	K4	K12	L2
L6	L15	M10	M14	N7	N11	N15
P5	P7	P10	R10	-	-	-

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BG256

VCC Pins						
C14	D6	D7	D11	D14	D15	E20
F1	F4	F17	G4	G17	K4	L17
P4	P17	P19	R2	R4	R17	U6
U7	U10	U14	U15	V7	W20	-
GND Pins						
A1	B7	D4	D8	D13	D17	G20
H4	H17	N3	N4	N17	U4	U8
U13	U17	W14	-	-	-	-
N.C. Pins						
A6	A7	A13	B13	B16	C4	C7
C8	C13	C16	D5	D12	E19	F2
F3	F18	F19	G18	H1	H2	H20
J3	J4	M4	M19	N1	N2	N18
P20	R3	T1	T18	U20	V9	V13
V15	W6	W9	W10	W13	W16	Y6
Y9	Y13	Y14	-	-	-	-

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Pin Locations for XC4013E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
VCC	P128	P142	P155	P183	VCC*	VCC*	P212	VCC*	-
I/O (A8)	P129	P143	P156	P184	J3	E8	P213	C10	74
I/O (A9)	P130	P144	P157	P185	J2	B7	P214	D10	77
I/O (A19) ††	P131	P145	P158	P186	J1	A7	P215	A9	80
I/O (A18) ††	P132	P146	P159	P187	H1	C7	P216	B9	83
I/O	-	-	P160	P188	H2	D7	P217	C9	86
I/O	-	-	P161	P189	H3	E7	P218	D9	89
I/O (A10)	P133	P147	P162	P190	G1	A8	P220	A8	92
I/O (A11)	P134	P148	P163	P191	G2	B6	P221	B8	95
VCC	-	-	-	-	VCC*	VCC*	P222	VCC*	-
I/O	-	-	-	-	H4	C6	P223	A6	98
I/O	-	-	-	-	G4	F7	P224	C7	101
I/O	P135	P149	P164	P192	F1	A5	P225	B6	104
I/O	P136	P150	P165	P193	E1	B5	P226	A5	107
GND	P137	P151	P166	P194	GND*	GND*	P227	GND*	-
I/O	-	-	-	P195	F2	D6	P228	C6	110
I/O	-	-	P167	P196	D1	C5	P229	B5	113
I/O	-	P152	P168	P197	C1	A4	P230	A4	116
I/O	-	P153	P169	P198	E2	E6	P231	C5	119
I/O (A12)	P138	P154	P170	P199	F3	B4	P232	B4	122
I/O (A13)	P139	P155	P171	P200	D2	D5	P233	A3	125
I/O	-	-	-	-	F4	A3	P234	D5	128
I/O	-	-	-	-	E4	C4	P235	C4	131
I/O	P140	P156	P172	P201	B1	B3	P236	B3	134
I/O	P141	P157	P173	P202	E3	F6	P237	B2	137

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
I/O (A14)	P142	P158	P174	P203	C2	A2	P238	A2	140
I/O, SGCK1 †, GCK8 †† (A15)	P143	P159	P175	P204	B2	C3	P239	C3	143
VCC	P144	P160	P176	P205	VCC*	VCC*	P240	VCC*	-
GND	P1	P1	P1	P2	GND*	GND*	P1	GND*	-
I/O, PGCK1 †, GCK1 †† (A16)	P2	P2	P2	P4	C3	D4	P2	B1	146
I/O (A17)	P3	P3	P3	P5	C4	B1	P3	C2	149
I/O	P4	P4	P4	P6	B3	C2	P4	D2	152
I/O	P5	P5	P5	P7	C5	E5	P5	D3	155
I/O, TDI	P6	P6	P6	P8	A2	D3	P6	E4	158
I/O, TCK	P7	P7	P7	P9	B4	C1	P7	C1	161
I/O	-	P8	P8	P10	C6	D2	P8	D1	164
I/O	-	P9	P9	P11	A3	G6	P9	E3	167
I/O	-	-	-	P12	B5	E4	P10	E2	170
I/O	-	-	-	P13	B6	D1	P11	E1	173
I/O	-	-	-	-	D5	E3	P12	F3	176
I/O	-	-	-	-	D6	E2	P13	F2	179
GND	P8	P10	P10	P14	GND*	GND*	P14	GND*	-
I/O	P9	P11	P11	P15	A4	F5	P15	G3	182
I/O	P10	P12	P12	P16	A5	E1	P16	G2	185
I/O, TMS	P11	P13	P13	P17	B7	F4	P17	G1	188
I/O	P12	P14	P14	P18	A6	F3	P18	H3	191

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
VCC	-	-	-	-	VCC*	VCC*	P19	VCC*	-
I/O	-	-	-	-	D7	F2	P20	H2	194
I/O	-	-	-	-	D8	F1	P21	H1	197
I/O	-	-	P15	P19	C8	G4	P23	J2	200
I/O	-	-	P16	P20	A7	G3	P24	J1	203
I/O	P13	P15	P17	P21	B8	G2	P25	K2	206
I/O	P14	P16	P18	P22	A8	G1	P26	K3	209
I/O	P15	P17	P19	P23	B9	G5	P27	K1	212
I/O	P16	P18	P20	P24	C9	H3	P28	L1	215
GND	P17	P19	P21	P25	GND*	GND*	P29	GND*	-
VCC	P18	P20	P22	P26	VCC*	VCC*	P30	VCC*	-
I/O	P19	P21	P23	P27	C10	H4	P31	L2	218
I/O	P20	P22	P24	P28	B10	H5	P32	L3	221
I/O	P21	P23	P25	P29	A9	J2	P33	L4	224
I/O	P22	P24	P26	P30	A10	J1	P34	M1	227
I/O	-	-	P27	P31	A11	J3	P35	M2	230
I/O	-	-	P28	P32	C11	J4	P36	M3	233
I/O	-	-	-	-	D11	J5	P38	N1	236
I/O	-	-	-	-	D12	K1	P39	N2	239
VCC	-	-	-	-	VCC*	VCC*	P40	VCC*	-
I/O	P23	P25	P29	P33	B11	K2	P41	P1	242
I/O	P24	P26	P30	P34	A12	K3	P42	P2	245
I/O	P25	P27	P31	P35	B12	J6	P43	R1	248
I/O	P26	P28	P32	P36	A13	L1	P44	P3	251
GND	P27	P29	P33	P37	GND*	GND*	P45	GND*	-
I/O	-	-	-	-	D13	L2	P46	T1	254
I/O	-	-	-	-	D14	K4	P47	R3	257
I/O	-	-	-	P38	B13	L3	P48	T2	260
I/O	-	-	-	P39	A14	M1	P49	U1	263
I/O	-	P30	P34	P40	A15	K5	P50	T3	266
I/O	-	P31	P35	P41	C13	M2	P51	U2	269
I/O	P28	P32	P36	P42	B14	L4	P52	V1	272
I/O	P29	P33	P37	P43	A16	N1	P53	T4	275
I/O	P30	P34	P38	P44	B15	M3	P54	U3	278
I/O	P31	P35	P39	P45	C14	N2	P55	V2	281
I/O	P32	P36	P40	P46	A17	K6	P56	W1	284
I/O, SGCK2 †, GCK2 ††	P33	P37	P41	P47	B16	P1	P57	V3	287
O (M1)	P34	P38	P42	P48	C15	N3	P58	W2	290
GND	P35	P39	P43	P49	GND*	GND*	P59	GND*	-
I (M0)	P36	P40	P44	P50	A18	P2	P60	Y1	293
VCC	P37	P41	P45	P55	VCC*	VCC*	P61	VCC*	-
I (M2)	P38	P42	P46	P56	C16	M4	P62	W3	294
I/O, PGCK2 †, GCK3 ††	P39	P43	P47	P57	B17	R2	P63	Y2	295
I/O (HDC)	P40	P44	P48	P58	E16	P3	P64	W4	298
I/O	P41	P45	P49	P59	C17	L5	P65	V4	301
I/O	P42	P46	P50	P60	D17	N4	P66	U5	304
I/O	P43	P47	P51	P61	B18	R3	P67	Y3	307
I/O (LDC)	P44	P48	P52	P62	E17	P4	P68	Y4	310
I/O	-	P49	P53	P63	F16	K7	P69	V5	313
I/O	-	P50	P54	P64	C18	M5	P70	W5	316
I/O	-	-	-	P65	D18	R4	P71	Y5	319
I/O	-	-	-	P66	F17	N5	P72	V6	322
I/O	-	-	-	-	E15	P5	P73	W6	325
I/O	-	-	-	-	F15	L6	P74	Y6	328
GND	P45	P51	P55	P67	GND*	GND*	P75	GND*	-
I/O	P46	P52	P56	P68	E18	R5	P76	W7	331
I/O	P47	P53	P57	P69	F18	M6	P77	Y7	334
I/O	P48	P54	P58	P70	G17	N6	P78	V8	337
I/O	P49	P55	P59	P71	G18	P6	P79	W8	340
VCC	-	-	-	-	VCC*	VCC*	P80	VCC*	-
I/O	-	-	P60	P72	H16	R6	P81	Y8	343
I/O	-	-	P61	P73	H17	M7	P82	U9	346
I/O	-	-	-	-	G15	N7	P84	Y9	349
I/O	-	-	-	-	H15	P7	P85	W10	352
I/O	P50	P56	P62	P74	H18	R7	P86	V10	355
I/O	P51	P57	P63	P75	J18	L7	P87	Y10	358
I/O	P52	P58	P64	P76	J17	N8	P88	Y11	361
I/O (INIT)	P53	P59	P65	P77	J16	P8	P89	W11	364
VCC	P54	P60	P66	P78	VCC*	VCC*	P90	VCC*	-
GND	P55	P61	P67	P79	GND*	GND*	P91	GND*	-

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
I/O	P56	P62	P68	P80	K16	L8	P92	V1	367
I/O	P57	P63	P69	P81	K17	P9	P93	U11	370
I/O	P58	P64	P70	P82	K18	R9	P94	Y12	373
I/O	P59	P65	P71	P83	L18	N9	P95	W12	376
I/O	-	-	P72	P84	L17	M9	P96	V12	379
I/O	-	-	P73	P85	L16	L9	P97	U12	382
I/O	-	-	-	-	L15	R10	P99	V13	385
I/O	-	-	-	-	M15	P10	P100	Y14	388
VCC	-	-	-	-	VCC*	VCC*	P101	VCC*	-
I/O	P60	P66	P74	P86	M18	N10	P102	Y15	391
I/O	P61	P67	P75	P87	M17	K9	P103	V14	394
I/O	P62	P68	P76	P88	N18	R11	P104	W15	397
I/O	P63	P69	P77	P89	P18	P11	P105	Y16	400
GND	P64	P70	P78	P90	GND*	GND*	P106	GND*	-
I/O	-	-	-	-	N15	M10	P107	V15	403
I/O	-	-	-	-	P15	N11	P108	W16	406
I/O	-	-	-	P91	N17	R12	P109	Y17	409
I/O	-	-	-	P92	R18	L10	P110	V16	412
I/O	-	P71	P79	P93	T18	P12	P111	W17	415
I/O	-	P72	P80	P94	P17	M11	P112	Y18	418
I/O	P65	P73	P81	P95	N16	R13	P113	U16	421
I/O	P66	P74	P82	P96	T17	N12	P114	V17	424
I/O	P67	P75	P83	P97	R17	P13	P115	W18	427
I/O	P68	P76	P84	P98	P16	K10	P116	Y19	430
I/O	P69	P77	P85	P99	U18	R14	P117	V18	433
I/O, SGCK3 †, GCK4 ††	P70	P78	P86	P100	T16	N13	P118	W19	436
GND	P71	P79	P87	P101	GND*	GND*	P119	GND*	-
DONE	P72	P80	P88	P103	U17	P14	P120	Y20	-
VCC	P73	P81	P89	P106	VCC*	VCC*	P121	VCC*	-
PROGRAM	P74	P82	P90	P108	V18	M12	P122	V19	-
I/O (D7)	P75	P83	P91	P109	T15	P15	P123	U19	439
I/O, PGCK3 †, GCK5 ††	P76	P84	P92	P110	U16	N14	P124	U18	442
I/O	P77	P85	P93	P111	T14	L11	P125	T17	445
I/O	P78	P86	P94	P112	U15	M13	P126	V20	448
I/O	-	-	-	-	R14	N15	P127	U20	451
I/O	-	-	-	-	R13	M14	P128	T18	454
I/O (D6)	P79	P87	P95	P113	V17	J10	P129	T19	457
I/O	P80	P88	P96	P114	V16	L12	P130	T20	460
I/O	-	P89	P97	P115	T13	M15	P131	R18	463
I/O	-	P90	P98	P116	U14	L13	P132	R19	466
I/O	-	-	-	P117	V15	L14	P133	R20	469
I/O	-	-	-	P118	V14	K11	P134	P18	472
GND	P81	P91	P99	P119	GND*	GND*	P135	GND*	-
I/O	-	-	-	-	R12	L15	P136	P20	475
I/O	-	-	-	-	R11	K12	P137	N18	478
I/O	P82	P92	P100	P120	U13	K13	P138	N19	481
I/O	P83	P93	P101	P121	V13	K14	P139	N20	484
VCC	-	-	-	-	VCC*	VCC*	P140	VCC*	-
I/O (D5)	P84	P94	P102	P122	U12	K15	P141	M17	487
I/O (CS0)	P85	P95	P103	P123	V12	J12	P142	M18	490
I/O	-	-	P104	P124	T11	J13	P144	M20	493
I/O	-	-	P105	P125	U11	J14	P145	L19	496
I/O	P86	P96	P106	P126	V11	J15	P146	L18	499
I/O	P87	P97	P107	P127	V10	J11	P147	L20	502
I/O (D4)	P88	P98	P108	P128	U10	H13	P148	K20	505
I/O	P89	P99	P109	P129	T10	H14	P149	K19	508
VCC	P90	P100	P110	P130	VCC*	VCC*	P150	VCC*	-
GND	P91	P101	P111	P131	GND*	GND*	P151	GND*	-
I/O (D3)	P92	P102	P112	P132	T9	H12	P152	K18	511
I/O (RS)	P93	P103	P113	P133	U9	H11	P153	K17	514
I/O	P94	P104	P114	P134	V9	G14	P154	J20	517
I/O	P95	P105	P115	P135	V8	G15	P155	J19	520
I/O	-	-	P116	P136	U8	G13	P156	J18	523
I/O	-	-	P117	P137	T8	G12	P157	J17	526
I/O (D2)	P96	P106	P118	P138	V7	G11	P159	H19	529
I/O	P97	P107	P119	P139	U7	F15	P160	H18	532
VCC	-	-	-	-	VCC*	VCC*	P161	VCC*	-
I/O	P98	P108	P120	P140	V6	F14	P162	G19	535
I/O	P99	P109	P121	P141	U6	F13	P163	F20	538

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
I/O	-	-	-	-	R8	G10	P164	G18	541
I/O	-	-	-	-	R7	E15	P165	F19	544
GND	P100	P110	P122	P142	GND*	GND*	P166	GND*	-
I/O	-	-	-	-	R6	E14	P167	F18	547
I/O	-	-	-	-	R5	F12	P168	E19	550
I/O	-	-	-	P143	V5	E13	P169	D20	553
I/O	-	-	-	P144	V4	D15	P170	E18	556
I/O	-	P111	P123	P145	U5	F11	P171	D19	559
I/O	-	P112	P124	P146	T6	D14	P172	C20	562
I/O (D1)	P101	P113	P125	P147	V3	E12	P173	E17	565
I/O (RCLK, RDY/ BUSY)	P102	P114	P126	P148	V2	C15	P174	D18	568
I/O	P103	P115	P127	P149	U4	D13	P175	C19	571
I/O	P104	P116	P128	P150	T5	C14	P176	B20	574
I/O (D0, DIN)	P105	P117	P129	P151	U3	F10	P177	C18	577
I/O, SGCK4 †, GCK6 †† (DOUT)	P106	P118	P130	P152	T4	B15	P178	B19	580
CCLK	P107	P119	P131	P153	V1	C13	P179	A20	-
VCC	P108	P120	P132	P154	VCC*	VCC*	P180	VCC*	-
O, TDO	P109	P121	P133	P159	U2	A15	P181	A19	0
GND	P110	P122	P134	P160	GND*	GND*	P182	GND*	-
I/O (A0, WS)	P111	P123	P135	P161	T3	A14	P183	B18	2
I/O, PGCK4 †, GCK7 †† (A1)	P112	P124	P136	P162	U1	B13	P184	B17	5
I/O	P113	P125	P137	P163	P3	E11	P185	C17	8
I/O	P114	P126	P138	P164	R2	C12	P186	D16	11
I/O (CS1, A2)	P115	P127	P139	P165	T2	A13	P187	A18	14
I/O (A3)	P116	P128	P140	P166	N3	B12	P188	A17	17
I/O	-	-	-	-	P4	F9	P189	C16	20
I/O	-	-	-	-	N4	D11	P190	B16	23
I/O	P117	P129	P141	P167	P2	A12	P191	A16	26
I/O	-	P130	P142	P168	T1	C11	P192	C15	29
I/O	-	-	-	P169	R1	B11	P193	B15	32
I/O	-	-	-	P170	N2	E10	P194	A15	35
GND	P118	P131	P143	P171	GND*	GND*	P196	GND*	-
I/O	P119	P132	P144	P172	P1	A11	P197	B14	38
I/O	P120	P133	P145	P173	N1	D10	P198	A14	41
I/O	-	-	-	-	M4	C10	P199	C13	44
I/O	-	-	-	-	L4	B10	P200	B13	47
VCC	-	-	-	-	VCC*	VCC*	P201	VCC*	-
I/O (A4)	P121	P134	P146	P174	M2	A10	P202	C12	50
I/O (A5)	P122	P135	P147	P175	M1	D9	P203	B12	53
I/O	-	-	P148	P176	L3	C9	P205	A12	56
I/O	-	P136	P149	P177	L2	B9	P206	B11	59
I/O (A21) ††	P123	P137	P150	P178	L1	A9	P207	C11	62
I/O (A20) ††	P124	P138	P151	P179	K1	E9	P208	A11	65
I/O (A6)	P125	P139	P152	P180	K2	C8	P209	A10	68
I/O (A7)	P126	P140	P153	P181	K3	B8	P210	B10	71
GND	P127	P141	P154	P182	GND*	GND*	P211	GND*	-

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* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

† = E only, †† = XL only

Additional XC4013E/XL Package Pins

PQ/HQ208

N.C. Pins					
P1	P3	P51	P52	P53	P54
P102	P104	P105	P107	P155	P156
P157	P158	P206	P207	P208	-

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PG223

VCC Pins					
D3	D10	D16	J4	J15	R4
R10	R15	-	-	-	-
GND Pins					
C7	C12	D4	D9	D15	G3
G16	K4	K15	M3	M16	R3
R9	R16	T7	T12	-	-

5/5/97

BG225

VCC Pins				
B2	B14	D8	H1	H15
R1	R8	R15	-	-
GND Pins				
A1	A8	D12	F8	G7
G8	G9	H2	H6	H7
H8	H9	H10	J7	J8
J9	K8	M8	-	-

5/5/97

The BG225 package pins in this table are bonded to an internal Ground plane on the XC4013E die. They must all be externally connected to Ground.

PQ/HQ240

GND Pins					
P22‡	P37‡	P83‡	P98‡	P143‡	P158‡
P204‡	P219‡	-	-	-	-
N.C. Pins					
P195	-	-	-	-	-

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‡ Pins marked with this symbol are used for Ground connections on some revisions of the device. These pins may not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
N.C. Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

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Pin Locations for XC4020E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4020E/XL Pad Name	HT 144††	PQ 160††	HT 176††	HQ208† PQ208††	PG 223†	HQ240† PQ240††	BG 256††	Bndry Scan
VCC	P128	P142	P155	P183	VCC*	P212	VCC*	-
I/O (A8)	P129	P143	P156	P184	J3	P213	C10	86
I/O (A9)	P130	P144	P157	P185	J2	P214	D10	89
I/O (A19) ††	P131	P145	P158	P186	J1	P215	A9	92
I/O (A18) ††	P132	P146	P159	P187	H1	P216	B9	95
I/O	-	-	P160	P188	H2	P217	C9	98
I/O	-	-	P161	P189	H3	P218	D9	101
I/O (A10)	P133	P147	P162	P190	G1	P220	A8	104
I/O (A11)	P134	P148	P163	P191	G2	P221	B8	107
I/O	-	-	-	-	-	-	C8	110
I/O	-	-	-	-	-	-	A7	113
VCC	-	-	-	-	VCC*	P222	VCC*	-
I/O	-	-	-	-	H4	P223	A6	116
I/O	-	-	-	-	G4	P224	C7	119
I/O	P135	P149	P164	P192	F1	P225	B6	122
I/O	P136	P150	P165	P193	E1	P226	A5	125
GND	P137	P151	P166	P194	GND*	P227	GND*	-
I/O	-	-	-	P195	F2	P228	C6	128
I/O	-	-	P167	P196	D1	P229	B5	131
I/O	-	P152	P168	P197	C1	P230	A4	134
I/O	-	P153	P169	P198	E2	P231	C5	137
I/O (A12)	P138	P154	P170	P199	F3	P232	B4	140
I/O (A13)	P139	P155	P171	P200	D2	P233	A3	143
I/O	-	-	-	-	F4	P234	D5	152
I/O	-	-	-	-	E4	P235	C4	155
I/O	P140	P156	P172	P201	B1	P236	B3	158
I/O	P141	P157	P173	P202	E3	P237	B2	161
I/O (A14)	P142	P158	P174	P203	C2	P238	A2	164
I/O, SGCK1 †, GCK8 †† (A15)	P143	P159	P175	P204	B2	P239	C3	167
VCC	P144	P160	P176	P205	VCC*	P240	VCC*	-
GND	P1	P1	P1	P2	GND*	P1	GND*	-
I/O, PGCK1 †, GCK1 †† (A16)	P2	P2	P2	P4	C3	P2	B1	170
I/O (A17)	P3	P3	P3	P5	C4	P3	C2	173
I/O	P4	P4	P4	P6	B3	P4	D2	176
I/O	P5	P5	P5	P7	C5	P5	D3	179
I/O, TDI	P6	P6	P6	P8	A2	P6	E4	182
I/O, TCK	P7	P7	P7	P9	B4	P7	C1	185
I/O	-	P8	P8	P10	C6	P8	D1	194
I/O	-	P9	P9	P11	A3	P9	E3	197
I/O	-	-	-	P12	B5	P10	E2	200
I/O	-	-	-	P13	B6	P11	E1	203
I/O	-	-	-	-	D5	P12	F3	206
I/O	-	-	-	-	D6	P13	F2	209
GND	P8	P10	P10	P14	GND*	P14	GND*	-
I/O	P9	P11	P11	P15	A4	P15	G3	212
I/O	P10	P12	P12	P16	A5	P16	G2	215
I/O, TMS	P11	P13	P13	P17	B7	P17	G1	218
I/O	P12	P14	P14	P18	A6	P18	H3	221
VCC	-	-	-	-	VCC*	P19	VCC*	-
I/O	-	-	-	-	D7	P20	H2	224
I/O	-	-	-	-	D8	P21	H1	227
I/O	-	-	-	-	-	-	J4	230
I/O	-	-	-	-	-	-	J3	233
I/O	-	-	P15	P19	C8	P23	J2	236
I/O	-	-	P16	P20	A7	P24	J1	239
I/O	P13	P15	P17	P21	B8	P25	K2	242
I/O	P14	P16	P18	P22	A8	P26	K3	245
I/O	P15	P17	P19	P23	B9	P27	K1	248
I/O	P16	P18	P20	P24	C9	P28	L1	251
GND	P17	P19	P21	P25	GND*	P29	GND*	-
VCC	P18	P20	P22	P26	VCC*	P30	VCC*	-
I/O	P19	P21	P23	P27	C10	P31	L2	254
I/O	P20	P22	P24	P28	B10	P32	L3	257
I/O	P21	P23	P25	P29	A9	P33	L4	260
I/O	P22	P24	P26	P30	A10	P34	M1	263
I/O	-	-	P27	P31	A11	P35	M2	266
I/O	-	-	P28	P32	C11	P36	M3	269
I/O	-	-	-	-	-	-	M4	272
I/O	-	-	-	-	D11	P38	N1	278
I/O	-	-	-	-	D12	P39	N2	281
VCC	-	-	-	-	VCC*	P40	VCC*	-
I/O	P23	P25	P29	P33	B11	P41	P1	284

XC4020E/XL Pad Name	HT 144††	PQ 160††	HT 176††	HQ208† PQ208††	PG 223†	HQ240† PQ240††	BG 256††	Bndry Scan
I/O	P24	P26	P30	P34	A12	P42	P2	287
I/O	P25	P27	P31	P35	B12	P43	R1	290
I/O	P26	P28	P32	P36	A13	P44	P3	293
GND	P27	P29	P33	P37	GND*	P45	GND*	-
I/O	-	-	-	-	D13	P46	T1	296
I/O	-	-	-	-	D14	P47	R3	299
I/O	-	-	-	P38	B13	P48	T2	302
I/O	-	-	-	P39	A14	P49	U1	305
I/O	-	P30	P34	P40	A15	P50	T3	308
I/O	-	P31	P35	P41	C13	P51	U2	311
I/O	P28	P32	P36	P42	B14	P52	V1	320
I/O	P29	P33	P37	P43	A16	P53	T4	323
I/O	P30	P34	P38	P44	B15	P54	U3	326
I/O	P31	P35	P39	P45	C14	P55	V2	329
I/O	P32	P36	P40	P46	A17	P56	W1	332
I/O, SCGK2 †, GCK2 ††	P33	P37	P41	P47	B16	P57	V3	335
O (M1)	P34	P38	P42	P48	C15	P58	W2	338
GND	P35	P39	P43	P49	GND*	P59	GND*	-
I (M0)	P36	P40	P44	P50	A18	P60	Y1	341
VCC	P37	P41	P45	P55	VCC*	P61	VCC*	-
I (M2)	P38	P42	P46	P56	C16	P62	W3	342
I/O PGCK2 †, GCK3 ††	P39	P43	P47	P57	B17	P63	Y2	343
I/O (HDC)	P40	P44	P48	P58	E16	P64	W4	346
I/O	P41	P45	P49	P59	C17	P65	V4	349
I/O	P42	P46	P50	P60	D17	P66	U5	352
I/O	P43	P47	P51	P61	B18	P67	Y3	355
I/O (LDC)	P44	P48	P52	P62	E17	P68	Y4	358
I/O	-	P49	P53	P63	F16	P69	V5	367
I/O	-	P50	P54	P64	C18	P70	W5	370
I/O	-	-	-	P65	D18	P71	Y5	373
I/O	-	-	-	P66	F17	P72	V6	376
I/O	-	-	-	-	E15	P73	W6	379
I/O	-	-	-	-	F15	P74	Y6	382
GND	P45	P51	P55	P67	GND*	P75	GND*	-
I/O	P46	P52	P56	P68	E18	P76	W7	385
I/O	P47	P53	P57	P69	F18	P77	Y7	388
I/O	P48	P54	P58	P70	G17	P78	V8	391
I/O	P49	P55	P59	P71	G18	P79	W8	394
VCC	-	-	-	-	VCC*	P80	VCC*	-
I/O	-	-	P60	P72	H16	P81	Y8	397
I/O	-	-	P61	P73	H17	P82	U9	400
I/O	-	-	-	-	-	-	V9	403
I/O	-	-	-	-	-	-	W9	406
I/O	-	-	-	-	G15	P84	Y9	409
I/O	-	-	-	-	H15	P85	W10	412
I/O	P50	P56	P62	P74	H18	P86	V10	415
I/O	P51	P57	P63	P75	J18	P87	Y10	418
I/O	P52	P58	P64	P76	J17	P88	Y11	421
I/O (INIT)	P53	P59	P65	P77	J16	P89	W11	424
VCC	P54	P60	P66	P78	VCC*	P90	VCC*	-
GND	P55	P61	P67	P79	GND*	P91	GND*	-
I/O	P56	P62	P68	P80	K16	P92	V11	427
I/O	P57	P63	P69	P81	K17	P93	U11	430
I/O	P58	P64	P70	P82	K18	P94	Y12	433
I/O	P59	P65	P71	P83	L18	P95	W12	436
I/O	-	-	P72	P84	L17	P96	V12	439
I/O	-	-	P73	P85	L16	P97	U12	442
I/O	-	-	-	-	-	-	Y13	445
I/O	-	-	-	-	-	-	W13	448
I/O	-	-	-	-	L15	P99	V13	451
I/O	-	-	-	-	M15	P100	Y14	454
VCC	-	-	-	-	VCC*	P101	VCC*	-
I/O	P60	P66	P74	P86	M18	P102	Y15	457
I/O	P61	P67	P75	P87	M17	P103	V14	460
I/O	P62	P68	P76	P88	N18	P104	W15	463
I/O	P63	P69	P77	P89	P18	P105	Y16	466
GND	P64	P70	P78	P90	GND*	P106	GND*	-
I/O	-	-	-	-	N15	P107	V15	469
I/O	-	-	-	-	P15	P108	W16	472
I/O	-	-	-	P91	N17	P109	Y17	475
I/O	-	-	-	P92	R18	P110	V16	478
I/O	-	P71	P79	P93	T18	P111	W17	481
I/O	-	P72	P80	P94	P17	P112	Y18	484

XC4020E/XL Pad Name	HT 144††	PQ 160††	HT 176††	HQ208† PQ208††	PG 223†	HQ240† PQ240††	BG 256††	Bndry Scan
I/O	P65	P73	P81	P95	N16	P113	U16	493
I/O	P66	P74	P82	P96	T17	P114	V17	496
I/O	P67	P75	P83	P97	R17	P115	W18	499
I/O	P68	P76	P84	P98	P16	P116	Y19	502
I/O	P69	P77	P85	P99	U18	P117	V18	505
I/O, SGCK3 †, GCK4 ††	P70	P78	P86	P100	T16	P118	W19	508
GND	P71	P79	P87	P101	GND*	P119	GND*	-
DONE	P72	P80	P88	P103	U17	P120	Y20	-
VCC	P73	P81	P89	P106	VCC*	P121	VCC*	-
PROGRAM	P74	P82	P90	P108	V18	P122	V19	-
I/O (D7)	P75	P83	P91	P109	T15	P123	U19	511
I/O, PGCK3 †, GCK5 ††	P76	P84	P92	P110	U16	P124	U18	514
I/O	P77	P85	P93	P111	T14	P125	T17	517
I/O	P78	P86	P94	P112	U15	P126	V20	520
I/O	-	-	-	-	R14	P127	U20	523
I/O	-	-	-	-	R13	P128	T18	526
I/O (D6)	P79	P87	P95	P113	V17	P129	T19	535
I/O	P80	P88	P96	P114	V16	P130	T20	538
I/O	-	P89	P97	P115	T13	P131	R18	541
I/O	-	P90	P98	P116	U14	P132	R19	544
I/O	-	-	-	P117	V15	P133	R20	547
I/O	-	-	-	P118	V14	P134	P18	550
GND	P81	P91	P99	P119	GND*	P135	GND*	-
I/O	-	-	-	-	R12	P136	P20	553
I/O	-	-	-	-	R11	P137	N18	556
I/O	P82	P92	P100	P120	U13	P138	N19	559
I/O	P83	P93	P101	P121	V13	P139	N20	562
VCC	-	-	-	-	VCC*	P140	VCC*	-
I/O (D5)	P84	P94	P102	P122	U12	P141	M17	565
I/O ($\overline{CS0}$)	P85	P95	P103	P123	V12	P142	M18	568
I/O	-	-	-	-	-	-	M19	574
I/O	-	-	P104	P124	T11	P144	M20	577
I/O	-	-	P105	P125	U11	P145	L19	580
I/O	P86	P96	P106	P126	V11	P146	L18	583
I/O	P87	P97	P107	P127	V10	P147	L20	586
I/O (D4)	P88	P98	P108	P128	U10	P148	K20	589
I/O	P89	P99	P109	P129	T10	P149	K19	592
VCC	P90	P100	P110	P130	VCC*	P150	VCC*	-
GND	P91	P101	P111	P131	GND*	P151	GND*	-
I/O (D3)	P92	P102	P112	P132	T9	P152	K18	595
I/O ($\overline{RS}$)	P93	P103	P113	P133	U9	P153	K17	598
I/O	P94	P104	P114	P134	V9	P154	J20	601
I/O	P95	P105	P115	P135	V8	P155	J19	604
I/O	-	-	P116	P136	U8	P156	J18	607
I/O	-	-	P117	P137	T8	P157	J17	610
I/O	-	-	-	-	-	-	H20	613
I/O (D2)	P96	P106	P118	P138	V7	P159	H19	619
I/O	P97	P107	P119	P139	U7	P160	H18	622
VCC	-	-		-	VCC*	P161	VCC*	-
I/O	P98	P108	P120	P140	V6	P162	G19	625
I/O	P99	P109	P121	P141	U6	P163	F20	628
I/O	-	-	-	-	R8	P164	G18	631
I/O	-	-	-	-	R7	P165	F19	634
GND	P100	P110	P122	P142	GND*	P166	GND*	-
I/O	-	-	-	-	R6	P167	F18	637
I/O	-	-	-	-	R5	P168	E19	640
I/O	-	-	-	P143	V5	P169	D20	643
I/O	-	-	-	P144	V4	P170	E18	646
I/O	-	P111	P123	P145	U5	P171	D19	649
I/O	-	P112	P124	P146	T6	P172	C20	652
I/O (D1)	P101	P113	P125	P147	V3	P173	E17	655
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P102	P114	P126	P148	V2	P174	D18	658
I/O	P103	P115	P127	P149	U4	P175	C19	667
I/O	P104	P116	P128	P150	T5	P176	B20	670
I/O (D0, DIN)	P105	P117	P129	P151	U3	P177	C18	673
I/O, SGCK4 †, GCK6 †† (DOUT)	P106	P118	P130	P152	T4	P178	B19	676
CCLK	P107	P119	P131	P153	V1	P179	A20	-
VCC	P108	P120	P132	P154	VCC*	P180	VCC*	-
O, TDO	P109	P121	P133	P159	U2	P181	A19	0
GND	P110	P122	P134	P160	GND*	P182	GND*	-
I/O (A0, $\overline{WS}$)	P111	P123	P135	P161	T3	P183	B18	2
I/O, PGCK4 †, GCK7 †† (A1)	P112	P124	P136	P162	U1	P184	B17	5
I/O	P113	P125	P137	P163	P3	P185	C17	8
I/O	P114	P126	P138	P164	R2	P186	D16	11
I/O (CS1, A2)	P115	P127	P139	P165	T2	P187	A18	14
I/O (A3)	P116	P128	P140	P166	N3	P188	A17	17
I/O	-	-	-	-	P4	P189	C16	26
I/O	-	-	-	-	N4	P190	B16	29
I/O	P117	P129	P141	P167	P2	P191	A16	32
I/O	-	P130	P142	P168	T1	P192	C15	35
I/O	-	-	-	P169	R1	P193	B15	38
I/O	-	-	-	P170	N2	P194	A15	41
GND	P118	P131	P143	P171	GND*	P196	GND*	-
I/O	P119	P132	P144	P172	P1	P197	B14	44
I/O	P120	P133	P145	P173	N1	P198	A14	47
I/O	-	-	-	-	M4	P199	C13	50
I/O	-	-	-	-	L4	P200	B13	53
VCC	-	-	-	-	VCC*	P201	VCC*	-
I/O	-	-	-	-	-	-	A13	56
I/O	-	-	-	-	-	-	D12	59
I/O (A4)	P121	P134	P146	P174	M2	P202	C12	62
I/O (A5)	P122	P135	P147	P175	M1	P203	B12	65
I/O	-	-	P148	P176	L3	P205	A12	68
I/O	-	P136	P149	P177	L2	P206	B11	71
I/O (A21) ††	P123	P137	P150	P178	L1	P207	C11	74
I/O (A20) ††	P124	P138	P151	P179	K1	P208	A11	77
I/O (A6)	P125	P139	P152	P180	K2	P209	A10	80
I/O (A7)	P126	P140	P153	P181	K3	P210	B10	83
GND	P127	P141	P154	P182	GND*	P211	GND*	-

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† = E only

†† = XL only

Additional XC4020E/XL Package Pins

PQ/HQ208

N.C. Pins					
P1	P3	P51	P52	P53	P54
P102	P104	P105	P107	P155	P156
P157	P158	P206	P207	P208	-

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PG223

VCC Pins					
D3	D10	D16	J4	J15	R4
R10	R15	-	-	-	-
GND Pins					
C7	C12	D4	D9	D15	G3
G16	K4	K15	M3	M16	R3
R9	R16	T7	T12	-	-

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PQ/HQ240

GND Pins					
P22‡	P37‡	P83‡	P98‡	P143‡	P158‡
P204‡	P219‡	-	-	-	-
N.C. Pins					
P195	-	-	-	-	-

6/9/97

‡ Pins marked with this symbol are used for Ground connections on some revisions of the device. These pins may not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

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Pin Locations for XC4025E, XC4028EX/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan
VCC	P142	P183	VCC*	P212	VCC*	VCC*	P38	VCC*	-
I/O (A8)	P143	P184	J3	P213	C10	K2	P37	D14	98
I/O (A9)	P144	P185	J2	P214	D10	K3	P36	C14	101
I/O (A19) ‡	P145	P186	J1	P215	A9	K5	P35	A15	104
I/O (A18) ‡	P146	P187	H1	P216	B9	K4	P34	B15	107
I/O	-	P188	H2	P217	C9	J1	P33	C15	110
I/O	-	P189	H3	P218	D9	J2	P32	D15	113
I/O (A10)	P147	P190	G1	P220	A8	H1	P31	A16	116
I/O (A11)	P148	P191	G2	P221	B8	J3	P30	B16	119
GND	-	-	-	-	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	J4	P29	C16	122
I/O	-	-	-	-	-	J5	P28	B17	125
I/O	-	-	-	-	C8	H2	P27	C17	128
I/O	-	-	-	-	A7	G1	P26	B18	131
VCC	-	-	VCC*	P222	VCC*	VCC*	P25	VCC*	-
I/O	-	-	H4	P223	A6	H3	P23	C18	134
I/O	-	-	G4	P224	C7	G2	P22	D17	137
I/O	P149	P192	F1	P225	B6	H4	P21	A20	140
I/O	P150	P193	E1	P226	A5	F2	P20	B19	143
GND	P151	P194	GND*	P227	GND*	GND*	P19	GND*	-
I/O	-	-	-	-	-	H5	P18	C19	146
I/O	-	-	-	-	-	G3	P17	D18	149
I/O	-	P195	F2	P228	C6	D1	P16	A21	152
I/O	-	P196	D1	P229	B5	G4	P15	B20	155
I/O	P152	P197	C1	P230	A4	E2	P14	C20	158
I/O	P153	P198	E2	P231	C5	F3	P13	B21	161
I/O (A12)	P154	P199	F3	P232	B4	G5	P12	B22	164
I/O (A13)	P155	P200	D2	P233	A3	C1	P10	C21	167
GND	-	-	-	-	GND*	GND*	-	GND*	-
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
I/O	-	-	-	-	-	F4	P9	D20	170
I/O	-	-	-	-	-	E3	P8	A23	173
I/O	-	-	F4	P234	D5	D2	P7	D21	176
I/O	-	-	E4	P235	C4	C2	P6	C22	179
I/O	P156	P201	B1	P236	B3	F5	P5	B24	182
I/O	P157	P202	E3	P237	B2	E4	P4	C23	185
I/O (A14)	P158	P203	C2	P238	A2	D3	P3	D22	188
I/O, SGCK1 †, GCK8 ‡ (A15)	P159	P204	B2	P239	C3	C3	P2	C24	191
VCC	P160	P205	VCC*	P240	VCC*	VCC*	P1	VCC*	-
GND	P1	P2	GND*	P1	GND*	GND*	P304	GND*	-
I/O, PGCK1 †, GCK1 ‡ (A16)	P2	P4	C3	P2	B1	D4	P303	D23	194
I/O (A17)	P3	P5	C4	P3	C2	B2	P302	C25	197
I/O	P4	P6	B3	P4	D2	B3	P301	D24	200
I/O	P5	P7	C5	P5	D3	E6	P300	E23	203
I/O, TDI	P6	P8	A2	P6	E4	D5	P299	C26	206
I/O, TCK	P7	P9	B4	P7	C1	C4	P298	E24	209
I/O	-	-	-	-	-	A3	P297	F24	212
I/O	-	-	-	-	-	D6	P296	E25	215
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
GND	-	-	-	-	GND*	GND*	-	GND*	-
I/O	P8	P10	C6	P8	D1	E7	P295	D26	218
I/O	P9	P11	A3	P9	E3	B4	P294	G24	221
I/O	-	P12	B5	P10	E2	C5	P293	F25	224
I/O	-	P13	B6	P11	E1	A4	P292	F26	227
I/O	-	-	D5	P12	F3	D7	P291	H23	230
I/O	-	-	D6	P13	F2	C6	P290	H24	233
I/O	-	-	-	-	-	E8	P289	G25	236

XC4025E, XC4026 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan
I/O	-	-	-	-	-	B5	P288	G26	239
GND	P10	P14	GND*	P14	GND*	GND*	P287	GND*	-
I/O	P11	P15	A4	P15	G3	B6	P286	J23	242
I/O	P12	P16	A5	P16	G2	D8	P285	J24	245
I/O, TMS	P13	P17	B7	P17	G1	C7	P284	H25	248
I/O	P14	P18	A6	P18	H3	B7	P283	K23	251
VCC	-	-	VCC*	P19	VCC*	VCC*	P282	VCC*	-
I/O	-	-	D7	P20	H2	C8	P280	K24	254
I/O	-	-	D8	P21	H1	E9	P279	J25	257
I/O	-	-	-	-	-	A7	P278	L24	260
I/O	-	-	-	-	-	D9	P277	K25	263
GND	-	-	-	P22	GND*	GND*	-	GND*	-
I/O	-	-	-	-	J4	B8	P276	L25	266
I/O	-	-	-	-	J3	A8	P275	L26	269
I/O	-	P19	C8	P23	J2	C9	P274	M23	272
I/O	-	P20	A7	P24	J1	B9	P273	M24	275
I/O	P15	P21	B8	P25	K2	E10	P272	M25	278
I/O	P16	P22	A8	P26	K3	A9	P271	M26	281
I/O	P17	P23	B9	P27	K1	D10	P270	N24	284
I/O	P18	P24	C9	P28	L1	C10	P269	N25	287
GND	P19	P25	GND*	P29	GND*	GND*	P268	GND*	-
VCC	P20	P26	VCC*	P30	VCC*	VCC*	P267	VCC*	-
I/O	P21	P27	C10	P31	L2	B10	P266	N26	290
I/O	P22	P28	B10	P32	L3	B11	P265	P25	293
I/O	P23	P29	A9	P33	L4	C11	P264	P23	296
I/O	P24	P30	A10	P34	M1	E11	P263	P24	299
I/O	-	P31	A11	P35	M2	D11	P262	R26	302
I/O	-	P32	C11	P36	M3	A12	P261	R25	305
I/O	-	-	-	-	M4	B12	P260	R24	308
I/O	-	-	-	-	-	A13	P259	R23	311
GND	-	-	-	P37	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	C12	P258	T26	314
I/O	-	-	-	-	-	D12	P257	T25	317
I/O	-	-	D11	P38	N1	E12	P256	T23	320
I/O	-	-	D12	P39	N2	B13	P255	V26	323
VCC	-	-	VCC*	P40	VCC*	VCC*	P253	VCC*	-
I/O	P25	P33	B11	P41	P1	A14	P252	U24	326
I/O	P26	P34	A12	P42	P2	C13	P251	V25	329
I/O	P27	P35	B12	P43	R1	B14	P250	V24	332
I/O	P28	P36	A13	P44	P3	D13	P249	U23	335
GND	P29	P37	GND*	P45	GND*	GND*	P248	GND*	-
I/O	-	-	-	-	-	B15	P247	Y26	338
I/O	-	-	-	-	-	E13	P246	W25	341
I/O	-	-	D13	P46	T1	C14	P245	W24	344
I/O	-	-	D14	P47	R3	A17	P244	V23	347
I/O	-	P38	B13	P48	T2	D14	P243	AA26	350
I/O	-	P39	A14	P49	U1	B16	P242	Y25	353
I/O	P30	P40	A15	P50	T3	C15	P241	Y24	356
I/O	P31	P41	C13	P51	U2	E14	P240	AA25	359
GND	-	-	-	-	GND*	GND*	-	GND*	-
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
I/O	-	-	-	-	-	A18	P239	AB25	362
I/O	-	-	-	-	-	D15	P238	AA24	365
I/O	P32	P42	B14	P52	V1	C16	P237	Y23	368
I/O	P33	P43	A16	P53	T4	B17	P236	AC26	371
I/O	P34	P44	B15	P54	U3	B18	P235	AA23	374
I/O	P35	P45	C14	P55	V2	E15	P234	AB24	377
I/O	P36	P46	A17	P56	W1	D16	P233	AD25	380
I/O, SGCK2 †, GCK2 ‡	P37	P47	B16	P57	V3	C17	P232	AC24	383
O (M1)	P38	P48	C15	P58	W2	A20	P231	AB23	386
GND	P39	P49	GND*	P59	GND*	GND*	P230	GND*	-

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan
I (M0)	P40	P50	A18	P60	Y1	C18	P229	AD24	389
VCC	P41	P55	VCC*	P61	VCC*	VCC*	P228	VCC*	-
I (M2)	P42	P56	C16	P62	W3	D17	P227	AC23	390
I/O, PGCK2 †, GCK3 ‡	P43	P57	B17	P63	Y2	B19	P226	AE24	391
I/O (HDC)	P44	P58	E16	P64	W4	C19	P225	AD23	394
I/O	P45	P59	C17	P65	V4	F16	P224	AC22	397
I/O	P46	P60	D17	P66	U5	E17	P223	AF24	400
I/O	P47	P61	B18	P67	Y3	D18	P222	AD22	403
I/O ($\overline{LDC}$)	P48	P62	E17	P68	Y4	C20	P221	AE23	406
I/O	-	-	-	-	-	F17	P220	AE22	409
I/O	-	-	-	-	-	G16	P219	AF23	412
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
GND	-	-	-	-	GND*	GND*	-	GND*	-
I/O	P49	P63	F16	P69	V5	D19	P218	AD20	415
I/O	P50	P64	C18	P70	W5	E18	P217	AE21	418
I/O	-	P65	D18	P71	Y5	D20	P216	AF21	421
I/O	-	P66	F17	P72	V6	G17	P215	AC19	424
I/O	-	-	E15	P73	W6	F18	P214	AD19	427
I/O	-	-	F15	P74	Y6	H16	P213	AE20	430
I/O	-	-	-	-	-	E19	P212	AF20	433
I/O	-	-	-	-	-	F19	P211	AC18	436
GND	P51	P67	GND*	P75	GND*	GND*	P210	GND*	-
I/O	P52	P68	E18	P76	W7	H17	P209	AD18	439
I/O	P53	P69	F18	P77	Y7	G18	P208	AE19	442
I/O	P54	P70	G17	P78	V8	G19	P207	AC17	445
I/O	P55	P71	G18	P79	W8	H18	P206	AD17	448
VCC	-	-	VCC*	P80	VCC*	VCC*	P204	VCC*	-
I/O	-	P72	H16	P81	Y8	J16	P203	AE18	451
I/O	-	P73	H17	P82	U9	G20	P202	AF18	454
I/O	-	-	-	-	-	J17	P201	AE17	457
I/O	-	-	-	-	-	H19	P200	AE16	460
GND	-	-	-	P83	GND*	GND*	-	GND*	-
I/O	-	-	-	-	V9	H20	P199	AF16	463
I/O	-	-	-	-	W9	J18	P198	AC15	466
I/O	-	-	G15	P84	Y9	J19	P197	AD15	469
I/O	-	-	H15	P85	W10	K16	P196	AE15	472
I/O	P56	P74	H18	P86	V10	J20	P195	AF15	475
I/O	P57	P75	J18	P87	Y10	K17	P194	AD14	478
I/O	P58	P76	J17	P88	Y11	K18	P193	AE14	481
I/O ($\overline{INIT}$)	P59	P77	J16	P89	W11	K19	P192	AF14	484
VCC	P60	P78	VCC*	P90	VCC*	VCC*	P191	VCC*	-
GND	P61	P79	GND*	P91	GND*	GND*	P190	GND*	-
I/O	P62	P80	K16	P92	V11	L19	P189	AE13	487
I/O	P63	P81	K17	P93	U11	L18	P188	AC13	490
I/O	P64	P82	K18	P94	Y12	L16	P187	AD13	493
I/O	P65	P83	L18	P95	W12	L17	P186	AF12	496
I/O	-	P84	L17	P96	V12	M20	P185	AE12	499
I/O	-	P85	L16	P97	U12	M19	P184	AD12	502
I/O	-	-	-	-	Y13	N20	P183	AC12	505
I/O	-	-	-	-	W13	M18	P182	AF11	508
GND	-	-	-	P98	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	M17	P181	AE11	511
I/O	-	-	-	-	-	M16	P180	AD11	514
I/O	-	-	L15	P99	V13	N19	P179	AF9	517
I/O	-	-	M15	P100	Y14	P20	P178	AD10	520
VCC	-	-	VCC*	P101	VCC*	VCC*	P177	VCC*	-
I/O	P66	P86	M18	P102	Y15	N18	P175	AE9	523
I/O	P67	P87	M17	P103	V14	P19	P174	AD9	526
I/O	P68	P88	N18	P104	W15	N17	P173	AC10	529
I/O	P69	P89	P18	P105	Y16	R19	P172	AF7	532
GND	P70	P90	GND*	P106	GND*	GND*	P171	GND*	-
I/O	-	-	-	-	-	N16	P170	AE8	535
I/O	-	-	-	-	-	P18	P169	AD8	538
I/O	-	-	N15	P107	V15	U20	P168	AC9	541
I/O	-	-	P15	P108	W16	P17	P167	AF6	544
I/O	-	P91	N17	P109	Y17	T19	P166	AE7	547

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan
I/O	-	P92	R18	P110	V16	R18	P165	AD7	550
I/O	P71	P93	T18	P111	W17	P16	P164	AE6	553
I/O	P72	P94	P17	P112	Y18	V20	P163	AE5	556
GND	-	-	-	-	GND*	GND*	-	GND*	-
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
I/O	-	-	-	-	-	R17	P162	AD6	559
I/O	-	-	-	-	-	T18	P161	AC7	562
I/O	P73	P95	N16	P113	U16	U19	P160	AF4	565
I/O	P74	P96	T17	P114	V17	V19	P159	AF3	568
I/O	P75	P97	R17	P115	W18	R16	P158	AD5	571
I/O	P76	P98	P16	P116	Y19	T17	P157	AE3	574
I/O	P77	P99	U18	P117	V18	U18	P156	AD4	577
I/O, SGCK3 †, GCK4 ‡	P78	P100	T16	P118	W19	X20	P155	AC5	580
GND	P79	P101	GND*	P119	GND*	GND*	P154	GND*	-
DONE	P80	P103	U17	P120	Y20	V18	P153	AD3	-
VCC	P81	P106	VCC*	P121	VCC*	VCC*	P152	VCC*	-
$\overline{PRO-GRAM}$	P82	P108	V18	P122	V19	U17	P151	AC4	-
I/O (D7)	P83	P109	T15	P123	U19	W19	P150	AD2	583
I/O, PGCK3 †, GCK5 ‡	P84	P110	U16	P124	U18	W18	P149	AC3	586
I/O	P85	P111	T14	P125	T17	T15	P148	AB4	589
I/O	P86	P112	U15	P126	V20	U16	P147	AD1	592
I/O	-	-	R14	P127	U20	V17	P146	AA4	595
I/O	-	-	R13	P128	T18	X18	P145	AA3	598
I/O	-	-	-	-	-	U15	P144	AB2	601
I/O	-	-	-	-	-	T14	P143	AC1	604
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
GND	-	-	-	-	GND*	GND*	-	GND*	-
I/O (D6)	P87	P113	V17	P129	T19	W17	P142	Y3	607
I/O	P88	P114	V16	P130	T20	V16	P141	AA2	610
I/O	P89	P115	T13	P131	R18	X17	P140	AA1	613
I/O	P90	P116	U14	P132	R19	U14	P139	W4	616
I/O	-	P117	V15	P133	R20	V15	P138	W3	619
I/O	-	P118	V14	P134	P18	T13	P137	Y2	622
I/O	-	-	-	-	-	W16	P136	Y1	625
I/O	-	-	-	-	-	W15	P135	V4	628
GND	P91	P119	GND*	P135	GND*	GND*	P134	GND*	-
I/O	-	-	R12	P136	P20	U13	P133	V3	631
I/O	-	-	R11	P137	N18	V14	P132	W2	634
I/O	P92	P120	U13	P138	N19	W14	P131	U4	637
I/O	P93	P121	V13	P139	N20	V13	P130	U3	640
VCC	-	-	VCC*	P140	VCC*	VCC*	P129	VCC*	-
I/O (D5)	P94	P122	U12	P141	M17	T12	P127	V2	643
I/O ($\overline{CS0}$)	P95	P123	V12	P142	M18	X14	P126	V1	646
I/O	-	-	-	-	-	U12	P125	U2	649
I/O	-	-	-	-	-	W13	P124	T2	652
GND	-	-	-	P143	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	X13	P123	T1	655
I/O	-	-	-	-	M19	V12	P122	R4	658
I/O	-	P124	T11	P144	M20	W12	P121	R3	661
I/O	-	P125	U11	P145	L19	T11	P120	R2	664
I/O	P96	P126	V11	P146	L18	X12	P119	R1	667
I/O	P97	P127	V10	P147	L20	U11	P118	P3	670
I/O (D4)	P98	P128	U10	P148	K20	V11	P117	P2	673
I/O	P99	P129	T10	P149	K19	W11	P116	P1	676
VCC	P100	P130	VCC*	P150	VCC*	VCC*	P115	VCC*	-
GND	P101	P131	GND*	P151	GND*	GND*	P114	GND*	-
I/O (D3)	P102	P132	T9	P152	K18	W10	P113	N2	679
I/O ($\overline{RS}$)	P103	P133	U9	P153	K17	V10	P112	N4	682
I/O	P104	P134	V9	P154	J20	T10	P111	N3	685
I/O	P105	P135	V8	P155	J19	U10	P110	M1	688
I/O	-	P136	U8	P156	J18	X9	P109	M2	691
I/O	-	P137	T8	P157	J17	W9	P108	M3	694
I/O	-	-	-	-	H20	X8	P107	M4	697

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan
I/O	-	-	-	-	-	V9	P106	L1	700
GND	-	-	-	P158	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	U9	P105	L2	703
I/O	-	-	-	-	-	T9	P104	L3	706
I/O (D2)	P106	P138	V7	P159	H19	W8	P103	J1	709
I/O	P107	P139	U7	P160	H18	X7	P102	K3	712
VCC	-	-	VCC*	P161	VCC*	VCC*	P101	VCC*	-
I/O	P108	P140	V6	P162	G19	V8	P99	J2	715
I/O	P109	P141	U6	P163	F20	W7	P98	J3	718
I/O	-	-	R8	P164	G18	U8	P97	K4	721
I/O	-	-	R7	P165	F19	W6	P96	G1	724
GND	P110	P142	GND*	P166	GND*	GND*	P95	GND*	-
I/O	-	-	-	-	-	T8	P94	H2	727
I/O	-	-	-	-	-	V7	P93	H3	730
I/O	-	-	R6	P167	F18	X4	P92	J4	733
I/O	-	-	R5	P168	E19	U7	P91	F1	736
I/O	-	P143	V5	P169	D20	W5	P90	G2	739
I/O	-	P144	V4	P170	E18	V6	P89	G3	742
I/O	P111	P145	U5	P171	D19	T7	P88	F2	745
I/O	P112	P146	T6	P172	C20	X3	P87	E2	748
GND	-	-	-	-	GND*	GND*	-	GND*	-
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
I/O (D1)	P113	P147	V3	P173	E17	U6	P86	F3	751
I/O (RCLK, RDY/ BUSY)	P114	P148	V2	P174	D18	V5	P85	G4	754
I/O	-	-	-	-	-	W4	P84	D2	757
I/O	-	-	-	-	-	W3	P83	F4	760
I/O	P115	P149	U4	P175	C19	T6	P82	E3	763
I/O	P116	P150	T5	P176	B20	U5	P81	C2	766
I/O (D0, DIN)	P117	P151	U3	P177	C18	V4	P80	D3	769
I/O, SGCK4 †, GCK6 ‡ (DOUT)	P118	P152	T4	P178	B19	X1	P79	E4	772
CCLK	P119	P153	V1	P179	A20	V3	P78	C3	-
VCC	P120	P154	VCC*	P180	VCC*	VCC*	P77	VCC*	-
O, TDO	P121	P159	U2	P181	A19	U4	P76	D4	0
GND	P122	P160	GND*	P182	GND*	GND*	P75	GND*	-
I/O (A0, WS)	P123	P161	T3	P183	B18	W2	P74	B3	2
I/O, PGCK4 †, GCK7 ‡ (A1)	P124	P162	U1	P184	B17	V2	P73	C4	5
I/O	P125	P163	P3	P185	C17	R5	P72	D5	8
I/O	P126	P164	R2	P186	D16	T4	P71	A3	11
I/O (CS1, A2)	P127	P165	T2	P187	A18	U3	P70	D6	14
I/O (A3)	P128	P166	N3	P188	A17	V1	P69	C6	17
I/O	-	-	-	-	-	R4	P68	B5	20
I/O	-	-	-	-	-	P5	P67	A4	23
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
GND	-	-	-	-	GND*	GND*	-	GND*	-
I/O	-	-	P4	P189	C16	U2	P66	C7	26
I/O	-	-	N4	P190	B16	T3	P65	B6	29
I/O	P129	P167	P2	P191	A16	U1	P64	A6	32
I/O	P130	P168	T1	P192	C15	P4	P63	D8	35
I/O	-	P169	R1	P193	B15	R3	P62	B7	38
I/O	-	P170	N2	P194	A15	N5	P61	A7	41
I/O	-	-	-	P195	-	T2	P60	D9	44
I/O	-	-	-	-	-	R2	P59	C9	47
GND	P131	P171	GND*	P196	GND*	GND*	P58	GND*	-
I/O	P132	P172	P1	P197	B14	N4	P57	B8	50
I/O	P133	P173	N1	P198	A14	P3	P56	D10	53
I/O	-	-	M4	P199	C13	P2	P55	C10	56
I/O	-	-	L4	P200	B13	N3	P54	B9	59
VCC	-	-	VCC*	P201	VCC*	VCC*	P52	VCC*	-

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan
I/O	-	-	-	-	A13	M5	P51	A9	62
I/O	-	-	-	-	D12	P1	P50	D11	65
I/O	-	-	-	-	-	M4	P49	B11	68
I/O	-	-	-	-	-	N2	P48	A11	71
GND	-	-	-	-	GND*	GND*	-	GND*	-
I/O (A4)	P134	P174	M2	P202	C12	N1	P47	D12	74
I/O (A5)	P135	P175	M1	P203	B12	M3	P46	C12	77
I/O	-	P176	L3	P205	A12	M2	P45	B12	80
I/O	P136	P177	L2	P206	B11	L5	P44	A12	83
I/O (A21) ‡	P137	P178	L1	P207	C11	M1	P43	C13	86
I/O (A20) ‡	P138	P179	K1	P208	A11	L4	P42	B13	89
I/O (A6)	P139	P180	K2	P209	A10	L3	P41	A13	92
I/O (A7)	P140	P181	K3	P210	B10	L2	P40	B14	95
GND	P141	P182	GND*	P211	GND*	GND*	P39	GND*	-

6/19/97

* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

† = E only
†† = XL only
‡ = EX, XL only

Additional XC4025E, XC4028EX/XL Package Pins

HQ208

N.C. Pins					
P1	P52	P102	P107	P157	P207
P3	P53	P104	P155	P158	P208
P51	P54	P105	P156	P206	

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PG223

VCC Pins			
D3	D10	D16	J4
J15	R4	R10	R15
GND Pins			
C7	C12	D4	D9
D15	G3	G16	K4
K15	M3	M16	R3
R9	R16	T7	T12

5/9/97

HQ240

GND Pins	
P204	P219

5/9/97

Note: These pins may be N.C. for this device revision, however for compatability with other devices in this package, these pins should be tied to GND.

BG256

VCC Pins			
C14	D6	D7	D11
D14	D15	E20	F1
F4	F17	G4	G17
K4	L17	P4	P17
P19	R2	R4	R17
U6	U7	U10	U14
U15	V7	W20	-
GND Pins			
A1	B7	D4	D8
D13	D17	G20	H4
H17	N3	N4	N17
U4	U8	U13	U17
W14	-	-	-

5/9/97

PG299

VCC Pins			
A2	A6	A11	A16
B20	E1	E5	F20
K1	L20	R1	T16
T20	W1	X5	X10
X15	X19	-	-
GND Pins			
A5	A10	A15	A19
B1	E16	E20	F1
K20	L1	R20	T1
T5	W20	X2	X6
X11	X16	-	-

6/18/97

HQ304

N.C. Pins				
P11	P53	P128	P205	P281
P24	P100	P176	P254	-

5/15/97

Note: In XC4025 (no extension) devices in the HQ304 package, P101 is a No Connect (N.C.) pin. P101 is Vcc in XC4025E and XC4028EX/XL devices. Where necessary for compatibility, this pin can be left unconnected.

BG352

VCC Pins					
A10	A17	B2	B25	D7	D13
D19	G23	H4	K1	K26	N23
P4	U1	U26	W23	Y4	AC8
AC14	AC20	AE2	AE25	AF10	AF17
GND Pins					
A1	A2	A5	A8	A14	A19
A22	A25	A26	B1	B26	E1
E26	H1	H26	N1	P26	W1
W26	AB1	AB26	AE1	AE26	AF1
AF2	AF5	AF8	AF13	AF19	AF22
AF25	AF26	-	-	-	-
N.C. Pins					
A18	A24	B4	B10	B23	C1
C5	C8	C11	D1	D16	D25
F23	J26	K2	L4	L23	T3
T4	T24	U25	AB3	AC2	AC6
AC11	AC16	AC21	AC25	AD16	AD21
AD26	AE4	AE10	-	-	-

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Pin Locations for XC4036EX/XL

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
VCC	P142	P183	P212	P38	VCC*	VCC*	VCC*	-
I/O (A8)	P143	P184	P213	P37	D14	W3	D17	110
I/O (A9)	P144	P185	P214	P36	C14	Y2	A17	113
I/O (A19)	P145	P186	P215	P35	A15	V4	C18	116
I/O (A18)	P146	P187	P216	P34	B15	T2	D18	119
I/O	-	P188	P217	P33	C15	U1	B18	122
I/O	-	P189	P218	P32	D15	V6	A19	125
I/O (A10)	P147	P190	P220	P31	A16	U3	B19	128
I/O (A11)	P148	P191	P221	P30	B16	R1	C19	131
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O	-	-	-	P29	C16	U5	D19	134
I/O	-	-	-	P28	B17	T4	A20	137
I/O	-	-	-	-	D16	P2	B20	140
I/O	-	-	-	-	A18	N1	C20	143
I/O	-	-	-	P27	C17	R5	C21	146
I/O	-	-	-	P26	B18	M2	A22	149
VCC	-	-	P222	P25	VCC*	VCC*	VCC*	-
I/O	-	-	P223	P23	C18	L3	B22	152
I/O	-	-	P224	P22	D17	T6	C22	155
I/O	P149	P192	P225	P21	A20	N5	B23	158
I/O	P150	P193	P226	P20	B19	M4	A24	161
GND	P151	P194	P227	P19	GND*	GND*	GND*	-
I/O	-	-	-	P18	C19	K2	D22	164
I/O	-	-	-	P17	D18	K4	C23	167
I/O	-	P195	P228	P16	A21	P6	B24	170
I/O	-	P196	P229	P15	B20	M6	C24	173
I/O	P152	P197	P230	P14	C20	J3	A26	176
I/O	P153	P198	P231	P13	B21	H2	C25	179
I/O (A12)	P154	P199	P232	P12	B22	H4	D24	182

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I/O (A13)	P155	P200	P233	P10	C21	G3	B26	185
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P9	D20	K6	A27	188
I/O	-	-	-	P8	A23	G1	D25	191
I/O	-	-	-	-	A24	E1	C26	194
I/O	-	-	-	-	B23	E3	B27	197
I/O	-	-	P234	P7	D21	J7	C27	200
I/O	-	-	P235	P6	C22	H6	B28	203
I/O	P156	P201	P236	P5	B24	C3	D27	206
I/O	P157	P202	P237	P4	C23	D2	B29	209
I/O (A14)	P158	P203	P238	P3	D22	E5	C28	212
I/O, GCK8 (A15)	P159	P204	P239	P2	C24	G7	D28	215
VCC	P160	P205	P240	P1	VCC*	VCC*	VCC*	-
GND	P1	P2	P1	P304	GND*	GND*	GND*	-
I/O, GCK1 (A16)	P2	P4	P2	P303	D23	H8	D29	218
I/O (A17)	P3	P5	P3	P302	C25	F6	C30	221
I/O	P4	P6	P4	P301	D24	B4	E28	224
I/O	P5	P7	P5	P300	E23	D4	E29	227
I/O, TDI	P6	P8	P6	P299	C26	B2	D30	230
I/O, TCK	P7	P9	P7	P298	E24	G9	D31	233
I/O	-	-	-	-	D25	F8	E30	236
I/O	-	-	-	-	F23	C5	E31	239
I/O	-	-	-	P297	F24	A7	G28	242
I/O	-	-	-	P296	E25	A5	G29	245
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O	P8	P10	P8	P295	D26	B8	H28	248
I/O	P9	P11	P9	P294	G24	C9	H29	251
I/O	-	P12	P10	P293	F25	E9	G30	254

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I/O	-	P13	P11	P292	F26	F12	H30	257
I/O	-	-	P12	P291	H23	D10	J28	260
I/O	-	-	P13	P290	H24	B10	J29	263
I/O	-	-	-	P289	G25	F10	H31	266
I/O	-	-	-	P288	G26	F14	J30	269
GND	P10	P14	P14	P287	GND*	GND*	GND*	-
I/O	P11	P15	P15	P286	J23	C11	K28	272
I/O	P12	P16	P16	P285	J24	B12	K29	275
I/O, TMS	P13	P17	P17	P284	H25	E11	K30	278
I/O	P14	P18	P18	P283	K23	E15	K31	281
VCC	-	-	P19	P282	VCC*	VCC*	VCC*	-
I/O	-	-	P20	P280	K24	F16	L29	284
I/O	-	-	P21	P279	J25	C13	L30	287
I/O	-	-	-	-	J26	B14	M29	290
I/O	-	-	-	-	L23	E17	M31	293
I/O	-	-	-	P278	L24	E13	N31	296
I/O	-	-	-	P277	K25	A15	N28	299
GND	-	-	P22	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P276	L25	B16	P30	302
I/O	-	-	-	P275	L26	D16	P28	305
I/O	-	P19	P23	P274	M23	D18	P29	308
I/O	-	P20	P24	P273	M24	A17	R31	311
I/O	P15	P21	P25	P272	M25	E19	R30	314
I/O	P16	P22	P26	P271	M26	B18	R28	317
I/O	P17	P23	P27	P270	N24	C17	R29	320
I/O	P18	P24	P28	P269	N25	C19	T31	323
GND	P19	P25	P29	P268	GND*	GND*	GND*	-
VCC	P20	P26	P30	P267	VCC*	VCC*	VCC*	-
I/O	P21	P27	P31	P266	N26	F20	T30	326
I/O	P22	P28	P32	P265	P25	B20	T29	329
I/O	P23	P29	P33	P264	P23	C21	U31	332
I/O	P24	P30	P34	P263	P24	B22	U30	335
I/O	-	P31	P35	P262	R26	E21	U28	338
I/O	-	P32	P36	P261	R25	D22	U29	341
I/O	-	-	-	P260	R24	A23	V30	344
I/O	-	-	-	P259	R23	B24	V29	347
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	P37	-	GND*	GND*	GND*	-
I/O	-	-	-	P258	T26	A25	W30	350
I/O	-	-	-	P257	T25	D24	W29	353
I/O	-	-	-	-	T24	B26	Y30	356
I/O	-	-	-	-	U25	A27	Y29	359
I/O	-	-	P38	P256	T23	C27	Y28	362
I/O	-	-	P39	P255	V26	F24	AA30	365
VCC	-	-	P40	P253	VCC*	VCC*	VCC*	-
I/O	P25	P33	P41	P252	U24	E25	AA29	368
I/O	P26	P34	P42	P251	V25	E27	AB31	371
I/O	P27	P35	P43	P250	V24	B28	AB30	374
I/O	P28	P36	P44	P249	U23	C29	AB29	377
GND	P29	P37	P45	P248	GND*	GND*	GND*	-
I/O	-	-	-	P247	Y26	F26	AB28	380
I/O	-	-	-	P246	W25	D28	AC30	383
I/O	-	-	P46	P245	W24	B30	AC29	386
I/O	-	-	P47	P244	V23	E29	AC28	389
I/O	-	P38	P48	P243	AA26	F28	AD29	392
I/O	-	P39	P49	P242	Y25	F30	AD28	395
I/O	P30	P40	P50	P241	Y24	C31	AE30	398
I/O	P31	P41	P51	P240	AA25	E31	AE29	401
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P239	AB25	B32	AF31	404
I/O	-	-	-	P238	AA24	A33	AE28	407
I/O	P32	P42	P52	P237	Y23	A35	AG31	410
I/O	P33	P43	P53	P236	AC26	F32	AF28	413
I/O	-	-	-	-	AD26	C35	AG30	416
I/O	-	-	-	-	AC25	B38	AG29	419
I/O	P34	P44	P54	P235	AA23	E33	AH31	422
I/O	P35	P45	P55	P234	AB24	G31	AG28	425
I/O	P36	P46	P56	P233	AD25	H32	AH30	428
I/O, GCK2	P37	P47	P57	P232	AC24	B36	AJ30	431
O (M1)	P38	P48	P58	P231	AB23	A39	AH29	434
GND	P39	P49	P59	P230	GND*	GND*	GND*	-
I (M0)	P40	P50	P60	P229	AD24	E35	AH28	437
VCC	P41	P55	P61	P228	VCC*	VCC*	VCC*	-

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I (M2)	P42	P56	P62	P227	AC23	G33	AJ28	438
I/O, GCK3	P43	P57	P63	P226	AE24	D36	AK29	439
I/O (HDC)	P44	P58	P64	P225	AD23	C37	AH27	442
I/O	P45	P59	P65	P224	AC22	F34	AK28	445
I/O	P46	P60	P66	P223	AF24	J33	AJ27	448
I/O	P47	P61	P67	P222	AD22	D38	AL28	451
I/O (LDC)	P48	P62	P68	P221	AE23	G35	AH26	454
I/O	-	-	-	-	AC21	E39	AL27	457
I/O	-	-	-	-	AD21	K34	AH25	460
I/O	-	-	-	P220	AE22	F38	AK26	463
I/O	-	-	-	P219	AF23	G37	AL26	466
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O	P49	P63	P69	P218	AD20	H38	AH24	469
I/O	P50	P64	P70	P217	AE21	J37	AJ25	472
I/O	-	P65	P71	P216	AF21	G39	AK25	475
I/O	-	P66	P72	P215	AC19	M34	AJ24	478
I/O	-	-	P73	P214	AD19	N35	AL24	481
I/O	-	-	P74	P213	AE20	P34	AH22	484
I/O	-	-	-	P212	AF20	J35	AJ23	487
I/O	-	-	-	P211	AC18	L37	AK23	490
GND	P51	P67	P75	P210	GND*	GND*	GND*	-
I/O	P52	P68	P76	P209	AD18	M38	AJ22	493
I/O	P53	P69	P77	P208	AE19	R35	AK22	496
I/O	P54	P70	P78	P207	AC17	H36	AL22	499
I/O	P55	P71	P79	P206	AD17	T34	AJ21	502
VCC	-	-	P80	P204	VCC*	VCC*	VCC*	-
I/O	-	P72	P81	P203	AE18	N37	AH20	505
I/O	-	P73	P82	P202	AF18	N39	AK21	508
I/O	-	-	-	-	AC16	U35	AK20	511
I/O	-	-	-	-	AD16	R39	AJ19	514
I/O	-	-	-	P201	AE17	M36	AL20	517
I/O	-	-	-	P200	AE16	V34	AH18	520
GND	-	-	P83	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P199	AF16	R37	AK19	523
I/O	-	-	-	P198	AC15	T38	AJ18	526
I/O	-	-	P84	P197	AD15	T36	AL19	529
I/O	-	-	P85	P196	AE15	V36	AK18	532
I/O	P56	P74	P86	P195	AF15	U37	AH17	535
I/O	P57	P75	P87	P194	AD14	U39	AJ17	538
I/O	P58	P76	P88	P193	AE14	V38	AJ16	541
I/O (INIT)	P59	P77	P89	P192	AF14	W37	AK16	544
VCC	P60	P78	P90	P191	VCC*	VCC*	VCC*	-
GND	P61	P79	P91	P190	GND*	GND*	GND*	-
I/O	P62	P80	P92	P189	AE13	Y34	AL16	547
I/O	P63	P81	P93	P188	AC13	AC37	AH15	550
I/O	P64	P82	P94	P187	AD13	AB38	AK15	553
I/O	P65	P83	P95	P186	AF12	AD36	AJ14	556
I/O	-	P84	P96	P185	AE12	AA35	AH14	559
I/O	-	P85	P97	P184	AD12	AE37	AK14	562
I/O	-	-	-	P183	AC12	AB36	AL13	565
I/O	-	-	-	P182	AF11	AD38	AK13	568
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	P98	-	GND*	GND*	GND*	-
I/O	-	-	-	P181	AE11	AB34	AJ13	571
I/O	-	-	-	P180	AD11	AE39	AH13	574
I/O	-	-	-	-	AE10	AM36	AL12	577
I/O	-	-	-	-	AC11	AC35	AK12	580
I/O	-	-	P99	P179	AF9	AG39	AH12	583
I/O	-	-	P100	P178	AD10	AG37	AJ11	586
VCC	-	-	P101	P177	VCC*	VCC*	VCC*	-
I/O	P66	P86	P102	P175	AE9	AD34	AL10	589
I/O	P67	P87	P103	P174	AD9	AN39	AK10	592
I/O	P68	P88	P104	P173	AC10	AE35	AJ10	595
I/O	P69	P89	P105	P172	AF7	AH38	AK9	598
GND	P70	P90	P106	P171	GND*	GND*	GND*	-
I/O	-	-	-	P170	AE8	AJ37	AL8	601
I/O	-	-	-	P169	AD8	AG35	AH10	604
I/O	-	-	P107	P168	AC9	AF34	AJ9	607
I/O	-	-	P108	P167	AF6	AH36	AK8	610
I/O	-	P91	P109	P166	AE7	AK36	AK7	613
I/O	-	P92	P110	P165	AD7	AM34	AL6	616
I/O	P71	P93	P111	P164	AE6	AH34	AJ7	619
I/O	P72	P94	P112	P163	AE5	AJ35	AH8	622

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P162	AD6	AL37	AK6	625
I/O	-	-	-	P161	AC7	AT38	AL5	628
I/O	P73	P95	P113	P160	AF4	AM38	AH7	631
I/O	P74	P96	P114	P159	AF3	AN37	AJ6	634
I/O	-	-	-	-	AE4	AK34	AK5	637
I/O	-	-	-	-	AC6	AR39	AL4	640
I/O	P75	P97	P115	P158	AD5	AN35	AK4	643
I/O	P76	P98	P116	P157	AE3	AL33	AH5	646
I/O	P77	P99	P117	P156	AD4	AV38	AK3	649
I/O, GCK4	P78	P100	P118	P155	AC5	AT36	AJ4	652
GND	P79	P101	P119	P154	GND*	GND*	GND*	-
DONE	P80	P103	P120	P153	AD3	AR35	AH4	-
VCC	P81	P106	P121	P152	VCC*	VCC*	VCC*	-
$\overline{\text{PROGRAM}}$	P82	P108	P122	P151	AC4	AN33	AH3	-
I/O (D7)	P83	P109	P123	P150	AD2	AM32	AJ2	655
I/O, GCK5	P84	P110	P124	P149	AC3	AP34	AG4	658
I/O	P85	P111	P125	P148	AB4	AW39	AG3	661
I/O	P86	P112	P126	P147	AD1	AN31	AH2	664
I/O	-	-	-	-	AB3	AV36	AH1	667
I/O	-	-	-	-	AC2	AR33	AF4	670
I/O	-	-	P127	P146	AA4	AP32	AF3	673
I/O	-	-	P128	P145	AA3	AU35	AG2	676
I/O	-	-	-	P144	AB2	AW33	AE3	679
I/O	-	-	-	P143	AC1	AU33	AF2	682
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O (D6)	P87	P113	P129	P142	Y3	AV32	AF1	685
I/O	P88	P114	P130	P141	AA2	AU31	AD4	688
I/O	P89	P115	P131	P140	AA1	AR31	AD3	691
I/O	P90	P116	P132	P139	W4	AP28	AE2	694
I/O	-	P117	P133	P138	W3	AT32	AC3	697
I/O	-	P118	P134	P137	Y2	AV30	AD1	700
I/O	-	-	-	P136	Y1	AR29	AC2	703
I/O	-	-	-	P135	V4	AP26	AB4	706
GND	P91	P119	P135	P134	GND*	GND*	GND*	-
I/O	-	-	P136	P133	V3	AU29	AB3	709
I/O	-	-	P137	P132	W2	AV28	AB2	712
I/O	P92	P120	P138	P131	U4	AT28	AB1	715
I/O	P93	P121	P139	P130	U3	AR25	AA3	718
VCC	-	-	P140	P129	VCC*	VCC*	VCC*	-
I/O (D5)	P94	P122	P141	P127	V2	AP24	AA2	721
I/O ($\overline{\text{CS0}}$)	P95	P123	P142	P126	V1	AU27	Y2	724
I/O	-	-	-	-	T4	AR27	Y4	727
I/O	-	-	-	-	T3	AW27	Y3	730
I/O	-	-	-	P125	U2	AT24	W4	733
I/O	-	-	-	P124	T2	AR23	W3	736
GND	-	-	P143	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P123	T1	AP22	V4	739
I/O	-	-	-	P122	R4	AV24	V3	742
I/O	-	P124	P144	P121	R3	AU23	U1	745
I/O	-	P125	P145	P120	R2	AT22	U2	748
I/O	P96	P126	P146	P119	R1	AR21	U4	751
I/O	P97	P127	P147	P118	P3	AV22	U3	754
I/O (D4)	P98	P128	P148	P117	P2	AP20	T1	757
I/O	P99	P129	P149	P116	P1	AU21	T2	760
VCC	P100	P130	P150	P115	VCC*	VCC*	VCC*	-
GND	P101	P131	P151	P114	GND*	GND*	GND*	-
I/O (D3)	P102	P132	P152	P113	N2	AU19	T3	763
I/O ($\overline{\text{RS}}$)	P103	P133	P153	P112	N4	AV20	R1	766
I/O	P104	P134	P154	P111	N3	AV18	R2	769
I/O	P105	P135	P155	P110	M1	AR19	R4	772
I/O	-	P136	P156	P109	M2	AT18	R3	775
I/O	-	P137	P157	P108	M3	AW17	P2	778
I/O	-	-	-	P107	M4	AV16	P3	781
I/O	-	-	-	P106	L1	AP18	P4	784
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	P158	-	GND*	GND*	GND*	-
I/O	-	-	-	P105	L2	AR17	N3	787
I/O	-	-	-	P104	L3	AT16	N4	790
I/O	-	-	-	-	K2	AV14	M1	793
I/O	-	-	-	-	L4	AW13	M2	796
I/O (D2)	P106	P138	P159	P103	J1	AR15	L2	799

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I/O	P107	P139	P160	P102	K3	AP16	L3	802
VCC	-	-	P161	P101	VCC*	VCC*	VCC*	-
I/O	P108	P140	P162	P99	J2	AV12	K1	805
I/O	P109	P141	P163	P98	J3	AR13	K2	808
I/O	-	-	P164	P97	K4	AU11	K3	811
I/O	-	-	P165	P96	G1	AT12	K4	814
GND	P110	P142	P166	P95	GND*	GND*	GND*	-
I/O	-	-	-	P94	H2	AP14	J2	817
I/O	-	-	-	P93	H3	AR11	J3	820
I/O	-	-	P167	P92	J4	AV10	J4	823
I/O	-	-	P168	P91	F1	AT8	H1	826
I/O	-	P143	P169	P90	G2	AT10	H2	829
I/O	-	P144	P170	P89	G3	AP10	H3	832
I/O	P111	P145	P171	P88	F2	AP12	H4	835
I/O	P112	P146	P172	P87	E2	AR9	G2	838
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O (D1)	P113	P147	P173	P86	F3	AU7	G4	841
I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	P114	P148	P174	P85	G4	AW7	F2	844
I/O	-	-	-	-	D1	AW5	F3	847
I/O	-	-	-	-	C1	AV6	E1	850
I/O	-	-	-	P84	D2	AR7	E3	853
I/O	-	-	-	P83	F4	AV4	D1	856
I/O	P115	P149	P175	P82	E3	AN9	E4	859
I/O	P116	P150	P176	P81	C2	AW1	D2	862
I/O (D0, DIN)	P117	P151	P177	P80	D3	AP6	C2	865
I/O, GCK6 (DOUT)	P118	P152	P178	P79	E4	AU3	D3	868
CCLK	P119	P153	P179	P78	C3	AR5	D4	-
VCC	P120	P154	P180	P77	VCC*	VCC*	VCC*	-
O, TDO	P121	P159	P181	P76	D4	AN7	C4	0
GND	P122	P160	P182	P75	GND*	GND*	GND*	-
I/O (A0, $\overline{\text{WS}}$)	P123	P161	P183	P74	B3	AT4	B3	2
I/O, GCK7 (A1)	P124	P162	P184	P73	C4	AV2	D5	5
I/O	P125	P163	P185	P72	D5	AM8	B4	8
I/O	P126	P164	P186	P71	A3	AL7	C5	11
I/O	-	-	-	-	C5	AR3	B5	14
I/O	-	-	-	-	B4	AR1	C6	17
I/O (CS1, A2)	P127	P165	P187	P70	D6	AK6	A5	20
I/O (A3)	P128	P166	P188	P69	C6	AN3	D7	23
I/O	-	-	-	P68	B5	AM6	B6	26
I/O	-	-	-	P67	A4	AM2	A6	29
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O	-	-	P189	P66	C7	AL3	D8	32
I/O	-	-	P190	P65	B6	AH6	C7	35
I/O	P129	P167	P191	P64	A6	AP2	B7	38
I/O	P130	P168	P192	P63	D8	AK4	D9	41
I/O	-	P169	P193	P62	B7	AG5	D10	44
I/O	-	P170	P194	P61	A7	AF6	C9	47
I/O	-	-	P195	P60	D9	AL5	B9	50
I/O	-	-	-	P59	C9	AJ3	C10	53
GND	P131	P171	P196	P58	GND*	GND*	GND*	-
I/O	P132	P172	P197	P57	B8	AH2	B10	56
I/O	P133	P173	P198	P56	D10	AE5	A10	59
I/O	-	-	P199	P55	C10	AM4	C11	62
I/O	-	-	P200	P54	B9	AD6	D12	65
VCC	-	-	P201	P52	VCC*	VCC*	VCC*	-
I/O	-	-	-	P51	A9	AG3	B11	68
I/O	-	-	-	P50	D11	AG1	C12	71
I/O	-	-	-	-	C11	AC5	C13	74
I/O	-	-	-	-	B10	AE1	A12	77
I/O	-	-	-	P49	B11	AH4	D14	80
I/O	-	-	-	P48	A11	AB6	B13	83
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O (A4)	P134	P174	P202	P47	D12	AD2	C14	86
I/O (A5)	P135	P175	P203	P46	C12	AB4	A13	89
I/O	-	P176	P205	P45	B12	AE3	B14	92
I/O	P136	P177	P206	P44	A12	AC1	D15	95
I/O (A21)	P137	P178	P207	P43	C13	AD4	C15	98
I/O (A20)	P138	P179	P208	P42	B13	AA5	B15	101
I/O (A6)	P139	P180	P209	P41	A13	AA3	B16	104
I/O (A7)	P140	P181	P210	P40	B14	Y6	A16	107

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
GND	P141	P182	P211	P39	GND*	GND*	GND*	-

6/17/97

* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

†† = XL only

Additional XC4036EX/XL Package Pins

HQ208

N.C. Pins				
P1	P3	P51	P52	P53
P54	P102	P104	P105	P107
P155	P156	P157	P158	P206
P207	P208	-	-	-

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HQ240

GND Pins				
P204	P219	-	-	-

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The Ground (GND) package pins in the above table should be externally connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

HQ304

N.C. Pins				
P11	P24	P53	P100	P128
P176	P205	P254	P281	-

5/15/97

BG352

VCC Pins					
A10	A17	B2	B25	D7	D13
D19	G23	H4	K1	K26	N23
P4	U1	U26	W23	Y4	AC8
AC14	AC20	AE2	AE25	AF10	AF17
GND Pins					
A1	A2	A5	A8	A14	A19
A22	A25	A26	B1	B26	E1
E26	H1	H26	N1	P26	W1
W26	AB1	AB26	AE1	AE26	AF1
AF2	AF5	AF8	AF13	AF19	AF22
AF25	AF26	-	-	-	-
N.C. Pins					
C8	-	-	-	-	

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PG411

VCC Pins					
A3	A11	A21	A31	C39	D6
F36	J1	L39	W1	AA39	AJ1
AL39	AP4	AT34	AU1	AW9	AW19
AW29	AW37	-	-	-	-
GND Pins					
A9	A19	A29	A37	C1	D14
D20	D26	D34	F4	J39	L1
P4	P36	W39	Y4	Y36	AA1
AF4	AF36	AJ39	AL1	AP36	AT6
AT14	AT20	AT26	AU39	AW3	AW11
AW21	AW31	-	-	-	-
N.C. Pins					
A13	B6	B34	C7	C15	C23
C25	C33	D8	D12	D30	D32
E7	E23	E37	F2	F18	F22
G5	H34	J5	K36	K38	L5
L35	N3	P38	R3	V2	W5
W35	Y38	AA37	AB2	AC3	AC39
AF2	AF38	AJ5	AK2	AK38	AL35
AN1	AN5	AP8	AP30	AP38	AR37
AT2	AT30	AU5	AU9	AU13	AU15
AU17	AU25	AU37	AV8	AV26	AV34
AW15	AW23	AW25	AW35	-	-

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BG432

VCC Pins					
A1	A11	A21	A31	C3	C29
D11	D21	L1	L4	L28	L31
AA1	AA4	AA28	AA31	AH11	AH21
AJ3	AJ29	AL1	AL11	AL21	AL31
GND Pins					
A2	A3	A7	A9	A14	A18
A23	A25	A29	A30	B1	B2
B30	B31	C1	C31	D16	G1
G31	J1	J31	P1	P31	T4
T28	V1	V31	AC1	AC31	AE1
AE31	AH16	AJ1	AJ31	AK1	AK2
AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30
N.C. Pins					
A4	A8	A15	A28	B8	B12
B17	B21	B25	C8	C16	C17
D6	D13	D20	D23	D26	E2
F1	F4	F28	F29	F30	F31
G3	M3	M4	M28	M30	N1
N2	N29	N30	V2	V28	W1
W2	W28	W31	Y1	Y31	AC4
AD2	AD30	AD31	AE4	AF29	AF30
AG1	AH6	AH9	AH19	AH23	AJ5
AJ8	AJ12	AJ15	AJ20	AJ26	AK11
AK17	AK24	AK27	AL15	AL17	-

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Pin Locations for XC4044XL Devices

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
VCC	P142	P183	P212	VCC*	VCC*	VCC*
I/O (A8)	P143	P184	P213	D14	W3	D17
I/O (A9)	P144	P185	P214	C14	Y2	A17
I/O	-	-	-	-	V2	C17
I/O	-	-	-	-	W5	B17
I/O (A19)	P145	P186	P215	A15	V4	C18
I/O (A18)	P146	P187	P216	B15	T2	D18
I/O	-	P188	P217	C15	U1	B18

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	-	P189	P218	D15	V6	A19
I/O (A10)	P147	P190	P220	A16	U3	B19
I/O (A11)	P148	P191	P221	B16	R1	C19
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O	-	-	-	C16	U5	D19
I/O	-	-	-	B17	T4	A20
I/O	-	-	-	D16	P2	B20
I/O	-	-	-	A18	N1	C20

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	-	-	-	C17	R5	C21
I/O	-	-	-	B18	M2	A22
VCC	-	-	P222	VCC*	VCC*	VCC*
I/O	-	-	P223	C18	L3	B22
I/O	-	-	P224	D17	T6	C22
I/O	P149	P192	P225	A20	N5	B23
I/O	P150	P193	P226	B19	M4	A24
GND	P151	P194	P227	GND*	GND*	GND*
I/O	-	-	-	C19	K2	D22
I/O	-	-	-	D18	K4	C23
I/O	-	P195	P228	A21	P6	B24
I/O	-	P196	P229	B20	M6	C24
I/O	-	-	-	-	L5	D23
I/O	-	-	-	-	J5	B25
I/O	P152	P197	P230	C20	J3	A26
I/O	P153	P198	P231	B21	H2	C25
I/O (A12)	P154	P199	P232	B22	H4	D24
I/O (A13)	P155	P200	P233	C21	G3	B26
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	D20	K6	A27
I/O	-	-	-	A23	G1	D25
I/O	-	-	-	A24	E1	C26
I/O	-	-	-	B23	E3	B27
I/O	-	-	P234	D21	J7	C27
I/O	-	-	P235	C22	H6	B28
I/O	P156	P201	P236	B24	C3	D27
I/O	P157	P202	P237	C23	D2	B29
I/O (A14)	P158	P203	P238	D22	E5	C28
I/O, GCK8 (A15)	P159	P204	P239	C24	G7	D28
VCC	P160	P205	P240	VCC*	VCC*	VCC*
GND	P1	P2	P1	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	P4	P2	D23	H8	D29
I/O (A17)	P3	P5	P3	C25	F6	C30
I/O	P4	P6	P4	D24	B4	E28
I/O	P5	P7	P5	E23	D4	E29
I/O, TDI	P6	P8	P6	C26	B2	D30
I/O, TCK	P7	P9	P7	E24	G9	D31
I/O	-	-	-	D25	F8	E30
I/O	-	-	-	F23	C5	E31
I/O	-	-	-	F24	A7	G28
I/O	-	-	-	E25	A5	G29
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	C7	F30
I/O	-	-	-	-	D8	F31
I/O	P8	P10	P8	D26	B8	H28
I/O	P9	P11	P9	G24	C9	H29
I/O	-	P12	P10	F25	E9	G30
I/O	-	P13	P11	F26	F12	H30
I/O	-	-	P12	H23	D10	J28
I/O	-	-	P13	H24	B10	J29
I/O	-	-	-	G25	F10	H31
I/O	-	-	-	G26	F14	J30
GND	P10	P14	P14	GND*	GND*	GND*
I/O	P11	P15	P15	J23	C11	K28
I/O	P12	P16	P16	J24	B12	K29
I/O, TMS	P13	P17	P17	H25	E11	K30
I/O	P14	P18	P18	K23	E15	K31
VCC	-	-	P19	VCC*	VCC*	VCC*
I/O	-	-	P20	K24	F16	L29
I/O	-	-	P21	J25	C13	L30
I/O	-	-	-	J26	B14	M29
I/O	-	-	-	L23	E17	M31
I/O	-	-	-	L24	E13	N31
I/O	-	-	-	K25	A15	N28
GND	-	-	P22	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	F18	N29
I/O	-	-	-	-	C15	N30
I/O	-	-	-	L25	B16	P30
I/O	-	-	-	L26	D16	P28
I/O	-	P19	P23	M23	D18	P29
I/O	-	P20	P24	M24	A17	R31
I/O	P15	P21	P25	M25	E19	R30

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	P16	P22	P26	M26	B18	R28
I/O	P17	P23	P27	N24	C17	R29
I/O	P18	P24	P28	N25	C19	T31
GND	P19	P25	P29	GND*	GND*	GND*
VCC	P20	P26	P30	VCC*	VCC*	VCC*
I/O	P21	P27	P31	N26	F20	T30
I/O	P22	P28	P32	P25	B20	T29
I/O	P23	P29	P33	P23	C21	U31
I/O	P24	P30	P34	P24	B22	U30
I/O	-	P31	P35	R26	E21	U28
I/O	-	P32	P36	R25	D22	U29
I/O	-	-	-	R24	A23	V30
I/O	-	-	-	R23	B24	V29
I/O	-	-	-	-	C23	V28
I/O	-	-	-	-	F22	W31
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P37	GND*	GND*	GND*
I/O	-	-	-	T26	A25	W30
I/O	-	-	-	T25	D24	W29
I/O	-	-	-	T24	B26	Y30
I/O	-	-	-	U25	A27	Y29
I/O	-	-	P38	T23	C27	Y28
I/O	-	-	P39	V26	F24	AA30
VCC	-	-	P40	VCC*	VCC*	VCC*
I/O	P25	P33	P41	U24	E25	AA29
I/O	P26	P34	P42	V25	E27	AB31
I/O	P27	P35	P43	V24	B28	AB30
I/O	P28	P36	P44	U23	C29	AB29
GND	P29	P37	P45	GND*	GND*	GND*
I/O	-	-	-	Y26	F26	AB28
I/O	-	-	-	W25	D28	AC30
I/O	-	-	P46	W24	B30	AC29
I/O	-	-	P47	V23	E29	AC28
I/O	-	-	-	-	D30	AD31
I/O	-	-	-	-	D32	AD30
I/O	-	P38	P48	AA26	F28	AD29
I/O	-	P39	P49	Y25	F30	AD28
I/O	P30	P40	P50	Y24	C31	AE30
I/O	P31	P41	P51	AA25	E31	AE29
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	AB25	B32	AF31
I/O	-	-	-	AA24	A33	AE28
I/O	P32	P42	P52	Y23	A35	AG31
I/O	P33	P43	P53	AC26	F32	AF28
I/O	-	-	-	AD26	C35	AG30
I/O	-	-	-	AC25	B38	AG29
I/O	P34	P44	P54	AA23	E33	AH31
I/O	P35	P45	P55	AB24	G31	AG28
I/O	P36	P46	P56	AD25	H32	AH30
I/O, GCK2	P37	P47	P57	AC24	B36	AJ30
O (M1)	P38	P48	P58	AB23	A39	AH29
GND	P39	P49	P59	GND*	GND*	GND*
I (M0)	P40	P50	P60	AD24	E35	AH28
VCC	P41	P55	P61	VCC*	VCC*	VCC*
I (M2)	P42	P56	P62	AC23	G33	AJ28
I/O, GCK3	P43	P57	P63	AE24	D36	AK29
I/O (HDC)	P44	P58	P64	AD23	C37	AH27
I/O	P45	P59	P65	AC22	F34	AK28
I/O	P46	P60	P66	AF24	J33	AJ27
I/O	P47	P61	P67	AD22	D38	AL28
I/O ($\overline{LDC}$)	P48	P62	P68	AE23	G35	AH26
I/O	-	-	-	AC21	E39	AL27
I/O	-	-	-	AD21	K34	AH25
I/O	-	-	-	AE22	F38	AK26
I/O	-	-	-	AF23	G37	AL26
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O	P49	P63	P69	AD20	H38	AH24
I/O	P50	P64	P70	AE21	J37	AJ25
I/O	-	P65	P71	AF21	G39	AK25
I/O	-	P66	P72	AC19	M34	AJ24
I/O	-	-	-	-	K36	AH23
I/O	-	-	-	-	K38	AK24
I/O	-	-	P73	AD19	N35	AL24

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	-	-	P74	AE20	P34	AH22
I/O	-	-	-	AF20	J35	AJ23
I/O	-	-	-	AC18	L37	AK23
GND	P51	P67	P75	GND*	GND*	GND*
I/O	P52	P68	P76	AD18	M38	AJ22
I/O	P53	P69	P77	AE19	R35	AK22
I/O	P54	P70	P78	AC17	H36	AL22
I/O	P55	P71	P79	AD17	T34	AJ21
VCC	-	-	P80	VCC*	VCC*	VCC*
I/O	-	P72	P81	AE18	N37	AH20
I/O	-	P73	P82	AF18	N39	AK21
I/O	-	-	-	AC16	U35	AK20
I/O	-	-	-	AD16	R39	AJ19
I/O	-	-	-	AE17	M36	AL20
I/O	-	-	-	AE16	V34	AH18
GND	-	-	P83	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	AF16	R37	AK19
I/O	-	-	-	AC15	T38	AJ18
I/O	-	-	P84	AD15	T36	AL19
I/O	-	-	P85	AE15	V36	AK18
I/O	P56	P74	P86	AF15	U37	AH17
I/O	P57	P75	P87	AD14	U39	AJ17
I/O	-	-	-	-	W35	AK17
I/O	-	-	-	-	AC39	AL17
I/O	P58	P76	P88	AE14	V38	AJ16
I/O ($\overline{INIT}$)	P59	P77	P89	AF14	W37	AK16
VCC	P60	P78	P90	VCC*	VCC*	VCC*
GND	P61	P79	P91	GND*	GND*	GND*
I/O	P62	P80	P92	AE13	Y34	AL16
I/O	P63	P81	P93	AC13	AC37	AH15
I/O	-	-	-	-	Y38	AL15
I/O	-	-	-	-	AA37	AJ15
I/O	P64	P82	P94	AD13	AB38	AK15
I/O	P65	P83	P95	AF12	AD36	AJ14
I/O	-	P84	P96	AE12	AA35	AH14
I/O	-	P85	P97	AD12	AE37	AK14
I/O	-	-	-	AC12	AB36	AL13
I/O	-	-	-	AF11	AD38	AK13
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P98	GND*	GND*	GND*
I/O	-	-	-	AE11	AB34	AJ13
I/O	-	-	-	AD11	AE39	AH13
I/O	-	-	-	AE10	AM36	AL12
I/O	-	-	-	AC11	AC35	AK12
I/O	-	-	P99	AF9	AG39	AH12
I/O	-	-	P100	AD10	AG37	AJ11
VCC	-	-	P101	VCC*	VCC*	VCC*
I/O	P66	P86	P102	AE9	AD34	AL10
I/O	P67	P87	P103	AD9	AN39	AK10
I/O	P68	P88	P104	AC10	AE35	AJ10
I/O	P69	P89	P105	AF7	AH38	AK9
GND	P70	P90	P106	GND*	GND*	GND*
I/O	-	-	-	AE8	AJ37	AL8
I/O	-	-	-	AD8	AG35	AH10
I/O	-	-	P107	AC9	AF34	AJ9
I/O	-	-	P108	AF6	AH36	AK8
I/O	-	-	-	-	AK38	AJ8
I/O	-	-	-	-	AP38	AH9
I/O	-	P91	P109	AE7	AK36	AK7
I/O	-	P92	P110	AD7	AM34	AL6
I/O	P71	P93	P111	AE6	AH34	AJ7
I/O	P72	P94	P112	AE5	AJ35	AH8
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	AD6	AL37	AK6
I/O	-	-	-	AC7	AT38	AL5
I/O	P73	P95	P113	AF4	AM38	AH7
I/O	P74	P96	P114	AF3	AN37	AJ6
I/O	-	-	-	AE4	AK34	AK5
I/O	-	-	-	AC6	AR39	AL4
I/O	P75	P97	P115	AD5	AN35	AK4
I/O	P76	P98	P116	AE3	AL33	AH5
I/O	P77	P99	P117	AD4	AV38	AK3
I/O, GCK4	P78	P100	P118	AC5	AT36	AJ4

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
GND	P79	P101	P119	GND*	GND*	GND*
DONE	P80	P103	P120	AD3	AR35	AH4
VCC	P81	P106	P121	VCC*	VCC*	VCC*
$\overline{PROGRAM}$	P82	P108	P122	AC4	AN33	AH3
I/O (D7)	P83	P109	P123	AD2	AM32	AJ2
I/O, GCK5	P84	P110	P124	AC3	AP34	AG4
I/O	P85	P111	P125	AB4	AW39	AG3
I/O	P86	P112	P126	AD1	AN31	AH2
I/O	-	-	-	AB3	AV36	AH1
I/O	-	-	-	AC2	AR33	AF4
I/O	-	-	P127	AA4	AP32	AF3
I/O	-	-	P128	AA3	AU35	AG2
I/O	-	-	-	AB2	AW33	AE3
I/O	-	-	-	AC1	AU33	AF2
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O (D6)	P87	P113	P129	Y3	AV32	AF1
I/O	P88	P114	P130	AA2	AU31	AD4
I/O	P89	P115	P131	AA1	AR31	AD3
I/O	P90	P116	P132	W4	AP28	AE2
I/O	-	-	-	-	AP30	AD2
I/O	-	-	-	-	AT30	AC4
I/O	-	P117	P133	W3	AT32	AC3
I/O	-	P118	P134	Y2	AV30	AD1
I/O	-	-	-	Y1	AR29	AC2
I/O	-	-	-	V4	AP26	AB4
GND	P91	P119	P135	GND*	GND*	GND*
I/O	-	-	P136	V3	AU29	AB3
I/O	-	-	P137	W2	AV28	AB2
I/O	P92	P120	P138	U4	AT28	AB1
I/O	P93	P121	P139	U3	AR25	AA3
VCC	-	-	P140	VCC*	VCC*	VCC*
I/O (D5)	P94	P122	P141	V2	AP24	AA2
I/O ($\overline{CS0}$)	P95	P123	P142	V1	AU27	Y2
I/O	-	-	-	T4	AR27	Y4
I/O	-	-	-	T3	AW27	Y3
I/O	-	-	-	U2	AT24	W4
I/O	-	-	-	T2	AR23	W3
GND	-	-	P143	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	AW25	W2
I/O	-	-	-	-	AW23	V2
I/O	-	-	-	T1	AP22	V4
I/O	-	-	-	R4	AV24	V3
I/O	-	P124	P144	R3	AU23	U1
I/O	-	P125	P145	R2	AT22	U2
I/O	P96	P126	P146	R1	AR21	U4
I/O	P97	P127	P147	P3	AV22	U3
I/O (D4)	P98	P128	P148	P2	AP20	T1
I/O	P99	P129	P149	P1	AU21	T2
VCC	P100	P130	P150	VCC*	VCC*	VCC*
GND	P101	P131	P151	GND*	GND*	GND*
I/O (D3)	P102	P132	P152	N2	AU19	T3
I/O ($\overline{RS}$)	P103	P133	P153	N4	AV20	R1
I/O	P104	P134	P154	N3	AV18	R2
I/O	P105	P135	P155	M1	AR19	R4
I/O	-	P136	P156	M2	AT18	R3
I/O	-	P137	P157	M3	AW17	P2
I/O	-	-	-	M4	AV16	P3
I/O	-	-	-	L1	AP18	P4
I/O	-	-	-	-	AU17	N1
I/O	-	-	-	-	AW15	N2
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P158	GND*	GND*	GND*
I/O	-	-	-	L2	AR17	N3
I/O	-	-	-	L3	AT16	N4
I/O	-	-	-	K2	AV14	M1
I/O	-	-	-	L4	AW13	M2
I/O (D2)	P106	P138	P159	J1	AR15	L2
I/O	P107	P139	P160	K3	AP16	L3
VCC	-	-	P161	VCC*	VCC*	VCC*
I/O	P108	P140	P162	J2	AV12	K1
I/O	P109	P141	P163	J3	AR13	K2
I/O	-	-	P164	K4	AU11	K3
I/O	-	-	P165	G1	AT12	K4

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
GND	P110	P142	P166	GND*	GND*	GND*
I/O	-	-	-	H2	AP14	J2
I/O	-	-	-	H3	AR11	J3
I/O	-	-	P167	J4	AV10	J4
I/O	-	-	P168	F1	AT8	H1
I/O	-	P143	P169	G2	AT10	H2
I/O	-	P144	P170	G3	AP10	H3
I/O	P111	P145	P171	F2	AP12	H4
I/O	P112	P146	P172	E2	AR9	G2
I/O	-	-	-	-	AU9	G3
I/O	-	-	-	-	AV8	F1
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O (D1)	P113	P147	P173	F3	AU7	G4
I/O (RCLK, RDY/BUSY)	P114	P148	P174	G4	AW7	F2
I/O	-	-	-	D1	AW5	F3
I/O	-	-	-	C1	AV6	E1
I/O	-	-	-	D2	AR7	E3
I/O	-	-	-	F4	AV4	D1
I/O	P115	P149	P175	E3	AN9	E4
I/O	P116	P150	P176	C2	AW1	D2
I/O (D0, DIN)	P117	P151	P177	D3	AP6	C2
I/O, GCK6 (DOUT)	P118	P152	P178	E4	AU3	D3
CCLK	P119	P153	P179	C3	AR5	D4
VCC	P120	P154	P180	VCC*	VCC*	VCC*
O, TDO	P121	P159	P181	D4	AN7	C4
GND	P122	P160	P182	GND*	GND*	GND*
I/O (A0, WS)	P123	P161	P183	B3	AT4	B3
I/O, GCK7 (A1)	P124	P162	P184	C4	AV2	D5
I/O	P125	P163	P185	D5	AM8	B4
I/O	P126	P164	P186	A3	AL7	C5
I/O	-	-	-	C5	AR3	B5
I/O	-	-	-	B4	AR1	C6
I/O (CS1,A2)	P127	P165	P187	D6	AK6	A5
I/O (A3)	P128	P166	P188	C6	AN3	D7
I/O	-	-	-	B5	AM6	B6
I/O	-	-	-	A4	AM2	A6
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O	-	-	P189	C7	AL3	D8
I/O	-	-	P190	B6	AH6	C7
I/O	P129	P167	P191	A6	AP2	B7
I/O	P130	P168	P192	D8	AK4	D9
I/O	-	-	-	C8	AN1	B8
I/O	-	-	-	-	AK2	A8
I/O	-	P169	P193	B7	AG5	D10
I/O	-	P170	P194	A7	AF6	C9
I/O	-	-	P195	D9	AL5	B9
I/O	-	-	-	C9	AJ3	C10
GND	P131	P171	P196	GND*	GND*	GND*
I/O	P132	P172	P197	B8	AH2	B10
I/O	P133	P173	P198	D10	AE5	A10
I/O	-	-	P199	C10	AM4	C11
I/O	-	-	P200	B9	AD6	D12
VCC	-	-	P201	VCC*	VCC*	VCC*
I/O	-	-	-	A9	AG3	B11
I/O	-	-	-	D11	AG1	C12
I/O	-	-	-	C11	AC5	C13
I/O	-	-	-	B10	AE1	A12
I/O	-	-	-	B11	AH4	D14
I/O	-	-	-	A11	AB6	B13
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O (A4)	P134	P174	P202	D12	AD2	C14
I/O (A5)	P135	P175	P203	C12	AB4	A13
I/O	-	P176	P205	B12	AE3	B14
I/O	P136	P177	P206	A12	AC1	D15
I/O (A21)	P137	P178	P207	C13	AD4	C15
I/O (A20)	P138	P179	P208	B13	AA5	B15
I/O	-	-	-	-	AB2	A15
I/O	-	-	-	-	AC3	C16
I/O (A6)	P139	P180	P209	A13	AA3	B16
I/O (A7)	P140	P181	P210	B14	Y6	A16
GND	P141	P182	P211	GND*	GND*	GND*

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* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

Additional XC4044XL Package Pins

HQ208

N.C. Pins						
P1	P3	P51	P52	P53	P54	P102
P104	P105	P107	P155	P156	P157	P158
P206	P207	P208	-	-	-	-

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HQ240

GND Pins						
P204	P219	-	-	-	-	-

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Note: These pins may be N.C. for this device revision, however for compatability with other devices in this package, these pins should be tied to GND.

BG352

VCC Pins						
A10	A17	B2	B25	D7	D13	D19
G23	H4	K1	K26	N23	P4	U1
U26	W23	Y4	AC8	AC14	AC20	AE2
AE25	AF10	AF17	-	-	-	-
GND Pins						
A1	A2	A5	A8	A14	A19	A22
A25	A26	B1	B26	E1	E26	H1
H26	N1	P26	W1	W26	AB1	AB26
AE1	AE26	AF1	AF2	AF5	AF8	AF13
AF19	AF22	AF25	AF26	-	-	-

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PG411

VCC Pins						
A3	A11	A21	A31	C39	D6	F36
J1	L39	W1	AA39	AJ1	AL39	AP4
AT34	AU1	AW9	AW19	AW29	AW37	-
GND Pins						
A9	A19	A29	A37	C1	D14	D20
D26	D34	F4	J39	L1	P4	P36
W39	Y4	Y36	AA1	AF4	AF36	AJ39
AL1	AP36	AT6	AT14	AT20	AT26	AU39
AW3	AW11	AW21	AW31	-	-	-
N.C. Pins						
A13	B6	B34	C25	C33	D12	E7
E23	E37	F2	G5	H34	L35	N3
P38	R3	AF2	AF38	AJ5	AL35	AN5
AP8	AR37	AT2	AU5	AU13	AU15	AU25
AU37	AV26	AV34	AW35	-	-	-

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BG432

VCC Pins						
A1	A11	A21	A31	C3	C29	D11
D21	L1	L4	L28	L31	AA1	AA4
AA28	AA31	AH11	AH21	AJ3	AJ29	AL1
AL11	AL21	AL31	-	-	-	-
GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1
AK2	AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30	-
N.C. Pins						
A4	A28	B12	B21	C8	D6	D13
D20	D26	E2	F4	F28	F29	M3
M4	M28	M30	W1	W28	Y1	Y31
AE4	AF29	AF30	AG1	AH6	AH19	AJ5
AJ12	AJ20	AJ26	AK11	AK27	-	-

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Pin Locations for XC4052XL Devices

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
VCC	P212	VCC*	VCC*	VCC*
I/O (A8)	P213	W3	D17	A17
I/O (A9)	P214	Y2	A17	B18
I/O	-	V2	C17	C18
I/O	-	W5	B17	E18
GND	-	GND*	GND*	GND*
I/O (A19)	P215	V4	C18	C19
I/O (A18)	P216	T2	D18	D19
I/O	P217	U1	B18	E19
I/O	P218	V6	A19	B20
I/O (A10)	P220	U3	B19	C20
I/O (A11)	P221	R1	C19	D20
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	U5	D19	A21
I/O	-	T4	A20	E20
I/O	-	P2	B20	B21
I/O	-	N1	C20	C21
I/O	-	R3	B21	D21
I/O	-	N3	D20	B22
GND	-	GND*	GND*	GND*
I/O	-	R5	C21	C23
I/O	-	M2	A22	E22
VCC	P222	VCC*	VCC*	VCC*
I/O	P223	L3	B22	B24
I/O	P224	T6	C22	D23
I/O	P225	N5	B23	C24
I/O	P226	M4	A24	A25
GND	P227	GND*	GND*	GND*
I/O	-	K2	D22	E23
I/O	-	K4	C23	B25
I/O	P228	P6	B24	D24
I/O	P229	M6	C24	C25
GND	-	GND*	GND*	GND*
I/O	-	L5	D23	E25
I/O	-	J5	B25	C27
I/O	P230	J3	A26	D26
I/O	P231	H2	C25	B28
I/O (A12)	P232	H4	D24	B29
I/O (A13)	P233	G3	B26	E26
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	K6	A27	C28
I/O	-	G1	D25	D27
I/O	-	E1	C26	B30

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
I/O	-	E3	B27	C29
I/O	-	F2	A28	E27
I/O	-	G5	D26	A31
GND	-	GND*	GND*	GND*
I/O	P234	J7	C27	D28
I/O	P235	H6	B28	C30
I/O	P236	C3	D27	D29
I/O	P237	D2	B29	E28
I/O (A14)	P238	E5	C28	D30
I/O, GCK8 (A15)	P239	G7	D28	E29
VCC	P240	VCC*	VCC*	VCC*
GND	P1	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	H8	D29	B33
I/O (A17)	P3	F6	C30	F29
I/O	P4	B4	E28	E30
I/O	P5	D4	E29	D31
I/O, TDI	P6	B2	D30	F30
I/O, TCK	P7	G9	D31	C33
GND	-	GND*	GND*	GND*
I/O	-	E7	F28	G29
I/O	-	B6	F29	E31
I/O	-	F8	E30	D32
I/O	-	C5	E31	G30
I/O	-	A7	G28	F31
I/O	-	A5	G29	H29
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	C7	F30	H30
I/O	-	D8	F31	G31
I/O	P8	B8	H28	J29
I/O	P9	C9	H29	F33
I/O	P10	E9	G30	G32
I/O	P11	F12	H30	J30
GND	-	GND*	GND*	GND*
I/O	P12	D10	J28	K30
I/O	P13	B10	J29	H33
I/O	-	F10	H31	L29
I/O	-	F14	J30	K31
GND	P14	GND*	GND*	GND*
I/O	P15	C11	K28	L30
I/O	P16	B12	K29	K32
I/O, TMS	P17	E11	K30	J33
I/O	P18	E15	K31	M29
VCC	P19	VCC*	VCC*	VCC*
I/O	P20	F16	L29	L32

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
I/O	P21	C13	L30	M31
GND	-	GND*	GND*	GND*
I/O	-	A13	M30	N29
I/O	-	D12	M28	L33
I/O	-	B14	M29	M32
I/O	-	E17	M31	P29
I/O	-	E13	N31	P30
I/O	-	A15	N28	N33
GND	P22	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	F18	N29	P31
I/O	-	C15	N30	P32
I/O	-	B16	P30	R29
I/O	-	D16	P28	R30
I/O	P23	D18	P29	R31
I/O	P24	A17	R31	R33
GND	-	GND*	GND*	GND*
I/O	P25	E19	R30	T31
I/O	P26	B18	R28	T29
I/O	P27	C17	R29	U32
I/O	P28	C19	T31	U31
GND	P29	GND*	GND*	GND*
VCC	P30	VCC*	VCC*	VCC*
I/O	P31	F20	T30	U29
I/O	P32	B20	T29	U30
I/O	P33	C21	U31	V31
I/O	P34	B22	U30	V29
GND	-	GND*	GND*	GND*
I/O	P35	E21	U28	V30
I/O	P36	D22	U29	W33
I/O	-	A23	V30	W31
I/O	-	B24	V29	W30
I/O	-	C23	V28	W29
I/O	-	F22	W31	Y32
VCC	-	VCC*	VCC*	VCC*
GND	P37	GND*	GND*	GND*
I/O	-	A25	W30	Y31
I/O	-	D24	W29	Y30
I/O	-	E23	W28	AA32
I/O	-	C25	Y31	AA31
I/O	-	B26	Y30	AA30
I/O	-	A27	Y29	AB32
GND	-	GND*	GND*	GND*
I/O	P38	C27	Y28	AA29
I/O	P39	F24	AA30	AB31
VCC	P40	VCC*	VCC*	VCC*
I/O	P41	E25	AA29	AC31
I/O	P42	E27	AB31	AB29
I/O	P43	B28	AB30	AD32
I/O	P44	C29	AB29	AC30
GND	P45	GND*	GND*	GND*
I/O	-	F26	AB28	AD31
I/O	-	D28	AC30	AE33
I/O	P46	B30	AC29	AC29
I/O	P47	E29	AC28	AE32
GND	-	GND*	GND*	GND*
I/O	-	D30	AD31	AG33
I/O	-	D32	AD30	AH33
I/O	P48	F28	AD29	AE29
I/O	P49	F30	AD28	AG31
I/O	P50	C31	AE30	AF30
I/O	P51	E31	AE29	AH32
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	B32	AF31	AJ32
I/O	-	A33	AE28	AF29
I/O	-	C33	AF30	AH31
I/O	-	B34	AF29	AG30
I/O	P52	A35	AG31	AK32
I/O	P53	F32	AF28	AJ31

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
GND	-	GND*	GND*	GND*
I/O	-	C35	AG30	AG29
I/O	-	B38	AG29	AL33
I/O	P54	E33	AH31	AH30
I/O	P55	G31	AG28	AK31
I/O	P56	H32	AH30	AJ30
I/O, GCK2	P57	B36	AJ30	AH29
O (M1)	P58	A39	AH29	AK30
GND	P59	GND*	GND*	GND*
I (M0)	P60	E35	AH28	AJ29
VCC	P61	VCC*	VCC*	VCC*
I (M2)	P62	G33	AJ28	AN32
I/O, GCK3	P63	D36	AK29	AJ28
I/O (HDC)	P64	C37	AH27	AK29
I/O	P65	F34	AK28	AL30
I/O	P66	J33	AJ27	AK28
I/O	P67	D38	AL28	AM31
I/O ($\overline{LDC}$)	P68	G35	AH26	AJ27
GND	-	GND*	GND*	GND*
I/O	-	E37	AK27	AN31
I/O	-	H34	AJ26	AL29
I/O	-	E39	AL27	AK27
I/O	-	K34	AH25	AL28
I/O	-	F38	AK26	AJ26
I/O	-	G37	AL26	AM30
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P69	H38	AH24	AM29
I/O	P70	J37	AJ25	AK26
I/O	P71	G39	AK25	AL27
I/O	P72	M34	AJ24	AJ25
I/O	-	K36	AH23	AN29
I/O	-	K38	AK24	AN28
GND	-	GND*	GND*	GND*
I/O	P73	N35	AL24	AL25
I/O	P74	P34	AH22	AJ23
I/O	-	J35	AJ23	AN26
I/O	-	L37	AK23	AL24
GND	P75	GND*	GND*	GND*
I/O	P76	M38	AJ22	AK23
I/O	P77	R35	AK22	AN25
I/O	P78	H36	AL22	AJ22
I/O	P79	T34	AJ21	AL23
VCC	P80	VCC*	VCC*	VCC*
I/O	P81	N37	AH20	AM24
I/O	P82	N39	AK21	AK22
GND	-	GND*	GND*	GND*
I/O	-	P38	AJ20	AK21
I/O	-	L35	AH19	AM22
I/O	-	U35	AK20	AJ20
I/O	-	R39	AJ19	AL21
I/O	-	M36	AL20	AN21
I/O	-	V34	AH18	AK20
GND	P83	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	R37	AK19	AL20
I/O	-	T38	AJ18	AJ19
I/O	P84	T36	AL19	AM20
I/O	P85	V36	AK18	AK19
I/O	P86	U37	AH17	AL19
I/O	P87	U39	AJ17	AN19
GND	-	GND*	GND*	GND*
I/O	-	W35	AK17	AL18
I/O	-	AC39	AL17	AM18
I/O	P88	V38	AJ16	AK17
I/O ($\overline{INIT}$)	P89	W37	AK16	AJ17
VCC	P90	VCC*	VCC*	VCC*
GND	P91	GND*	GND*	GND*
I/O	P92	Y34	AL16	AL17
I/O	P93	AC37	AH15	AM17

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
I/O	-	Y38	AL15	AN17
I/O	-	AA37	AJ15	AK16
GND	-	GND*	GND*	GND*
I/O	P94	AB38	AK15	AM16
I/O	P95	AD36	AJ14	AL15
I/O	P96	AA35	AH14	AK15
I/O	P97	AE37	AK14	AJ15
I/O	-	AB36	AL13	AN15
I/O	-	AD38	AK13	AM14
VCC	-	VCC*	VCC*	VCC*
GND	P98	GND*	GND*	GND*
I/O	-	AB34	AJ13	AL14
I/O	-	AE39	AH13	AK14
I/O	-	AM36	AL12	AJ14
I/O	-	AC35	AK12	AN13
I/O	-	AL35	AJ12	AM13
I/O	-	AF38	AK11	AL13
GND	-	GND*	GND*	GND*
I/O	P99	AG39	AH12	AK12
I/O	P100	AG37	AJ11	AN11
VCC	P101	VCC*	VCC*	VCC*
I/O	P102	AD34	AL10	AJ12
I/O	P103	AN39	AK10	AL11
I/O	P104	AE35	AJ10	AK11
I/O	P105	AH38	AK9	AM10
GND	P106	GND*	GND*	GND*
I/O	-	AJ37	AL8	AL10
I/O	-	AG35	AH10	AJ11
I/O	P107	AF34	AJ9	AN9
I/O	P108	AH36	AK8	AK10
GND	-	GND*	GND*	GND*
I/O	-	AK38	AJ8	AN7
I/O	-	AP38	AH9	AJ9
I/O	P109	AK36	AK7	AL7
I/O	P110	AM34	AL6	AK8
I/O	P111	AH34	AJ7	AN6
I/O	P112	AJ35	AH8	AM6
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AL37	AK6	AJ8
I/O	-	AT38	AL5	AL6
I/O	P113	AM38	AH7	AK7
I/O	P114	AN37	AJ6	AM5
I/O	-	AK34	AK5	AM4
I/O	-	AR39	AL4	AJ7
GND	-	GND*	GND*	GND*
I/O	-	AR37	AH6	AL5
I/O	-	AU37	AJ5	AK6
I/O	P115	AN35	AK4	AN3
I/O	P116	AL33	AH5	AK5
I/O	P117	AV38	AK3	AJ6
I/O, GCK4	P118	AT36	AJ4	AL4
GND	P119	GND*	GND*	GND*
DONE	P120	AR35	AH4	AJ5
VCC	P121	VCC*	VCC*	VCC*
PROGRAM	P122	AN33	AH3	AM1
I/O (D7)	P123	AM32	AJ2	AH5
I/O, GCK5	P124	AP34	AG4	AJ4
I/O	P125	AW39	AG3	AK3
I/O	P126	AN31	AH2	AH4
I/O	-	AV36	AH1	AL1
I/O	-	AR33	AF4	AG5
GND	-	GND*	GND*	GND*
I/O	P127	AP32	AF3	AJ3
I/O	P128	AU35	AG2	AK2
I/O	-	AV34	AG1	AG4
I/O	-	AW35	AE4	AH3
I/O	-	AW33	AE3	AF5
I/O	-	AU33	AF2	AJ2
VCC	-	VCC*	VCC*	VCC*

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
GND	-	GND*	GND*	GND*
I/O (D6)	P129	AV32	AF1	AJ1
I/O	P130	AU31	AD4	AF4
I/O	P131	AR31	AD3	AG3
I/O	P132	AP28	AE2	AE5
I/O	-	AP30	AD2	AH1
I/O	-	AT30	AC4	AF3
GND	-	GND*	GND*	GND*
I/O	P133	AT32	AC3	AE3
I/O	P134	AV30	AD1	AC5
I/O	-	AR29	AC2	AE1
I/O	-	AP26	AB4	AD3
GND	P135	GND*	GND*	GND*
I/O	P136	AU29	AB3	AC4
I/O	P137	AV28	AB2	AD2
I/O	P138	AT28	AB1	AB5
I/O	P139	AR25	AA3	AC3
VCC	P140	VCC*	VCC*	VCC*
I/O (D5)	P141	AP24	AA2	AA5
I/O ($\overline{CS0}$)	P142	AU27	Y2	AB3
GND	-	GND*	GND*	GND*
I/O	-	AR27	Y4	AB2
I/O	-	AW27	Y3	AA4
I/O	-	AU25	Y1	AA3
I/O	-	AV26	W1	Y5
I/O	-	AT24	W4	Y3
I/O	-	AR23	W3	Y2
GND	P143	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AW25	W2	W5
I/O	-	AW23	V2	W4
I/O	-	AP22	V4	W3
I/O	-	AV24	V3	W1
I/O	P144	AU23	U1	V3
I/O	P145	AT22	U2	V5
GND	-	GND*	GND*	GND*
I/O	P146	AR21	U4	V4
I/O	P147	AV22	U3	V2
I/O (D4)	P148	AP20	T1	U5
I/O	P149	AU21	T2	U4
VCC	P150	VCC*	VCC*	VCC*
GND	P151	GND*	GND*	GND*
I/O (D3)	P152	AU19	T3	U3
I/O ($\overline{RS}$)	P153	AV20	R1	T2
I/O	P154	AV18	R2	T4
I/O	P155	AR19	R4	R1
GND	-	GND*	GND*	GND*
I/O	P156	AT18	R3	R3
I/O	P157	AW17	P2	R4
I/O	-	AV16	P3	R5
I/O	-	AP18	P4	P2
I/O	-	AU17	N1	P3
I/O	-	AW15	N2	P4
VCC	-	VCC*	VCC*	VCC*
GND	P158	GND*	GND*	GND*
I/O	-	AR17	N3	N1
I/O	-	AT16	N4	P5
I/O	-	AV14	M1	N2
I/O	-	AW13	M2	N3
I/O	-	AU15	M3	N5
I/O	-	AU13	M4	M3
GND	-	GND*	GND*	GND*
I/O (D2)	P159	AR15	L2	M4
I/O	P160	AP16	L3	L1
VCC	P161	VCC*	VCC*	VCC*
I/O	P162	AV12	K1	K2
I/O	P163	AR13	K2	L4
I/O	P164	AU11	K3	J1
I/O	P165	AT12	K4	K3
GND	P166	GND*	GND*	GND*

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
I/O	-	AP14	J2	L5
I/O	-	AR11	J3	J2
I/O	P167	AV10	J4	K4
I/O	P168	AT8	H1	J3
GND	-	GND*	GND*	GND*
I/O	P169	AT10	H2	G1
I/O	P170	AP10	H3	F1
I/O	P171	AP12	H4	J5
I/O	P172	AR9	G2	G3
I/O	-	AU9	G3	H4
I/O	-	AV8	F1	F2
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O (D1)	P173	AU7	G4	F3
I/O ($\overline{RCLK}$, $\overline{RDY/BUSY}$)	P174	AW7	F2	G4
I/O	-	AW5	F3	D2
I/O	-	AV6	E1	E3
I/O	-	AU5	F4	G5
I/O	-	AP8	E2	C1
GND	-	GND*	GND*	GND*
I/O	-	AR7	E3	F4
I/O	-	AV4	D1	D3
I/O	P175	AN9	E4	B3
I/O	P176	AW1	D2	F5
I/O (D0, DIN)	P177	AP6	C2	E4
I/O, GCK6 (DOUT)	P178	AU3	D3	D4
CCLK	P179	AR5	D4	C4
VCC	P180	VCC*	VCC*	VCC*
O, TDO	P181	AN7	C4	E6
GND	P182	GND*	GND*	GND*
I/O (A0, $\overline{WS}$)	P183	AT4	B3	D5
I/O, GCK7 (A1)	P184	AV2	D5	A2
I/O	P185	AM8	B4	D6
I/O	P186	AL7	C5	A3
I/O	-	AT2	A4	E7
I/O	-	AN5	D6	C5
GND	-	GND*	GND*	GND*
I/O	-	AR3	B5	B4
I/O	-	AR1	C6	D7
I/O (CS1, A2)	P187	AK6	A5	C6
I/O (A3)	P188	AN3	D7	E8
I/O	-	AM6	B6	B5
I/O	-	AM2	A6	A5
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P189	AL3	D8	D8
I/O	P190	AH6	C7	C7
I/O	P191	AP2	B7	E9
I/O	P192	AK4	D9	A6
I/O	-	AN1	B8	B7
I/O	-	AK2	A8	D9
GND	-	GND*	GND*	GND*
I/O	P193	AG5	D10	E11
I/O	P194	AF6	C9	A9
I/O	P195	AL5	B9	C10
I/O	-	AJ3	C10	D11
GND	P196	GND*	GND*	GND*
I/O	P197	AH2	B10	B10
I/O	P198	AE5	A10	E12
I/O	P199	AM4	C11	C11
I/O	P200	AD6	D12	B11
VCC	P201	VCC*	VCC*	VCC*
I/O	-	AG3	B11	D12
I/O	-	AG1	C12	A11
GND	-	GND*	GND*	GND*
I/O	-	AF2	D13	C13
I/O	-	AJ5	B12	E14
I/O	-	AC5	C13	A13
I/O	-	AE1	A12	D14
I/O	-	AH4	D14	C14
I/O	-	AB6	B13	B14
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O (A4)	P202	AD2	C14	E15
I/O (A5)	P203	AB4	A13	D15
I/O	P205	AE3	B14	C15
I/O	P206	AC1	D15	A15
I/O (A21)	P207	AD4	C15	C16
I/O (A20)	P208	AA5	B15	E16
GND	-	GND*	GND*	GND*
I/O	-	AB2	A15	B17
I/O	-	AC3	C16	C17
I/O (A6)	P209	AA3	B16	E17
I/O (A7)	P210	Y6	A16	D17
GND	P211	GND*	GND*	GND*

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* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

Additional XC4052XL Package Pins

HQ240

GND Pins						
P204	P219	-	-	-	-	-

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Note: These pins may be N.C. for this device revision, however for compatability with other devices in this package, these pins should be tied to GND.

PG411

VCC Pins						
A3	A11	A21	A31	C39	D6	F36
J1	L39	W1	AA39	AJ1	AL39	AP4
AT34	AU1	AW9	AW19	AW29	AW37	-
GND Pins						
A9	A19	A29	A37	C1	D14	D20
D26	D34	F4	J39	LI	P4	P36
W39	Y4	Y36	AA1	AF4	AF36	AJ39
AL1	AP36	AT6	AT14	AT20	AT26	AU39
AW3	AW11	AW21	AW31	-	-	-

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BG432

VCC Pins						
A1	A11	A21	A31	C3	C29	D11
D21	L1	L4	L28	L31	AA1	AA4
AA28	AA31	AH11	AH21	AJ3	AJ29	AL1
AL11	AL21	AL31	-	-	-	-
GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1
AK2	AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30	-
N.C. Pins						
C8	-	-	-	-	-	-

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PG560

VCC Pins						
A4	A10	A16	A22	A26	A30	B2
B13	B19	B32	C3	C31	C32	D1
D33	E5	H1	K33	M1	N32	R2
T33	V1	W32	AA2	AB33	AD1	AF33
AK1	AK4	AK33	AL2	AL3	AL31	AM2
AM15	AM21	AM32	AN4	AN8	AN12	AN18
AN24	AN30	-	-	-	-	-
GND Pins						
A7	A12	A14	A18	A20	A24	A29
A32	B1	B6	B9	B15	B23	B27
B31	C2	E1	F32	G2	G33	J32
K1	L2	M33	P1	P33	R32	T1
V33	W2	Y1	Y33	AB1	AC32	AD33
AE2	AG1	AG32	AH2	AJ33	AL32	AM3
AM7	AM11	AM19	AM25	AM28	AM33	AN2
AN5	AN10	AN14	AN16	AN20	AN22	AN27
N.C. Pins						
A1	A8	A19	A23	A27	A28	A33
B8	B12	B16	B26	C8	C9	C12
C22	C26	D10	D13	D16	D18	D22
D25	E2	E10	E13	E21	E24	E32
E33	H2	H3	H5	H31	H32	J4
J31	K5	K29	L3	L31	M2	M5
M30	N4	N30	N31	T3	T5	T30
T32	U1	U2	U33	V32	Y4	Y29
AA1	AA33	AB4	AB30	AC1	AC2	AC33
AD4	AD5	AD29	AD30	AE4	AE30	AE31
AF1	AF2	AF31	AF32	AG2	AJ10	AJ13
AJ16	AJ18	AJ21	AJ24	AK9	AK13	AK18
AK24	AK25	AL8	AL9	AL12	AL16	AL22
AL26	AM8	AM9	AM12	AM23	AM26	AM27
AN1	AN23	AN33	-	-	-	-

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Pin Locations for XC4062XL Devices

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
VCC	P212	VCC*	VCC*	VCC*
I/O (A8)	P213	D17	Y2	A17
I/O (A9)	P214	A17	Y4	B18
I/O	-	C17	W5	C18
I/O	-	B17	Y6	E18
I/O	-	-	U3	D18
I/O	-	-	W3	A19
GND	-	GND*	GND*	GND*
I/O (A19)	P215	C18	W1	C19
I/O (A18)	P216	D18	U5	D19
I/O	P217	B18	W7	E19
I/O	P218	A19	U7	B20
I/O (A10)	P220	B19	V2	C20
I/O (A11)	P221	C19	V4	D20
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	D19	V6	A21
I/O	-	A20	R1	E20
I/O	-	B20	T6	B21
I/O	-	C20	R3	C21
I/O	-	B21	R5	D21
I/O	-	D20	T4	B22
GND	-	GND*	GND*	GND*
I/O	-	C21	P2	C23
I/O	-	A22	N1	E22
VCC	P222	VCC*	VCC*	VCC*
I/O	P223	B22	N3	B24
I/O	P224	C22	P4	D23
I/O	P225	B23	R7	C24
I/O	P226	A24	M2	A25

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
GND	P227	GND*	GND*	GND*
I/O	-	D22	M4	E23
I/O	-	C23	L3	B25
I/O	P228	B24	N5	D24
I/O	P229	C24	K2	C25
I/O	-	-	L5	B26
I/O	-	-	J1	E24
GND	-	GND*	GND*	GND*
I/O	-	D23	M6	E25
I/O	-	B25	K4	C27
I/O	P230	A26	J3	D26
I/O	P231	C25	J5	B28
I/O (A12)	P232	D24	H2	B29
I/O (A13)	P233	B26	G1	E26
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	A27	L7	C28
I/O	-	D25	K6	D27
I/O	-	C26	E1	B30
I/O	-	B27	H4	C29
I/O	-	A28	G5	E27
I/O	-	D26	F2	A31
GND	-	GND*	GND*	GND*
I/O	P234	C27	H6	D28
I/O	P235	B28	C3	C30
I/O	P236	D27	F4	D29
I/O	P237	B29	C5	E28
I/O (A14)	P238	C28	E3	D30
I/O GCK8 (A15)	P239	D28	E5	E29
VCC	P240	VCC*	VCC*	VCC*
GND	P1	GND*	GND*	GND*

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O, GCK1 (A16)	P2	D29	G7	B33
I/O (A17)	P3	C30	D4	F29
I/O	P4	E28	A5	E30
I/O	P5	E29	B4	D31
I/O, TDI	P6	D30	D6	F30
I/O, TCK	P7	D31	F8	C33
GND	-	GND*	GND*	GND*
I/O	-	F28	B6	G29
I/O	-	F29	E7	E31
I/O	-	E30	D8	D32
I/O	-	E31	G9	G30
I/O	-	G28	E9	F31
I/O	-	G29	A7	H29
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	F30	B8	H30
I/O	-	F31	C9	G31
I/O	P8	H28	G11	J29
I/O	P9	H29	D10	F33
I/O	P10	G30	E11	G32
I/O	P11	H30	A9	J30
GND	-	GND*	GND*	GND*
I/O	-	-	B10	H32
I/O	-	-	C11	J31
I/O	P12	J28	F12	K30
I/O	P13	J29	D12	H33
I/O	-	H31	A11	L29
I/O	-	J30	G15	K31
GND	P14	GND*	GND*	GND*
I/O	P15	K28	B12	L30
I/O	P16	K29	E13	K32
I/O, TMS	P17	K30	C13	J33
I/O	P18	K31	A13	M29
VCC	P19	VCC*	VCC*	VCC*
I/O	P20	L29	B14	L32
I/O	P21	L30	C15	M31
GND	-	GND*	GND*	GND*
I/O	-	M30	G17	N29
I/O	-	M28	F14	L33
I/O	-	M29	D16	M32
I/O	-	M31	D14	P29
I/O	-	N31	A15	P30
I/O	-	N28	C17	N33
GND	P22	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	N29	D18	P31
I/O	-	N30	B18	P32
I/O	-	P30	F16	R29
I/O	-	P28	G19	R30
I/O	P23	P29	E17	R31
I/O	P24	R31	E19	R33
GND	-	GND*	GND*	GND*
I/O	P25	R30	A19	T31
I/O	P26	R28	F18	T29
I/O	-	-	C19	T30
I/O	-	-	D20	T32
I/O	P27	R29	F20	U32
I/O	P28	T31	B20	U31
GND	P29	GND*	GND*	GND*
VCC	P30	VCC*	VCC*	VCC*
I/O	P31	T30	C21	U29
I/O	P32	T29	A21	U30
I/O	-	-	D22	U33
I/O	-	-	B22	V32
I/O	P33	U31	E23	V31
I/O	P34	U30	F22	V29
GND	-	GND*	GND*	GND*
I/O	P35	U28	C23	V30
I/O	P36	U29	F24	W33
I/O	-	V30	A23	W31

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O	-	V29	E25	W30
I/O	-	V28	G23	W29
I/O	-	W31	B24	Y32
VCC	-	VCC*	VCC*	VCC*
GND	P37	GND*	GND*	GND*
I/O	-	W30	D24	Y31
I/O	-	W29	C25	Y30
I/O	-	W28	D28	AA32
I/O	-	Y31	A27	AA31
I/O	-	Y30	E29	AA30
I/O	-	Y29	C27	AB32
GND	-	GND*	GND*	GND*
I/O	P38	Y28	G25	AA29
I/O	P39	AA30	D26	AB31
VCC	P40	VCC*	VCC*	VCC*
I/O	P41	AA29	F26	AC31
I/O	P42	AB31	B28	AB29
I/O	P43	AB30	D30	AD32
I/O	P44	AB29	A29	AC30
GND	P45	GND*	GND*	GND*
I/O	-	AB28	C29	AD31
I/O	-	AC30	G27	AE33
I/O	P46	AC29	F30	AC29
I/O	P47	AC28	B30	AE32
I/O	-	-	E31	AD30
I/O	-	-	C31	AE31
GND	-	GND*	GND*	GND*
I/O	-	AD31	F28	AG33
I/O	-	AD30	D32	AH33
I/O	P48	AD29	B32	AE29
I/O	P49	AD28	G31	AG31
I/O	P50	AE30	A33	AF30
I/O	P51	AE29	C33	AH32
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AF31	B34	AJ32
I/O	-	AE28	A35	AF29
I/O	-	AF30	E33	AH31
I/O	-	AF29	D34	AG30
I/O	P52	AG31	D36	AK32
I/O	P53	AF28	B36	AJ31
GND	-	GND*	GND*	GND*
I/O	-	AG30	F34	AG29
I/O	-	AG29	D38	AL33
I/O	P54	AH31	C37	AH30
I/O	P55	AG28	G37	AK31
I/O	P56	AH30	B38	AJ30
I/O, GCK2	P57	AJ30	F38	AH29
O (M1)	P58	AH29	A39	AK30
GND	P59	GND*	GND*	GND*
I (M0)	P60	AH28	E35	AJ29
VCC	P61	VCC*	VCC*	VCC*
I (M2)	P62	AJ28	G33	AN32
I/O, GCK3	P63	AK29	J37	AJ28
I/O (HDC)	P64	AH27	G35	AK29
I/O	P65	AK28	K36	AL30
I/O	P66	AJ27	C39	AK28
I/O	P67	AL28	K38	AM31
I/O (LDC)	P68	AH26	C41	AJ27
GND	-	GND*	GND*	GND*
I/O	-	AK27	D40	AN31
I/O	-	AJ26	L37	AL29
I/O	-	AL27	H36	AK27
I/O	-	AH25	M36	AL28
I/O	-	AK26	J35	AJ26
I/O	-	AL26	E41	AM30
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P69	AH24	F40	AM29
I/O	P70	AJ25	H38	AK26

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O	P71	AK25	N37	AL27
I/O	P72	AJ24	L35	AJ25
I/O	-	AH23	R35	AN29
I/O	-	AK24	G41	AN28
GND	-	GND*	GND*	GND*
I/O	-	-	H40	AM26
I/O	-	-	P38	AK24
I/O	P73	AL24	J39	AL25
I/O	P74	AH22	R37	AJ23
I/O	-	AJ23	J41	AN26
I/O	-	AK23	K40	AL24
GND	P75	GND*	GND*	GND*
I/O	P76	AJ22	L39	AK23
I/O	P77	AK22	M38	AN25
I/O	P78	AL22	T36	AJ22
I/O	P79	AJ21	M40	AL23
VCC	P80	VCC*	VCC*	VCC*
I/O	P81	AH20	N39	AM24
I/O	P82	AK21	N41	AK22
GND	-	GND*	GND*	GND*
I/O	-	AJ20	P40	AK21
I/O	-	AH19	T38	AM22
I/O	-	AK20	U35	AJ20
I/O	-	AJ19	U37	AL21
I/O	-	AL20	R39	AN21
I/O	-	AH18	R41	AK20
GND	P83	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AK19	V36	AL20
I/O	-	AJ18	U39	AJ19
I/O	P84	AL19	V38	AM20
I/O	P85	AK18	V40	AK19
I/O	P86	AH17	W37	AL19
I/O	P87	AJ17	W35	AN19
GND	-	GND*	GND*	GND*
I/O	-	-	W41	AJ18
I/O	-	-	Y36	AK18
I/O	-	AK17	W39	AL18
I/O	-	AL17	AB36	AM18
I/O	P88	AJ16	Y40	AK17
I/O ($\overline{\text{INIT}}$)	P89	AK16	Y38	AJ17
VCC	P90	VCC*	VCC*	VCC*
GND	P91	GND*	GND*	GND*
I/O	P92	AL16	AA39	AL17
I/O	P93	AH15	AB38	AM17
I/O	-	AL15	AB40	AN17
I/O	-	AJ15	AC37	AK16
I/O	-	-	AC39	AJ16
I/O	-	-	AC41	AL16
GND	-	GND*	GND*	GND*
I/O	P94	AK15	AD36	AM16
I/O	P95	AJ14	AC35	AL15
I/O	P96	AH14	AE37	AK15
I/O	P97	AK14	AD40	AJ15
I/O	-	AL13	AD38	AN15
I/O	-	AK13	AE39	AM14
VCC	-	VCC*	VCC*	VCC*
GND	P98	GND*	GND*	GND*
I/O	-	AJ13	AG41	AL14
I/O	-	AH13	AG39	AK14
I/O	-	AL12	AG37	AJ14
I/O	-	AK12	AE35	AN13
I/O	-	AJ12	AH38	AM13
I/O	-	AK11	AF38	AL13
GND	-	GND*	GND*	GND*
I/O	P99	AH12	AF36	AK12
I/O	P100	AJ11	AH40	AN11
VCC	P101	VCC*	VCC*	VCC*
I/O	P102	AL10	AJ41	AJ12
I/O	P103	AK10	AJ39	AL11

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O	P104	AJ10	AJ37	AK11
I/O	P105	AK9	AG35	AM10
GND	P106	GND*	GND*	GND*
I/O	-	AL8	AK40	AL10
I/O	-	AH10	AK38	AJ11
I/O	P107	AJ9	AL37	AN9
I/O	P108	AK8	AL39	AK10
I/O	-	-	AM38	AM9
I/O	-	-	AM40	AL9
GND	-	GND*	GND*	GND*
I/O	-	AJ8	AN41	AN7
I/O	-	AH9	AM36	AJ9
I/O	P109	AK7	AK36	AL7
I/O	P110	AL6	AU41	AK8
I/O	P111	AJ7	AN39	AN6
I/O	P112	AH8	AP40	AM6
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AK6	AR41	AJ8
I/O	-	AL5	AL35	AL6
I/O	P113	AH7	AV40	AK7
I/O	P114	AJ6	AN37	AM5
I/O	-	AK5	AT38	AM4
I/O	-	AL4	AP38	AJ7
GND	-	GND*	GND*	GND*
I/O	-	AH6	AT40	AL5
I/O	-	AJ5	AW39	AK6
I/O	P115	AK4	AP36	AN3
I/O	P116	AH5	AU37	AK5
I/O	P117	AK3	AR37	AJ6
I/O, GCK4	P118	AJ4	AU39	AL4
GND	P119	GND*	GND*	GND*
DONE	P120	AH4	AR35	AJ5
VCC	P121	VCC*	VCC*	VCC*
$\overline{\text{PROGRAM}}$	P122	AH3	AN35	AM1
I/O (D7)	P123	AJ2	AU35	AH5
I/O, GCK5	P124	AG4	AV38	AJ4
I/O	P125	AG3	AT34	AK3
I/O	P126	AH2	BA39	AH4
I/O	-	AH1	AU33	AL1
I/O	-	AF4	AY38	AG5
GND	-	GND*	GND*	GND*
I/O	P127	AF3	AV36	AJ3
I/O	P128	AG2	AR31	AK2
I/O	-	AG1	AR33	AG4
I/O	-	AE4	AV32	AH3
I/O	-	AE3	BA37	AF5
I/O	-	AF2	AY36	AJ2
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O (D6)	P129	AF1	AV34	AJ1
I/O	P130	AD4	BA35	AF4
I/O	P131	AD3	AU31	AG3
I/O	P132	AE2	AY34	AE5
I/O	-	AD2	AT30	AH1
I/O	-	AC4	AW33	AF3
GND	-	GND*	GND*	GND*
I/O	-	-	BA33	AF1
I/O	-	-	AV30	AD4
I/O	P133	AC3	AY32	AE3
I/O	P134	AD1	AU29	AC5
I/O	-	AC2	AW31	AE1
I/O	-	AB4	BA31	AD3
GND	P135	GND*	GND*	GND*
I/O	P136	AB3	AR27	AC4
I/O	P137	AB2	AT28	AD2
I/O	P138	AB1	AY30	AB5
I/O	P139	AA3	AW29	AC3
VCC	P140	VCC*	VCC*	VCC*
I/O (D5)	P141	AA2	BA29	AA5

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O ($\overline{CS0}$)	P142	Y2	AY28	AB3
GND	P143	GND*	GND*	GND*
I/O	-	Y4	AR25	AB2
I/O	-	Y3	AV28	AA4
I/O	-	Y1	AW27	AA3
I/O	-	W1	AT26	Y5
I/O	-	W4	AV26	Y3
I/O	-	W3	BA27	Y2
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	W2	AW25	W5
I/O	-	V2	AV24	W4
I/O	-	V4	AU25	W3
I/O	-	V3	AR23	W1
I/O	P144	U1	AT24	V3
I/O	P145	U2	AY24	V5
GND	-	GND*	GND*	GND*
I/O	P146	U4	BA23	V4
I/O	P147	U3	AU23	V2
I/O	-	-	AW23	U2
I/O	-	-	AV20	U1
I/O (D4)	P148	T1	AY22	U5
I/O	P149	T2	AV22	U4
VCC	P150	VCC*	VCC*	VCC*
GND	P151	GND*	GND*	GND*
I/O (D3)	P152	T3	AW21	U3
I/O ($\overline{RS}$)	P153	R1	BA21	T2
I/O	-	-	AU19	T3
I/O	-	-	AY20	T5
I/O	P154	R2	AU17	T4
I/O	P155	R4	AW19	R1
GND	-	GND*	GND*	GND*
I/O	P156	R3	BA19	R3
I/O	P157	P2	AT16	R4
I/O	-	P3	AR19	R5
I/O	-	P4	AV14	P2
I/O	-	N1	AY18	P3
I/O	-	N2	AV18	P4
VCC	-	VCC*	VCC*	VCC*
GND	P158	GND*	GND*	GND*
I/O	-	N3	AT18	N1
I/O	-	N4	AW17	P5
I/O	-	M1	AR15	N2
I/O	-	M2	BA15	N3
I/O	-	M3	AT14	N5
I/O	-	M4	AR17	M3
GND	-	GND*	GND*	GND*
I/O (D2)	P159	L2	AW15	M4
I/O	P160	L3	AV16	L1
VCC	P161	VCC*	VCC*	VCC*
I/O	P162	K1	AY14	K2
I/O	P163	K2	BA13	L4
I/O	P164	K3	AU13	J1
I/O	P165	K4	AW13	K3
GND	P166	GND*	GND*	GND*
I/O	-	J2	AY12	L5
I/O	-	J3	BA11	J2
I/O	P167	J4	AV12	K4
I/O	P168	H1	AT12	J3
I/O	-	-	AW11	H2
I/O	-	-	AY10	K5
GND	-	GND*	GND*	GND*
I/O	P169	H2	BA9	G1
I/O	P170	H3	AU11	F1
I/O	P171	H4	AW9	J5
I/O	P172	G2	AV10	G3
I/O	-	G3	AY8	H4
I/O	-	F1	BA7	F2
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O (D1)	P173	G4	AV8	F3
I/O (RCLK, RDY/BUSY)	P174	F2	AY6	G4
I/O	-	F3	AR11	D2
I/O	-	E1	AT8	E3
I/O	-	F4	AU9	G5
I/O	-	E2	AW5	C1
GND	-	GND*	GND*	GND*
I/O	-	E3	AY4	F4
I/O	-	D1	BA5	D3
I/O	P175	E4	AV4	B3
I/O	P176	D2	AR9	F5
I/O (D0, DIN)	P177	C2	AU5	E4
I/O, GCK6 (DOUT)	P178	D3	AV6	D4
CCLK	P179	D4	AR5	C4
VCC	P180	VCC*	VCC*	VCC*
O, TDO	P181	C4	AN7	E6
GND	P182	GND*	GND*	GND*
I/O (A0, $\overline{WS}$)	P183	B3	AR7	D5
I/O, GCK7 (A1)	P184	D5	AW3	A2
I/O	P185	B4	AU3	D6
I/O	P186	C5	AW1	A3
I/O	-	A4	AP6	E7
I/O	-	D6	AV2	C5
GND	-	GND*	GND*	GND*
I/O	-	B5	AT4	B4
I/O	-	C6	AN5	D7
I/O (CS1, A2)	P187	A5	AU1	C6
I/O (A3)	P188	D7	AM6	E8
I/O	-	B6	AT2	B5
I/O	-	A6	AL7	A5
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P189	D8	AR1	D8
I/O	P190	C7	AP2	C7
I/O	P191	B7	AM4	E9
I/O	P192	D9	AN3	A6
I/O	-	B8	AL5	B7
I/O	-	A8	AK6	D9
GND	-	GND*	GND*	GND*
I/O	-	-	AN1	D10
I/O	-	-	AJ5	C9
I/O	P193	D10	AM2	E11
I/O	P194	C9	AH4	A9
I/O	P195	B9	AL3	C10
I/O	-	C10	AK4	D11
GND	P196	GND*	GND*	GND*
I/O	P197	B10	AG7	B10
I/O	P198	A10	AG5	E12
I/O	P199	C11	AK2	C11
I/O	P200	D12	AJ3	B11
VCC	P201	VCC*	VCC*	VCC*
I/O	-	B11	AJ1	D12
I/O	-	C12	AF6	A11
GND	-	GND*	GND*	GND*
I/O	-	D13	AH2	C13
I/O	-	B12	AF4	E14
I/O	-	C13	AE7	A13
I/O	-	A12	AE5	D14
I/O	-	D14	AG3	C14
I/O	-	B13	AG1	B14
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O (A4)	P202	C14	AD6	E15
I/O (A5)	P203	A13	AD4	D15
I/O	P205	B14	AE3	C15
I/O	P206	D15	AC5	A15
I/O (A21)	P207	C15	AD2	C16
I/O (A20)	P208	B15	AC7	E16
GND	-	GND*	GND*	GND*
I/O	-	-	AC1	D16

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O	-	-	AC3	B16
I/O	-	A15	AB6	B17
I/O	-	C16	AB2	C17
I/O (A6)	P209	B16	AB4	E17
I/O (A7)	P210	A16	AA3	D17
GND	P211	GND*	GND*	GND*

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* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

Additional XC4062XL Package Pins

HQ240

GND Pins					
P204	P219	-	-	-	-

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Note: These pins may be N.C. for this device revision, however for compatability with other devices in this package, these pins should be tied to GND.

BG432

VCC Pins						
A1	A11	A21	A31	C3	C29	D11
D21	L1	L4	L28	L31	AA1	AA4
AA28	AA31	AH11	AH21	AJ3	AJ29	AL1
AL11	AL21	AL31	-	-	-	-
GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1
AK2	AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30	-
N.C. Pins						
C8	-	-	-	-	-	-

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PG475

VCC Pins					
A37	B2	B16	B26	B40	D2
E21	F6	F36	G13	G29	N7
N35	T2	T40	AA1	AA5	AA37
AA41	AF2	AF40	AJ7	AJ35	AR13
AR29	AT6	AT22	AT36	AU21	AW37
AW41	AY2	AY16	AY26	AY40	BA3
GND Pins					
A3	C1	C7	G3	L1	P6
U1	A17	A25	A41	AA7	AE1
AH6	AL1	AR3	AW7	BA1	C35
E15	E27	F10	F32	G21	G39
L41	P36	U41	AA35	AE41	AH36
AL41	AR21	AR39	AT10	AT20	AT32
AU15	AU27	AW35	BA17	BA25	BA41
E37	E39	A31	J7	AP4	AU7

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BG560

VCC Pins						
A4	A10	A16	A22	A26	A30	B2
B13	B19	B32	C3	C31	C32	D1
D33	E5	H1	K33	M1	N32	R2
T33	V1	W32	AA2	AB33	AD1	AF33
AK1	AK4	AK33	AL2	AL3	AL31	AM2
AM15	AM21	AM32	AN4	AN8	AN12	AN18
AN24	AN30	-	-	-	-	-
GND Pins						
A7	A12	A14	A18	A20	A24	A29
A32	B1	B6	B9	B15	B23	B27
B31	C2	E1	F32	G2	G33	J32
K1	L2	M33	P1	P33	R32	T1
V33	W2	Y1	Y33	AB1	AC32	AD33
AE2	AG1	AG32	AH2	AJ33	AL32	AM3
AM11	AM19	AM25	AM28	AM33	AM7	AN2
AN5	AN10	AN14	AN16	AN20	AN22	AN27
N.C. Pins						
A1	A8	A23	A27	A28	A33	B8
B12	C8	C12	C22	C26	D13	D22
D25	E2	E10	E13	E21	E32	E33
H3	H5	H31	J4	K29	L3	L31
M2	M5	M30	N4	N30	N31	Y4
Y29	AA1	AA33	AB4	AB30	AC1	AC2
AC33	AD5	AD29	AE4	AE30	AF2	AF31
AF32	AG2	AJ10	AJ13	AJ21	AJ24	AK9
AK13	AK25	AL8	AL12	AL22	AL26	AM8
AM12	AM23	AM27	AN1	AN23	AN33	-

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Pin Locations for XC4085XL Devices

XC4085XL Pad Name	BG560	PG559
VCC	VCC*	VCC*
I/O (A8)	A17	AB6
I/O (A9)	B18	AB4
I/O	C18	AA7
I/O	E18	AC1
I/O	D18	AA5
I/O	A19	AA3
GND	GND*	GND*
I/O (A19)	C19	Y8
I/O (A18)	D19	AB2
I/O	E19	Y6
I/O	B20	AA1
I/O (A10)	C20	Y4
I/O (A11)	D20	W7
VCC	VCC*	VCC*

XC4085XL Pad Name	BG560	PG559
GND	GND*	GND*
I/O	A21	W5
I/O	E20	V6
I/O	B21	V4
I/O	C21	Y2
I/O	D21	U3
I/O	B22	U7
I/O	E21	V2
I/O	C22	U5
GND	GND*	GND*
I/O	D22	T4
I/O	A23	U1
I/O	C23	R3
I/O	E22	R5
VCC	VCC*	VCC*

XC4085XL Pad Name	BG560	PG559
I/O	B24	T8
I/O	D23	T2
I/O	C24	P4
I/O	A25	R7
GND	GND*	GND*
I/O	E23	N3
I/O	B25	R1
I/O	D24	N5
I/O	C25	P2
I/O	B26	M4
I/O	E24	L1
I/O	C26	L3
I/O	D25	P8
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	A27	N7
I/O	A28	K2
I/O	E25	M6
I/O	C27	J1
I/O	D26	L5
I/O	B28	H2
I/O (A12)	B29	K4
I/O (A13)	E26	J3
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	C28	L7
I/O	D27	J5
I/O	B30	G1
I/O	C29	H4
I/O	E27	F2
I/O	A31	G5
GND	GND*	GND*
I/O	D28	H6
I/O	C30	K8
I/O	D29	D2
I/O	E28	J7
I/O (A14)	D30	F4
I/O, GCK8 (A15)	E29	E3
VCC	VCC*	VCC*
GND	GND*	GND*
I/O, GCK1 (A16)	B33	C1
I/O (A17)	F29	C3
I/O	E30	F6
I/O	D31	A3
I/O (TDI)	F30	H8
I/O (TCK)	C33	D4
GND	GND*	GND*
I/O	G29	D6
I/O	E31	C5
I/O	D32	E7
I/O	G30	B4
I/O	F31	H10
I/O	H29	G9
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	E32	F8
I/O	E33	D8
I/O	H30	B6
I/O	G31	E9
I/O	J29	A7
I/O	F33	G11
I/O	G32	H14
I/O	J30	F12
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	H31	G13
I/O	K29	E11
I/O	H32	B8
I/O	J31	D10
I/O	K30	A9

XC4085XL Pad Name	BG560	PG559
I/O	H33	G15
I/O	L29	B10
I/O	K31	H16
GND	GND*	GND*
I/O	L30	C9
I/O	K32	E13
I/O (TMS)	J33	A11
I/O	M29	D12
VCC	VCC*	VCC*
I/O	L31	C11
I/O	M30	B14
I/O	L32	G17
I/O	M31	E15
GND	GND*	GND*
I/O	N29	D14
I/O	L33	A15
I/O	N30	C13
I/O	N31	B16
I/O	M32	E17
I/O	P29	F18
I/O	P30	A17
I/O	N33	G19
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	P31	D16
I/O	P32	C15
I/O	R29	B18
I/O	R30	H20
I/O	R31	B20
I/O	R33	E19
GND	GND*	GND*
I/O	T31	D18
I/O	T29	F20
I/O	T30	G21
I/O	T32	C17
I/O	U32	D20
I/O	U31	E21
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	U29	C21
I/O	U30	F22
I/O	U33	A21
I/O	V32	D22
I/O	V31	B22
I/O	V29	G23
GND	GND*	GND*
I/O	V30	E23
I/O	W33	C23
I/O	W31	A23
I/O	W30	D24
I/O	W29	B24
I/O	Y32	H24
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	Y31	F24
I/O	Y30	E25
I/O	AA33	B26
I/O	Y29	D26
I/O	AA32	A27
I/O	AA31	G25
I/O	AA30	B28
I/O	AB32	C27
GND	GND*	GND*
I/O	AA29	F26
I/O	AB31	E27
I/O	AB30	A29
I/O	AC33	D28
VCC	VCC*	VCC*
I/O	AC31	G27
I/O	AB29	B30

XC4085XL Pad Name	BG560	PG559
I/O	AD32	C29
I/O	AC30	E29
GND	GND*	GND*
I/O	AD31	D30
I/O	AE33	A33
I/O	AC29	C31
I/O	AE32	B34
I/O	AD30	H28
I/O	AE31	A35
I/O	AF32	G29
I/O	AD29	E31
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	AF31	D32
I/O	AE30	C35
I/O	AG33	C33
I/O	AH33	B36
I/O	AE29	H30
I/O	AG31	A37
I/O	AF30	G31
I/O	AH32	F32
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	AJ32	E33
I/O	AF29	D34
I/O	AH31	B38
I/O	AG30	G33
I/O	AK32	A41
I/O	AJ31	E35
GND	GND*	GND*
I/O	AG29	D36
I/O	AL33	F36
I/O	AH30	G35
I/O	AK31	H34
I/O	AJ30	B40
I/O, GCK2	AH29	E37
O (M1)	AK30	D38
GND	GND*	GND*
I (M0)	AJ29	C39
VCC	VCC*	VCC*
I (M2)	AN32	H36
I/O, GCK3	AJ28	F38
I/O (HDC)	AK29	C41
I/O	AL30	D40
I/O	AK28	B42
I/O	AM31	J37
I/O ($\overline{\text{LDC}}$)	AJ27	K36
GND	GND*	GND*
I/O	AN31	H38
I/O	AL29	D42
I/O	AK27	G39
I/O	AL28	C43
I/O	AJ26	F40
I/O	AM30	E41
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	AM29	L37
I/O	AK26	J39
I/O	AL27	F42
I/O	AJ25	H40
I/O	AN29	G43
I/O	AN28	J41
I/O	AK25	H42
I/O	AL26	N37
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	AJ24	P36
I/O	AM27	M38
I/O	AM26	J43
I/O	AK24	L39

XC4085XL Pad Name	BG560	PG559
I/O	AL25	K42
I/O	AJ23	K40
I/O	AN26	L43
I/O	AL24	L41
GND	GND*	GND*
I/O	AK23	R37
I/O	AN25	P42
I/O	AJ22	T36
I/O	AL23	N39
VCC	VCC*	VCC*
I/O	AM24	M40
I/O	AK22	R43
I/O	AM23	N41
I/O	AJ21	R39
GND	GND*	GND*
I/O	AL22	U37
I/O	AN23	T42
I/O	AK21	P40
I/O	AM22	U43
I/O	AJ20	R41
I/O	AL21	V42
I/O	AN21	U39
I/O	AK20	V38
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	AL20	W37
I/O	AJ19	T40
I/O	AM20	Y42
I/O	AK19	U41
I/O	AL19	Y36
I/O	AN19	V40
GND	GND*	GND*
I/O	AJ18	W39
I/O	AK18	AA43
I/O	AL18	Y38
I/O	AM18	Y40
I/O	AK17	AA37
I/O ($\overline{\text{INIT}}$)	AJ17	AA39
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	AL17	AA41
I/O	AM17	AB38
I/O	AN17	AB42
I/O	AK16	AB40
I/O	AJ16	AC37
I/O	AL16	AC39
GND	GND*	GND*
I/O	AM16	AD36
I/O	AL15	AC41
I/O	AK15	AD38
I/O	AJ15	AC43
I/O	AN15	AD40
I/O	AM14	AE39
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	AL14	AE37
I/O	AK14	AF40
I/O	AJ14	AD42
I/O	AN13	AF42
I/O	AM13	AF38
I/O	AL13	AG39
I/O	AK13	AG43
I/O	AJ13	AG37
GND	GND*	GND*
I/O	AM12	AH40
I/O	AL12	AJ41
I/O	AK12	AG41
I/O	AN11	AK40
VCC	VCC*	VCC*
I/O	AJ12	AJ39

XC4085XL Pad Name	BG560	PG559
I/O	AL11	AH42
I/O	AK11	AH36
I/O	AM10	AL39
GND	GND*	GND*
I/O	AL10	AJ37
I/O	AJ11	AJ43
I/O	AN9	AM40
I/O	AK10	AK42
I/O	AM9	AN41
I/O	AL9	AL41
I/O	AJ10	AR41
I/O	AM8	AK36
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	AK9	AL37
I/O	AL8	AN43
I/O	AN7	AM38
I/O	AJ9	AP42
I/O	AL7	AN39
I/O	AK8	AR43
I/O	AN6	AP40
I/O	AM6	AT40
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	AJ8	AN37
I.O	AL6	AR39
I/O	AK7	AT42
I/O	AM5	BA43
I/O	AM4	AU43
I/O	AJ7	AU39
GND	GND*	GND*
I/O	AL5	AT38
I/O	AK6	AP36
I/O	AN3	AR37
I/O	AK5	AV42
I/O	AJ6	AV40
I/O, GCK4	AL4	AW41
GND	GND*	GND*
DONE	AJ5	AY42
VCC	VCC*	VCC*
$\overline{\text{PROGRAM}}$	AM1	BB42
I/O (D7)	AH5	BC41
I/O, GCK5	AJ4	AV38
I/O	AK3	BA39
I/O	AH4	AT36
I/O	AL1	BB40
I/O	AG5	AY40
GND	GND*	GND*
I/O	AJ3	BA41
I/O	AK2	BB38
I/O	AG4	AY38
I/O	AH3	BC37
I/O	AF5	AW37
I/O	AJ2	AT34
VCC	VCC*	VCC*
GND	GND*	GND*
I/O (D6)	AJ1	AU35
I/O	AF4	AV36
I/O	AG3	BB36
I/O	AE5	AY36
I/O	AH1	BC35
I/O	AF3	AW35
I/O	AE4	AU33
I/O	AG2	AT30
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	AD5	AV32
I/O	AF2	AU31
I/O	AF1	AW33
I/O	AD4	BB34

XC4085XL Pad Name	BG560	PG559
I/O	AE3	AY34
I/O	AC5	BC33
I/O	AE1	AU29
I/O	AD3	AT28
GND	GND*	GND*
I/O	AC4	BA35
I/O	AD2	BB30
I/O	AB5	AW31
I/O	AC3	AY32
VCC	VCC*	VCC*
I/O	AB4	BA33
I/O	AC1	AU27
I/O (D5)	AA5	BC29
I/O ($\overline{\text{CS0}}$)	AB3	AW29
GND	GND*	GND*
I/O	AB2	AY30
I/O	AA4	BA31
I/O	AA3	BB28
I/O	Y5	AW27
I/O	AA1	BC27
I/O	Y4	AV26
I/O	Y3	AU25
I/O	Y2	AY28
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	W5	BA29
I/O	W4	AT24
I/O	W3	BB26
I/O	W1	AW25
I/O	V3	BB24
I/O	V5	AY26
GND	GND*	GND*
I/O	V4	AV24
I/O	V2	AU23
I/O	U2	BA27
I/O	U1	BC23
I/O (D4)	U5	AY24
I/O	U4	AW23
VCC	VCC*	VCC*
GND	GND*	GND*
I/O (D3)	U3	BA23
I/O ($\overline{\text{RS}}$)	T2	AV22
I/O	T3	AY22
I/O	T5	BB22
I/O	T4	AU21
I/O	R1	AW21
GND	GND*	GND*
I/O	R3	BA21
I/O	R4	BC21
I/O	R5	AY20
I/O	P2	BB20
I/O	P3	AT20
I/O	P4	AV20
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	N1	AW19
I/O	P5	AY18
I/O	N2	BB18
I/O	N3	AU19
I/O	N4	BC17
I/O	M2	BA17
I/O	N5	AV18
I/O	M3	AW17
GND	GND*	GND*
I/O (D2)	M4	AY16
I/O	L1	BB16
I/O	L3	AU17
I/O	M5	BA15
VCC	VCC*	VCC*
I/O	K2	AW15

XC4085XL Pad Name	BG560	PG559
I/O	L4	BC15
I/O	J1	AY14
I/O	K3	BA13
GND	GND*	GND*
I/O	L5	AT16
I/O	J2	BB14
I/O	K4	AU15
I/O	J3	BC11
I/O	H2	AW13
I/O	K5	BB10
I/O	H3	AY12
I/O	J4	BA11
GND	GND*	GND*
VCC	VCC*	VCC*
I/O	G1	AT14
I/O	F1	AU13
I/O	J5	AV12
I/O	G3	BC9
I/O	H4	AW11
I/O	F2	BB8
I/O	E2	AY10
I/O	H5	AU11
GND	GND*	GND*
VCC	VCC*	VCC*
I/O (D1)	F3	BA9
I/O ($\overline{RCLK}$ $\overline{RDY/BUSY}$)	G4	AW9
I/O	D2	BC7
I/O	E3	AY8
I/O	G5	AV8
I/O	C1	AT10
GND	GND*	GND*
I/O	F4	AU9
I/O	D3	BB6
I/O	B3	AW7
I/O	F5	BC3
I/O (D0, DIN)	E4	AY6
I/O, GCK6 (DOUT)	D4	BB4
CCLK	C4	BA5
VCC	VCC*	VCC*
O, TDO	E6	BA3
GND	GND*	GND*
I/O (A0, $\overline{WS}$)	D5	AT8
I/O, GCK7 (A1)	A2	AV6
I/O	D6	BB2
I/O	A3	AY4
I/O	E7	AR7
I/O	C5	AP8
GND	GND*	GND*
I/O	B4	AT6
I/O	D7	AY2
I/O (CS1, A2)	C6	AU5
I/O (A3)	E8	BA1
I/O	B5	AV4
I/O	A5	AW3
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	D8	AN7
I/O	C7	AR5
I/O	E9	AV2
I/O	A6	AT4
I/O	B7	AU1
I/O	D9	AR3
I/O	C8	AT2
I/O	E10	AL7
VCC	VCC*	VCC*
GND	GND*	GND*
I/O	B8	AK8
I/O	A8	AM6
I/O	D10	AN5

XC4085XL Pad Name	BG560	PG559
I/O	C9	AR1
I/O	E11	AP4
I/O	A9	AN3
I/O	C10	AP2
I/O	D11	AJ7
GND	GND*	GND*
I/O	B10	AH8
I/O	E12	AL5
I/O	C11	AN1
I/O	B11	AM4
VCC	VCC*	VCC*
I/O	D12	AL3
I/O	A11	AJ5
I/O	E13	AK2
I/O	C12	AG7
GND	GND*	GND*
I/O	B12	AK4
I/O	D13	AJ3
I/O	C13	AG5
I/O	E14	AJ1
I/O	A13	AF6
I/O	D14	AH2
I/O	C14	AE7
I/O	B14	AH4
GND	GND*	GND*
VCC	VCC*	VCC*
I/O (A4)	E15	AG3
I/O (A5)	D15	AD8
I/O	C15	AG1
I/O	A15	AF4
I/O (A21)	C16	AE5
I/O (A20)	E16	AD6
GND	GND*	GND*
I/O	D16	AD4
I/O	B16	AF2
I/O	B17	AC7
I/O	C17	AD2
I/O (A6)	E17	AC5
I/O (A7)	D17	AC3
GND	GND*	GND*

6/13/97

Additional XC4085XL Package Pins

BG560

VCC Pins						
A4	A10	A16	A22	A26	A30	B2
B13	B19	B32	C3	C31	C32	D1
D33	E5	H1	K33	M1	N32	R2
T33	V1	W32	AA2	AB33	AD1	AF33
AK1	AK4	AK33	AL2	AL3	AL31	AM2
AM15	AM21	AM32	AN4	AN8	AN12	AN18
AN24	AN30	-	-	-	-	-
GND Pins						
A7	A12	A14	A18	A20	A24	A29
A32	B1	B6	B9	B15	B23	B27
B31	C2	E1	F32	G2	G33	J32
K1	L2	M33	P1	P33	R32	T1
V33	W2	Y1	Y33	AB1	AC32	AD33
AE2	AG1	AG32	AH2	AJ33	AL32	AM3
AM11	AM19	AM25	AM28	AM33	AM7	AN2
AN5	AN10	AN14	AN16	AN20	AN22	AN27
N.C. Pins						
A1	A33	AC2	AN1	AN33	-	-

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PG559

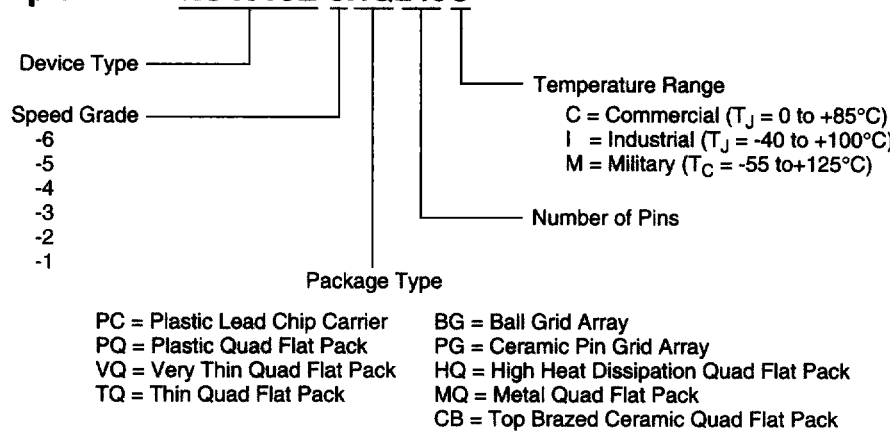
VCC Pins						
A13	A31	A43	B2	C7	C19	C25
C37	F14	F30	G3	G7	G37	G41
H12	H18	H26	H32	M8	M36	N1
N43	P6	P38	V8	V36	W3	W41
AE3	AE41	AF8	AF36	AK6	AK38	AL1
AL43	AM8	AM36	AT12	AT18	AT26	AT32
AU3	AU7	AU37	AU41	AV14	AV30	BA7
BA19	BA25	BA37	BC1	BC13	BC31	BC43
GND Pins						
A5	A19	A25	A39	B12	B32	E1
E5	E39	E43	F10	F16	F28	F34
H22	K6	K38	M2	M42	T6	T38
W1	W43	AB8	AB36	AE1	AE43	AH6
AH38	AM2	AM42	AP6	AP38	AT22	AV10
AV16	AV28	AV34	AW1	AW5	AW39	AW43
BB12	BB32	BC5	BC19	BC25	BC39	-

5/8/97

* Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
† = E only, †† = XL only

Ordering Information

Example: **XC4013E-3HQ240C**



X9020

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