



# CMOS Generic 20-Pin Programmable Logic Device

## Features

- **Fast**
  - Commercial:  $t_{PD} = 12 \text{ ns}$ ,  $t_{CO} = 10 \text{ ns}$ ,  $t_S = 10 \text{ ns}$
  - Military/Industrial:  $t_{PD} = 15 \text{ ns}$ ,  $t_{CO} = 12 \text{ ns}$ ,  $t_S = 12 \text{ ns}$
- **Low power**
  - $I_{CC}$  max. of 110 mA
- **Commercial, industrial, and military temperature range**
- **User-programmable output cells**
  - Selectable for registered or combinatorial operation
  - Output polarity control
  - Output enable source selectable from pin 11 or product term

- **Generic architecture to replace standard logic functions including: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8**
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - Uses proven EPROM technology
  - Fully AC and DC tested
  - Security feature prevents logic pattern duplication
  - >2000V input protection for electrostatic discharge

## Functional Description

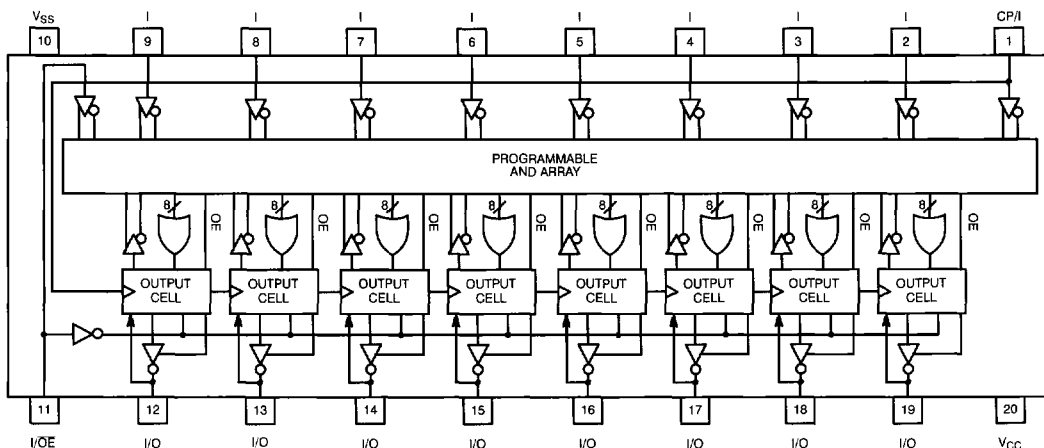
Cypress PLD devices are high-speed electrically programmable logic devices. These devices utilize the sum-of-products (AND-OR) structure, providing users with the ability to program custom logic functions for unique requirements.

In an unprogrammed state, the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PLD C18G8 uses an advanced 0.8-micron CMOS technology and a proven EPROM cell as the programmable

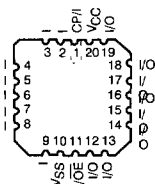
4  
PLDS

Logic Block Diagram, DIP and SOJ Pinout



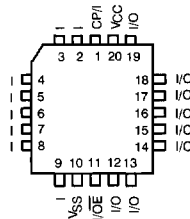
## Pin Configurations

LCC Top View



18G8-3

PLCC Top View



18G8-2

18G8-1

Selection Guide

| Generic Part Number | I <sub>CC</sub> (mA) |         | t <sub>PD</sub> (ns) |         | t <sub>s</sub> |         | t <sub>CO</sub> |         |
|---------------------|----------------------|---------|----------------------|---------|----------------|---------|-----------------|---------|
|                     | Com'l                | Mil/Ind | Com'l                | Mil/Ind | Com'l          | Mil/Ind | Com'l           | Mil/Ind |
| 18G8-12             | 90                   |         | 12                   |         | 10             |         | 10              |         |
| 18G8-15             | 90                   | 110     | 15                   | 15      | 12             | 12      | 12              | 12      |
| 18G8-15L            | 70                   |         | 15                   |         | 12             |         | 12              |         |
| 18G8-20             |                      | 110     |                      | 20      |                | 15      |                 | 15      |

Functional Description (continued)

element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit, reducing the customer's need to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

18G8 Functional Description

The PLDC18G8 is a generic 20-pin device that can be programmed to logic functions which include but are not limited to: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8. Thus, the PLDC18G8 provides significant design, inventory, and programming flexibility over dedicated 20-pin devices. It is executed in a 20-pin, 300-mil molded DIP and a 300-mil windowed cerDIP. It provides up to 18 inputs and 8 outputs. When the windowed cerDIP is exposed to UV light, the 18G8 is erased and can then be reprogrammed.

The programmable output cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with registered or combinatorial outputs, active HIGH or active LOW outputs, and product term or Pin 11 generated output enables. Four architecture bits determine the

configurations as shown in the Configuration Table. A total of sixteen different configurations are possible. The default or unprogrammed state is registered/active LOW/Pin 11 OE. The entire programmable output cell is shown in Figure 1.

Architecture bit C1 controls the registered/combinatorial option. In either combinatorial or registered configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In either registered or combinatorial configuration, the output of the register may be fed back to the array. This allows the creation of state machines by providing storage and feedback of the current system state. The register is clocked by the signal from Pin 1. The register is initialized upon power-up to Q output LOW and Q output HIGH.

In both the combinatorial and registered configurations, the source of the output enable signal can be individually chosen with architecture bit C2. The OE signal may be generated within the array or from the external OE (Pin 11). Pin 11 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for output polarity. The output can be either active HIGH or active LOW. This option is controlled by architecture bit C0.

Along with this increase in functional density, the Cypress PLDC18G8 provides lower-power operation through the use of CMOS technology and increased testability with a register preload feature.

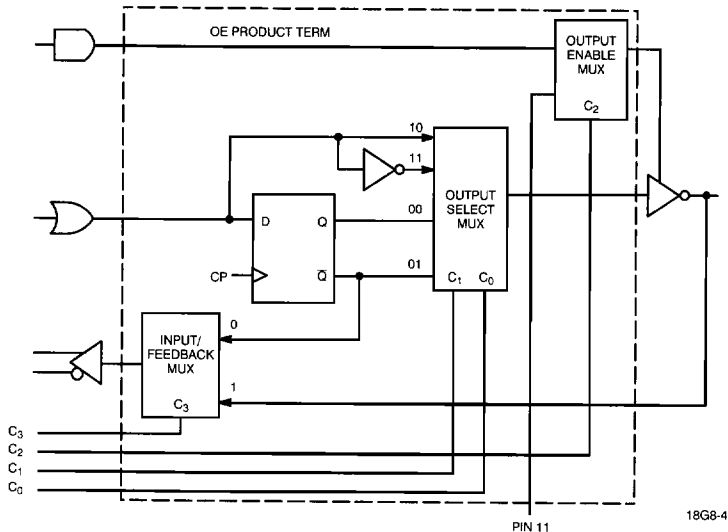


Figure 1. Programmable Output Cell

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

|   |                  |
|---|------------------|
| Storage Temperature                           | - 65°C to +150°C |
| Ambient Temperature with Power Applied        | - 55°C to +125°C |
| Supply Voltage to Ground Potential            | - 0.5V to +7.0V  |
| DC Voltage Applied to Outputs in High Z State | - 0.5V to +7.0V  |
| DC Input Voltage                              | - 3.0V to +7.0V  |
| Output Current into Outputs (LOW)             | 24 mA            |
| DC Programming Voltage                        | 13.0V            |

|  |         |
|--|---------|
| Static Discharge Voltage (per MIL-STD-883 Method 3015) | >2001V  |
| Latch-Up Current                                       | >200 mA |

### Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ±5%          |
| Industrial              | - 40°C to +85°C     | 5V ±10%         |
| Military <sup>[1]</sup> | - 55°C to +125°C    | 5V ±10%         |

### Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)

| Parameters      | Description                  | Test Conditions  |                            |                     | Min. | Max. | Units |
|-----------------|------------------------------|--|----------------------------|---------------------|------|------|-------|
| V <sub>OH</sub> | Output HIGH Voltage          | V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OH</sub> = - 3.2 mA | Commercial          | 2.4  |      | V     |
|                 |                              |  | I <sub>OH</sub> = - 2 mA   | Military/Industrial |      |      |       |
| V <sub>OL</sub> | Output LOW Voltage           | V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OL</sub> = 24 mA    | Commercial          |      | 0.5  | V     |
|                 |                              |  | I <sub>OL</sub> = 12 mA    | Military/Industrial |      |      |       |
| V <sub>IH</sub> | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[2]</sup>          |                            |                     | 2.0  |      | V     |
| V <sub>IL</sub> | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[2]</sup>           |                            |                     |      | 0.8  | V     |
| I <sub>IX</sub> | Input Leakage Current        | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                          |                            |                     | - 10 | +10  | μA    |
| V <sub>PP</sub> |                              | Programming Voltage @ I <sub>PP</sub> = 50 mA Max.                           |                            |                     | 12.0 | 13.0 | V     |
| I <sub>SC</sub> | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[3]</sup>               |                            |                     | - 30 | - 90 | mA    |
| I <sub>CC</sub> | Power Supply Current         | V <sub>IN</sub> = 0, V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA         | Commercial -15L            |                     |      | 70   | mA    |
|                 |                              |  | Commercial -12, -15        |                     |      |      |       |
|                 |                              |  | Military/Industrial        |                     |      |      |       |
| I <sub>OZ</sub> | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> |                            |                     | - 40 | +40  | μA    |

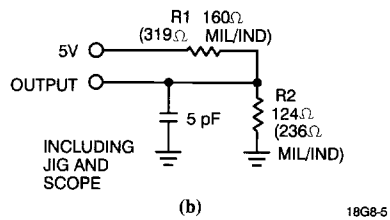
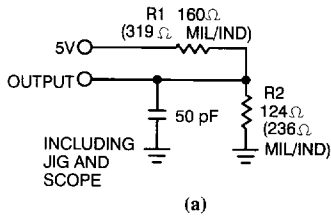
### Capacitance<sup>[4]</sup>

| Parameters       | Description        | Test Conditions                                | Max. | Units |
|------------------|--------------------|--|------|-------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz               | 10   | pF    |
| C <sub>OUT</sub> | Output Capacitance | V <sub>IN</sub> = 2.0V, V <sub>CC</sub> = 5.0V | 10   | pF    |

#### Notes:

- T<sub>A</sub> is the "instant on" case temperature.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.

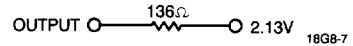
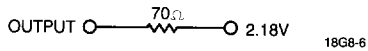
AC Test Loads and Waveforms



18G8-5

Equivalent to: THEVENIN EQUIVALENT (Commercial)

Equivalent to: THEVENIN EQUIVALENT (Military/Industrial)



Configuration Table<sup>[5]</sup>

| C <sub>3</sub> | C <sub>2</sub> | C <sub>1</sub> | C <sub>0</sub> | Configuration   |
|----------------|----------------|----------------|----------------|---|
| 0              | 0              | 0              | 0              | Active LOW, Registered Mode, Registered Feedback, Pin 11 OE           |
| 0              | 0              | 0              | 1              | Active HIGH, Registered Mode, Registered Feedback, Pin 11 OE          |
| 0              | 0              | 1              | 0              | Active LOW, Combinatorial Mode, Registered Feedback, Pin 11 OE        |
| 0              | 0              | 1              | 1              | Active HIGH, Combinatorial Mode, Registered Feedback, Pin 11 OE       |
| 0              | 1              | 0              | 0              | Active LOW, Registered Mode, Registered Feedback, Product Term OE     |
| 0              | 1              | 0              | 1              | Active HIGH, Registered Mode, Registered Feedback, Product Term OE    |
| 0              | 1              | 1              | 0              | Active LOW, Combinatorial Mode, Registered Feedback, Product Term OE  |
| 0              | 1              | 1              | 1              | Active HIGH, Combinatorial Mode, Registered Feedback, Product Term OE |
| 1              | 0              | 0              | 0              | Active LOW, Registered Mode, Pin Feedback, Pin 11 OE                  |
| 1              | 0              | 0              | 1              | Active HIGH, Registered Mode, Pin Feedback, Pin 11 OE                 |
| 1              | 0              | 1              | 0              | Active LOW, Combinatorial Mode, Pin Feedback, Pin 11 OE               |
| 1              | 0              | 1              | 1              | Active HIGH, Combinatorial Mode, Pin Feedback, Pin 11 OE              |
| 1              | 1              | 0              | 0              | Active LOW, Registered Mode, Pin Feedback, Product Term OE            |
| 1              | 1              | 0              | 1              | Active HIGH, Registered Mode, Pin Feedback, Product Term OE           |
| 1              | 1              | 1              | 0              | Active LOW, Combinatorial Mode, Pin Feedback, Product Term OE         |
| 1              | 1              | 1              | 1              | Active HIGH, Combinatorial Mode, Pin Feedback, Product Term OE        |

Notes:

5. In the virgin or unprogrammed state, a configuration bit is in the "0" state.

Switching Characteristics Over the Operating Range<sup>[1, 6, 7]</sup>

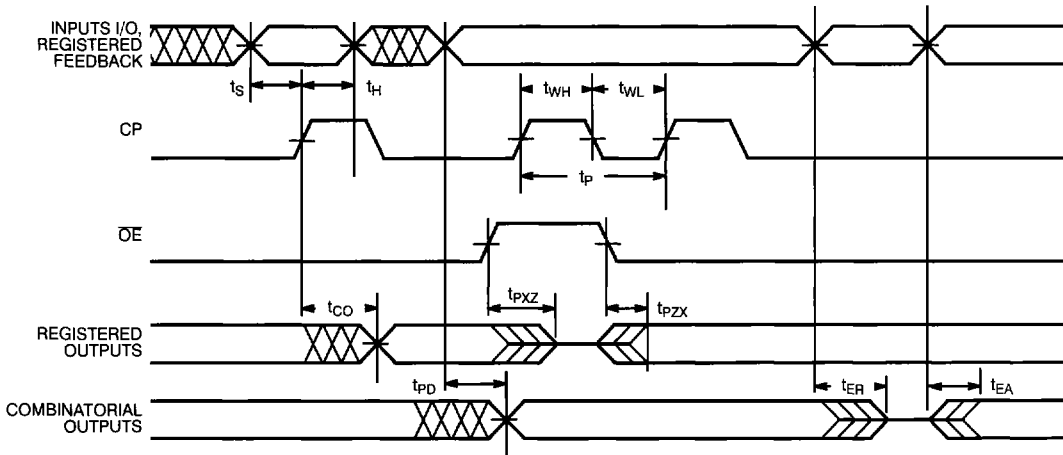
| Parameters      | Description                                | Commercial |      |           |      | Military/Industrial |      |      |      | Units |
|-----------------|--|------------|------|-----------|------|---------------------|------|------|------|-------|
|                 |  | -12        |      | -15, -15L |      | -15                 |      | -20  |      |       |
|                 |  | Min.       | Max. | Min.      | Max. | Min.                | Max. | Min. | Max. |       |
| $t_{PD}$        | Input or Feedback to Non-Registered Output |            | 12   |           | 15   |                     | 15   |      | 20   | ns    |
| $t_{EA}$        | Input to Output Enable                     |            | 12   |           | 15   |                     | 15   |      | 20   | ns    |
| $t_{ER}$        | Input to Output Disable                    |            | 12   |           | 15   |                     | 15   |      | 20   | ns    |
| $t_{PZX}$       | Pin 11 to Output Enable                    |            | 10   |           | 12   |                     | 12   |      | 15   | ns    |
| $t_{PXZ}$       | Pin 11 to Output Disable                   |            | 10   |           | 10   |                     | 10   |      | 15   | ns    |
| $t_{CO}$        | Clock to Output                            |            | 10   |           | 12   |                     | 12   |      | 15   | ns    |
| $t_S$           | Input or Feedback Set-Up Time              | 10         |      | 12        |      | 12                  |      | 15   |      | ns    |
| $t_H$           | Hold Time                                  | 0          |      | 0         |      | 0                   |      | 0    |      | ns    |
| $t_{p[8]}$      | Clock Period                               | 22         |      | 24        |      | 27                  |      | 35   |      | ns    |
| $t_{WH}$        | Clock High Time                            | 7          |      | 8         |      | 9                   |      | 10   |      | ns    |
| $t_{WL}$        | Clock Low Time                             | 8          |      | 9         |      | 10                  |      | 11   |      | ns    |
| $f_{MAX}^{[9]}$ | Maximum Frequency                          | 50.0       |      | 41.6      |      | 41.6                |      | 33.3 |      | MHz   |

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Notes:

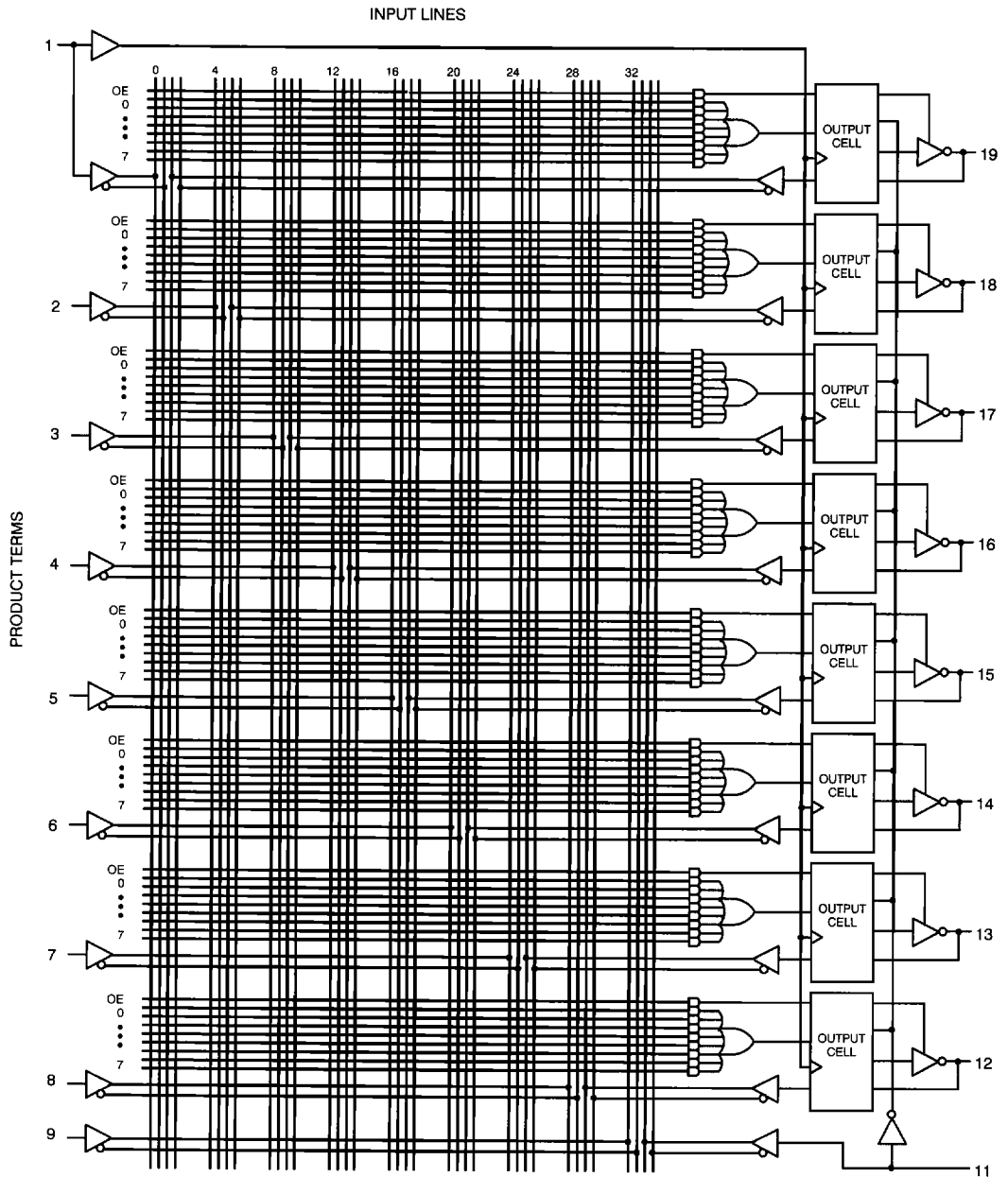
- Part (a) of AC Test Loads and Waveforms is used for all parameters except  $t_{ER}$ ,  $t_{PZX}$ , and  $t_{PXZ}$ . Part (b) of AC Test Loads and Waveforms is used for  $t_{ER}$ ,  $t_{PZX}$ , and  $t_{PXZ}$ .
  - The parameters  $t_{ER}$  and  $t_{PXZ}$  are measured as the delay from the input disable logic threshold transition to  $V_{OH} - 0.5V$  for an enabled HIGH output or  $V_{OL} + 0.5V$  for an enabled LOW input.
  - $t_H$  or minimum guaranteed clock period, is the clock period guaranteed for state machine operation and is calculated from  $t_p = t_S + t_{CO}$ .
- The minimum guaranteed period for registered data path operation (no feedback) can be calculated as the greater of  $(t_{WH} + t_{WL})$  or  $(t_S + t_H)$ .
- $f_{MAX}$ , or minimum guaranteed operating frequency, is the operating frequency guaranteed for state machine operation and is calculated from  $f_{MAX} = 1/(t_S + t_{CO})$ . The minimum guaranteed  $f_{MAX}$  for registered data path operation (no feedback) can be calculated as the lower of  $1/(t_{WH} + t_{WL})$  or  $1/(t_S + t_H)$ .

Switching Waveform



18G8-8

Functional Logic Diagram



**Ordering Information**

| ICC (mA) | Speed (ns) | Ordering Code  | Package Name | Package Type                                 | Operating Range |
|----------|------------|----------------|--------------|--|-----------------|
| 90       | 12         | PLDC18G8-12JC  | J61          | 20-Lead Plastic Leaded Chip Carrier          | Commercial      |
|          |            | PLDC18G8-12PC  | P5           | 20-Lead (300-Mil) Molded DIP                 |                 |
|          |            | PLDC18G8-12VC  | V5           | 20-Lead (300-Mil) Molded SOJ                 |                 |
|          |            | PLDC18G8-12WC  | W6           | 20-Lead (300-Mil) Windowed CerDIP            |                 |
| 70       | 15         | PLDC18G8L-15JC | J61          | 20-Lead Plastic Leaded Chip Carrier          | Commercial      |
|          |            | PLDC18G8L-15PC | P5           | 20-Lead (300-Mil) Molded DIP                 |                 |
|          |            | PLDC18G8L-15VC | V5           | 20-Lead (300-Mil) Molded SOJ                 |                 |
|          |            | PLDC18G8L-15WC | W6           | 20-Lead (300-Mil) Windowed CerDIP            |                 |
| 90       | 15         | PLDC18G8-15JC  | J61          | 20-Lead Plastic Leaded Chip Carrier          | Commercial      |
|          |            | PLDC18G8-15PC  | P5           | 20-Lead (300-Mil) Molded DIP                 |                 |
|          |            | PLDC18G8-15VC  | V5           | 20-Lead (300-Mil) Molded SOJ                 |                 |
|          |            | PLDC18G8-15WC  | W6           | 20-Lead (300-Mil) Windowed CerDIP            |                 |
| 110      | 15         | PLDC18G8-15JI  | J61          | 20-Lead Plastic Leaded Chip Carrier          | Industrial      |
|          |            | PLDC18G8-15PI  | P5           | 20-Lead (300-Mil) Molded DIP                 |                 |
|          |            | PLDC18G8-15WI  | W6           | 20-Lead (300-Mil) Windowed CerDIP            |                 |
| 110      | 15         | PLDC18G8-15DMB | D6           | 20-Lead (300-Mil) CerDIP                     | Military        |
|          |            | PLDC18G8-15LMB | L61          | 20-Pin Square Leadless Chip Carrier          |                 |
|          |            | PLDC18G8-15QMB | Q61          | 20-Pin Windowed Square Leadless Chip Carrier |                 |
|          |            | PLDC18G8-15WMB | W6           | 20-Lead (300-Mil) Windowed CerDIP            |                 |
| 110      | 20         | PLDC18G8-20JI  | J61          | 20-Lead Plastic Leaded Chip Carrier          | Industrial      |
|          |            | PLDC18G8-20PI  | P5           | 20-Lead (300-Mil) Molded DIP                 |                 |
|          |            | PLDC18G8-20WI  | W6           | 20-Lead (300-Mil) Windowed CerDIP            |                 |
| 110      | 20         | PLDC18G8-20DMB | D6           | 20-Lead (300-Mil) CerDIP                     | Military        |
|          |            | PLDC18G8-20LMB | L61          | 20-Pin Square Leadless Chip Carrier          |                 |
|          |            | PLDC18G8-20QMB | Q61          | 20-Pin Windowed Square Leadless Chip Carrier |                 |
|          |            | PLDC18G8-20WMB | W6           | 20-Lead (300-Mil) Windowed CerDIP            |                 |

**PLDs 4**
**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameters      | Subgroups |
|-----------------|-----------|
| V <sub>OH</sub> | 1, 2, 3   |
| V <sub>OL</sub> | 1, 2, 3   |
| V <sub>IH</sub> | 1, 2, 3   |
| V <sub>IL</sub> | 1, 2, 3   |
| I <sub>IX</sub> | 1, 2, 3   |
| I <sub>OZ</sub> | 1, 2, 3   |
| I <sub>CC</sub> | 1, 2, 3   |

**AC Characteristics**

| Parameters       | Subgroups |
|------------------|-----------|
| t <sub>PD</sub>  | 9, 10, 11 |
| t <sub>PZX</sub> | 9, 10, 11 |
| t <sub>CO</sub>  | 9, 10, 11 |
| t <sub>S</sub>   | 9, 10, 11 |
| t <sub>H</sub>   | 9, 10, 11 |