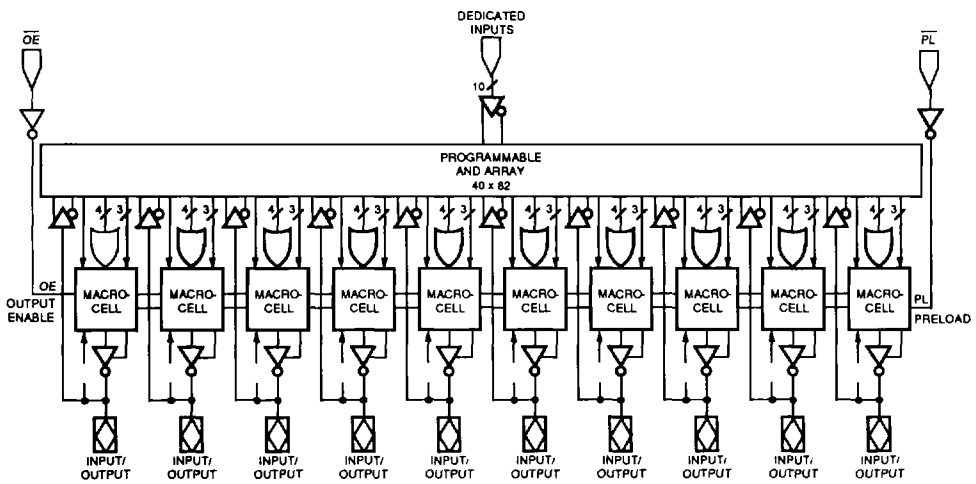
November 1989

## Features

- CMOS EEPLD with Zero Standby Power:
  - 10 µA Typical, 150 µA Maximum
- Operating Power Rises at Less Than 5 mA/MHz
- Propagation Delay: 35, 40 or 45 ns
- Asynchronous Architecture:
  - 10 Output Macro Cells with Individually Programmable Clocks, Preset and Reset Signals
- Individually Programmable and Global Output Enable
- Programmable Output Polarity
- Registers Can Be Bypassed Individually
- Preloadable Output Registers Facilitate Testing
- Quickly and Easily Reprogrammable in All Package Types
- 100 Reprogramming Cycles, Minimum
- Silicon Signature Bit for Design Secrecy
- 100 % Field Programming Yield
- 10 Years Data Retention Guaranteed
- Supported By: ABEL™, CUPL™, PALASM2®, PLDesigner™
- Programmed on Standard PAL® Device Programmers
- Space Saving 0.3" Wide 24-Pin Ceramic/Plastic DIP
- 28-Pin LCC and PLCC Packages in Development

## Block Diagram




ABEL is a trademark of DATA I/O Corporation

PLDesigner is a trademark of Minc Inc.

CUPL is a trademark of Logical Devices Inc.

## General Description

*The 20RA10Z is functionally equivalent to the bipolar PAL20RA10. SEEQ's 20RA10Z consumes significantly less power than its bipolar equivalent: Standby power consumption is typically less than 10 µA; active power rises at less than 5 mA per MHz of operating frequency.*

*Bipolar devices can not be reprogrammed while UV erasable PLDs can be reprogrammed only in windowed, ceramic packages. Electrically erasable device offer reprogrammability without constraints in all package types.*

*Reprogrammability reduces development costs and eliminates the risks involved in preprogramming production quantities. Systems can be updated quickly by reconfiguring the EEPLDs. Reprogrammability helps SEEQ to extensively test the entire device and offer 100% field programming yield.*

*The asynchronous 20RA10Z adds a new dimension to PAL device flexibility. Its unique architecture allows the designer to individually clock, set or reset each of the 10 output macro cells, and to enable/disable each output buffer individually.*

## Functional Description

*The 20RA10Z has ten dedicated input lines and 10 programmable I/0 macrocells. The Registered Asychronous (RA) macrocell is shown on page 3. Pin 1 of the EEPLD serves as global register perload, pin 13 (DIP) or pin 16 (LCC/PLCC) serves as global output enable. The exclusive-OR in every macro cell allows choosing between active high and active low output polarity, and ensures highest possibility utilization of the AND-OR array.*

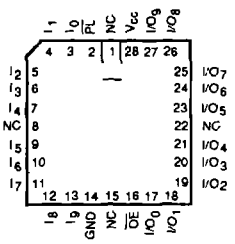
*Thrid party software packages allow users to enter PLD designs on personal computers or engineering workstations. Common input formats are; Boolean Algebra, Truth-Tables, State Diagrams, Wave Forms or schematics. The software automatically converts such specifications into fuse patterns. These files, once downloaded to PAL programmers, configure PLDs according to the user's specifications.*

## Programmability Preset and Reset

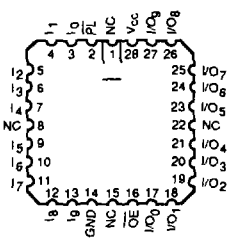
*In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product term is HIGH, the Q output of the register*

## Pin Configuration (Top View)

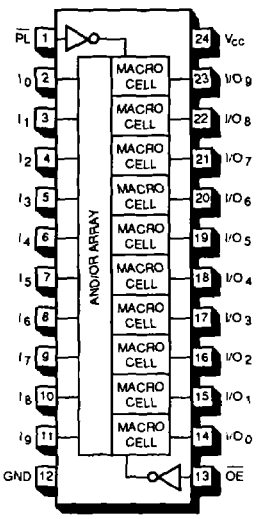
**20RA10Z PLCCPINOUT**




**20RA10Z LCC PINOUT**

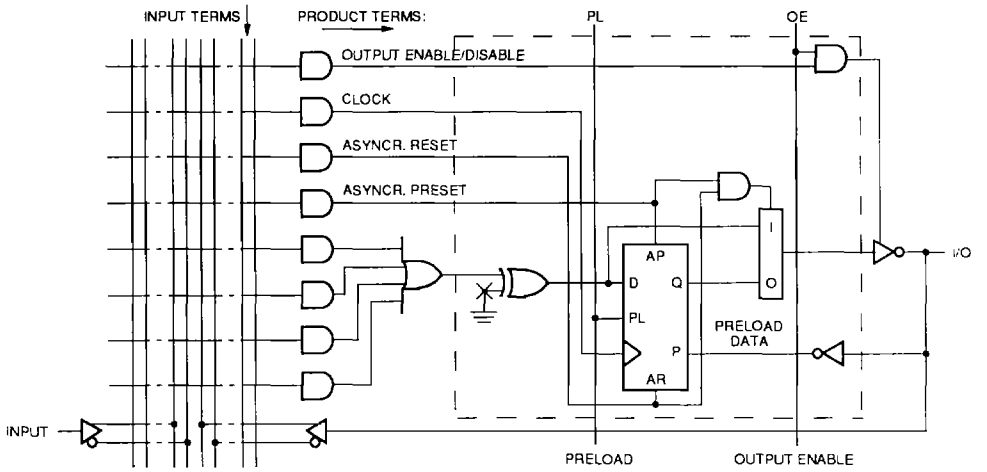



**20RA10Z SLIM DIP PINOUT**




Pin Designations: I = Input
I/O = Input/Output
$\overline{PL}$ = Preload
$\overline{OE}$ = Output Enable
$V_{CC}$ = Supply Voltage
GND = Ground
NC = No Connection

## RA Macrocell Configuration




*becomes logic 1. If the reset product term is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.*

### Programmable Clock

*The clock input to each flip-flop comes from the programmable array, Allowing any flip-flop to be clocked independently if desired.*

### Bypass Mode/Registered Mode

*If both the preset and reset product terms are HIGH, the flip-flop is bypassed (Bypass Mode) and the output becomes combinatorial. Otherwise, the output is from the register (Registered Mode). Each output can be configured to be combinatorial or registered.*

### Programmable Polarity

*The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the 20RA10Z logic diagram. When the output polarity bit is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity bit is unprogrammed, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.*

*The device provides a product term dedicated to local output control. There is a global output control pin. The output is enabled if both the global output oin is LOW ans the local output control product is HIGH, all outputs will be disabled. if the local output control product term is LOW, then that output will be disabled.*

**Remark:** The output buffer inverts the sum of products signal.

### Register Preload

*Register preload allows any arbitrary state to be loaded into the PAL device output registers. This allows complete logic verification, including states that are impossible or impractical to reach otherwise. To use the preload feature, first disable the outputs by bringing $\overline{OE}$ HIGH, and present the data at the output pins. A LOW level on the preload pin ($\overline{PL}$) will then load the data into registers. (See Register Preload Waveform on the bottom of page 11.)*

| $\overline{OE}$ Product Term | $\overline{OE}$ Pin | I/O |
|---|---|---|
| I | O | Indiv. output enabled |
| O | X | Indiv. output disabled* |
| X | I | All outputs disabled* |

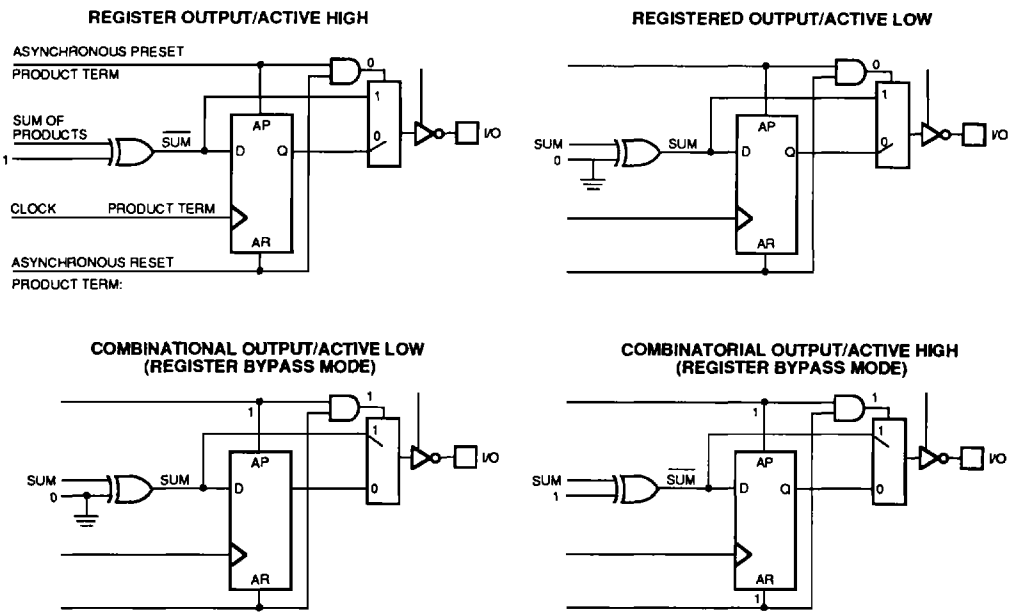
* Output pin(s) floating or used as input(s)

**Note:** Floaating outputs, as well as unused or floating inputs should be pulled HIGH or Low. Otherwise noise , amplified through the feedback paths or input buffers, may constantly trigger the edge defection circuitry within the 20RA10Z and inhibit standby mode.

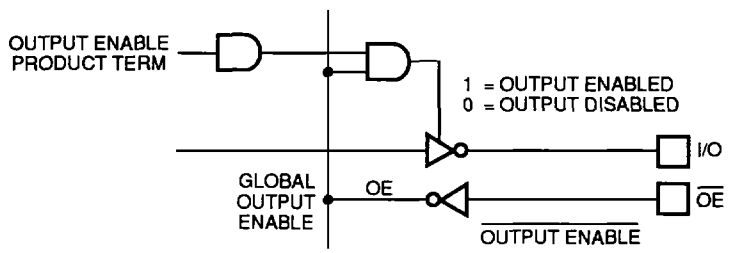
## Security Bit

*A security bit prevents copying of your proprietary design. When this bit is set, the verify data path in the PLD is disabled, making it impossible to copy your pattern. Since EEPLDs store patterns as electrical charges on floating polysilicon gates (and not in blown fuses, like other PLD technologies) it is not possible to determine the pattern by simply examining the die. A copy protected EEPLD can be reused after a block erase, which clears both the previously programmed pattern and the security bit at the same time.*

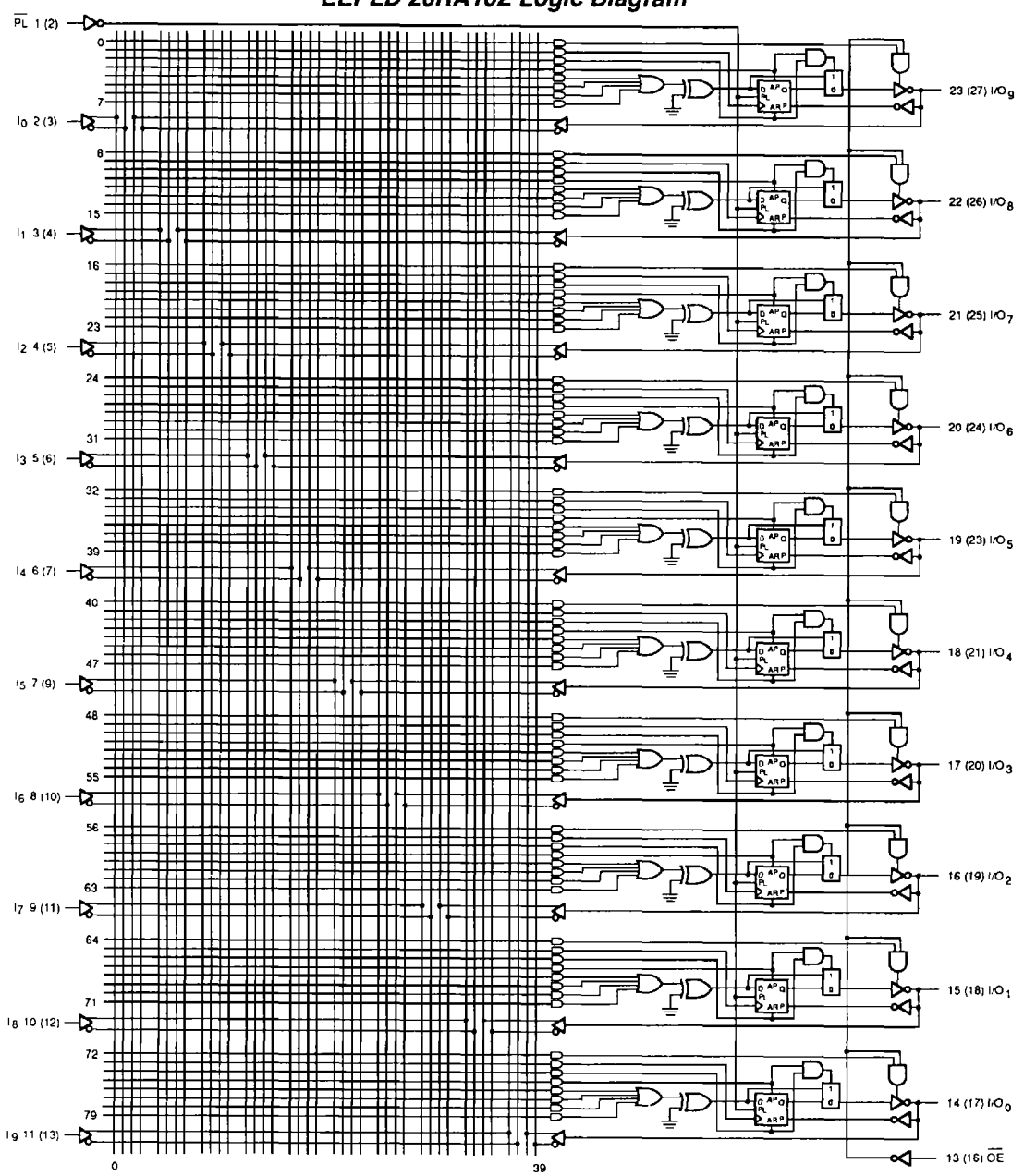
## Output Macrocell Configurations




## Output Buffer with Individually Programmable and Global Output Enable



## EEPLD 20RA10Z Logic Diagram




PIN NUMBERS REFER TO DIP (PLCC PINOUT)

## Absolute Maximum Ratings

*Supply voltage, $V_{CC}$ .. ..... –0.5 V to 7 V*
*DC input voltage, V .. ..... –0.5 V to VCC + 0.5V*
*DC output voltage $V_O$ . ..... –0.5 V to VCC + 0.5 V*
*DC output source/sink .....*
*current per output pin, $I_O$ . ..... ±35 mA*
*DC $V_{CC}$ or ground current, $I_{CC}$ or $I_{GND} \neq 100$ mA*
*Input diode current, $I_{IK}$*
*$V_I < 0$ ..... –20 mA*
*$V_I > V_{CC}$ . ..... +20 mA*
*Output diode current, $I_{OK}$*
*$V_O < 0$ ..... –20 mA*
*$V_O > V_{CC}$ . ..... +20 mA*
*Storage temperature ..... –65°C to 150°C*
*Static discharge voltage ..... > 2001 V*
*Latchup current ..... > 100 mA*
*Ambient Temperature under bias ..... –55°C to +125°C*

*Stresses above those listed under ABSOLUTE MAXIMUM RATING may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## Operating Ranges

*Commercial (Q) Devices*
*Temperature ($T_A$)*
*Operating Free Air ..... 0°C to +75°C*
*Supply voltage, $V_{CC}$ ..... 4.75 V to 5.25 V*
*Industrial (E) Devices*
*Temperature ($T_A$)*
*Case ..... –40°C to +85°C*
*Supply voltage, $V_{CC}$ ..... 4.5 V to 5.5 V*

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC Characteristics (over operating conditions unless otherwise specified)

| Symbol | Parameter | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level Input Voltage | Guaranteed Input Logical Low Voltage for all Inputs[1] | | 0 | 0.8 | V |
| $V_{IH}$ | High-level Input Voltage | Guaranteed Input Logical High Voltage for all Inputs[1] | | 2 | $V_{CC}$ | V |
| $I_{IL}$ | Low-level Input Current | $V_{CC}$ = Max. | $V_I$ =GND | – 1 | | µA |
| $I_{IH}$ | High-level Input Current | $V_{CC}$ = Max. | $V_I = V_{CC}$ | | 1 | µA |
| $V_{OL}$ | Low-level Output Voltage | $V_{CC}$ = Min. | $I_{OL}$ = 8 mA | | 0.5 | V |
| | | $V_{CC}$ = 5V | $I_{OL}$ = 1 µA | | 0.05 | |
| $V_{OH}$ | High-level Output Voltage | $V_{CC}$ = Min. | $I_{OH}$ = – 4.0 mA | 3.80 | | |
| | | $V_{CC}$ = 5V | $I_{OL}$ = –1 µA | 4.95 | | |
| $I_{OZL}$ | Off-state Output Current | VCC =Max. | $V_O$ = GND[4] | –10 | | µA |
| $I_{OZH}$ | | | $V_O = V_{CC}$[4] | | 10 | µA |
| $I_{CC}$ | Standby Supply Current[2] | $I_O$ = 0 mA, $V_I$ = GND or $V_{CC}$ | | | 150 | µA |
| | Operating Supply Current[3] | f = 1 MHz, $I_O$= 0 mA, $V_I$ = GND or $V_{CC}$ | | | 25 | mA |

Notes: 1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Disabled output pins = $V_{CC}$ or GND.
3. Frequency of any input. See gragh page 12 for $I_{CC}$ versus frequency
4. I/O pin leakage is worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OHZ}$).

## Capacitance

| Parameter Symbol | Parameter Description | Test conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance[1] | $V_{IN}$ = 2.0 V at f = 1.0 MHz<br>$V_{CC}$ = 5 V $T_A$ = 25°C | 7 | pF |
| $C_{OUT}$ | Output capacitance[1] | $V_{OUT}$ = 2.0 V at f = 1.0 MHz<br>$V_{CC}$ = 5 V $T_A$ = 25°C | 8 | |

**Note:** 1. Sampled but not 100% tested.

## Switching Characteristics (over commercial operating range[1])

| Symbol | Parameter[2] | | – 35[5] Min. | – 35[5] Max. | – 40 Min. | – 40 Max. | – 45[6] Min. | – 45[6] Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Output | | | 35 | | 40 | | 45 | ns |
| $t_S$ | Setup Time for Input or Feednack to Clock | | 15 | | 20 | | 20 | | ns |
| $t_H$ | Hold Time | | 10 | | 15 | | 15 | | ns |
| $t_{CO}$ | Clock to Output or Feedback[3] | | | 30 | | 40 | | 45 | ns |
| $t_{WP}$ | PreloadPulse Width | | 25 | | 30 | | 30 | | ns |
| $t_{SUP}$ | Preload Setup Time | | 20 | | 25 | | 25 | | ns |
| $t_{HP}$ | Preload Hold Time | | 20 | | 25 | | 25 | | ns |
| $t_{AP}$ | Asynchronous Preset to Registered Output[3] | | | 35 | | 45 | | 45 | ns |
| $t_{APW}$ | Asynchronous Preset Pulse Width | | 25 | | 25 | | 30 | | ns |
| $t_{APR}$ | Asynchronous Preset Recovery Time | | 10 | | 15 | | 15 | | ns |
| $t_{WL}$ | Width of Clock | LOW | 15 | | 20 | | 20 | | ns |
| $t_{WH}$ | | *HIGH* | 15 | | *20* | | *20* | | *ns* |
| $f_{MAX}$ | Maximum | Extenal Feedback $1/t_S = t_{CO}$) | 22.2 | | 16.6 | | 15.3 | | MHz |
| | Frequency | No Feedback $1/(t_{WL} = t_{WH})$ | 33.3 | | 25 | | 25 | | MHz |
| $t_{PZX}$ | Common Enable to Output Buffer Enabled | | | 20 | | 25 | | 30 | ns |
| $t_{PXZ}$ | Common Enable to Output Buffer Disabled | | | 20 | | 25 | | 30 | ns |
| $t_{EA}$ | Input to Output Buffer Enabled[4] | | | 30 | | 40 | | 45 | ns |
| $t_{ER}$ | Input to Output Buffer Disabled[4] | | | 30 | | 40 | | 45 | ns |

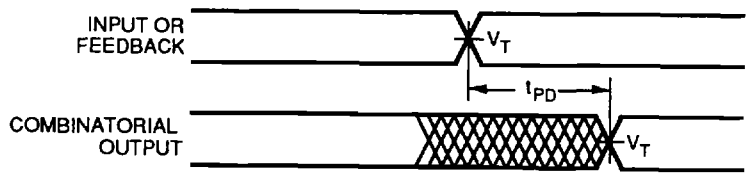
**Note:**
1. The 20RA10Z is designed for the full military operating range. Contact your nearest SEEQ representative for availability information and for specifications of industrial and military devices.
2. Test conditions are specified in table on page 12.
3. Minimum values of these parameters are guaranteed to be larger than the hold time $t_H$.
4. Equivalent functions to $t_{PZX}/t_{PXZ}$ but using product term control.
5. Preliminary specification.
6. *The 20RA10Z-45 is available and specified for commercial and industrial operating conditions.*

**Remarks:** All specified input-to-output delays include the time it takes the input edge detection circuitry to activate the device (from standby mode into operating mode).

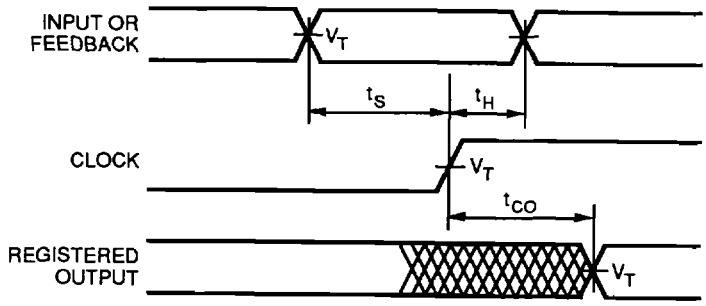
## Data Retention and Endurance

| Symbol | Parameter | Value | Unit | Conditions |
|---|---|---|---|---|
| $t_{DR}$ | Pattern data retention time | > 10 | years | Max. storage temperature<br>Mil-STD 883 Test Method 1008 |
| N | Min. reprogramming cycles | 100 | cycles | Operating conditions |

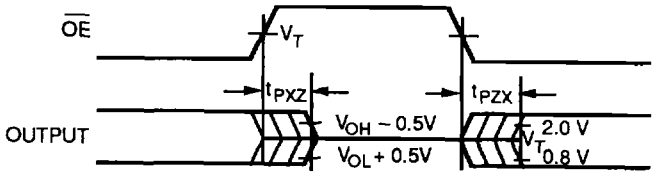
## Switching Waveforms



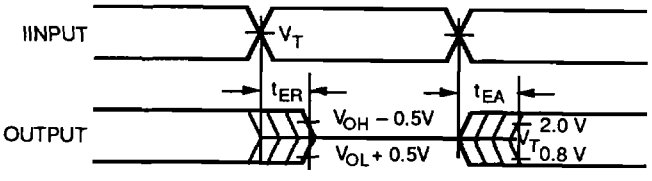

**COMBINATORIAL OUTPUT (BYPASS MODE)**




**REGISTERED OUTPUT (REGISTERED MODE)**

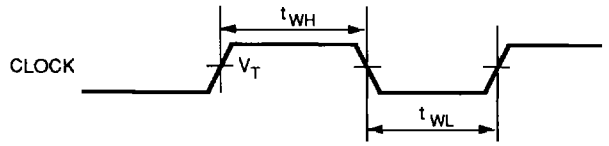



**COMMON ENABLE ($\overline{OE}$) TO OUTPUT DISABLE/ENABLE**

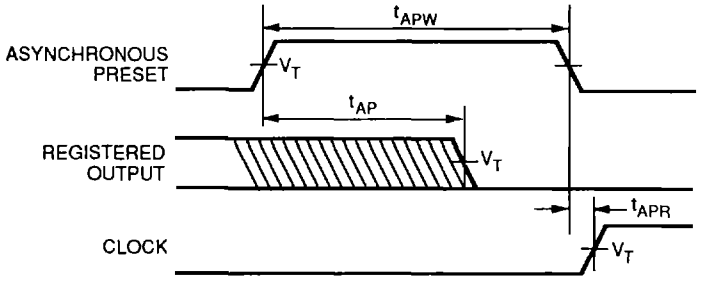



**INPUT TO OUTPUT DISABLE/ENABLE**

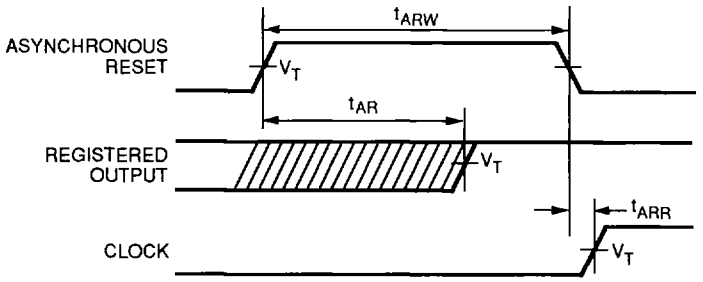
## Switching Waveforms (continued)



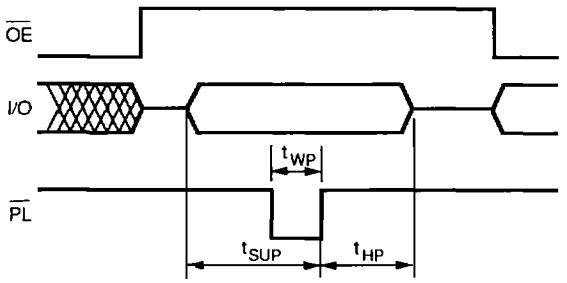

CLOCK WIDTH




ASYNCHRONOUS PRESET



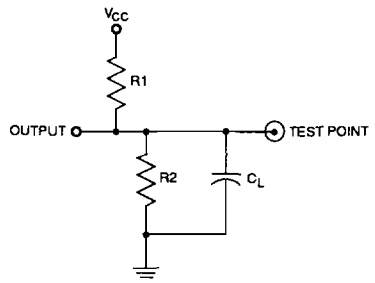

ASYNCHRONOUS RESET




PRELOAD TIMING

EEPLD

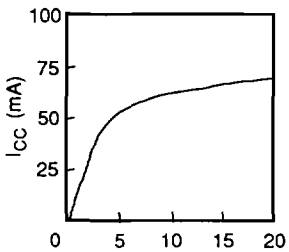
## Switching Test Laod




| Specification | $C_L$ | $R_1$ | $R_2$ | Measured Output Value |
|---|---|---|---|---|
| $t_{IL}$,$t_{CO}$ | 50 pF | 440Ω | 190Ω | 1.5V |
| $t_{PZX}$, $t_{EA}$ | 50 pF | 440Ω | 190Ω | Z–H: 2.0V<br>Z–L: 0.8V |
| $t_{PXZ}$, $t_{ER}$ | 5pF | 440Ω | 190Ω | H – Z: $V_{OH}$ –0.5 V<br>L – Z: $V_{OL}$ + 0.5V |

## $I_{cc}$ Versus Frequency

TYPICAL: $V_{CC}$ = 5V, $T_A$ = 25°C




## Key to Timing Diagrams

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | DON'T CARE:<br>CHANGE PERMITTED | CHANGING:<br>STATE UNKNOWN |
| | NOT APPLICABLE | CENTER LINE IS<br>HIGH IMPEDANCE STATE |
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM<br>H TO L | WILL BE CHANGING<br>FROM H TO L |
| | MAY CHANGE FROM<br>L TO H | WILL BE CHANGING<br>FROM L TO H |

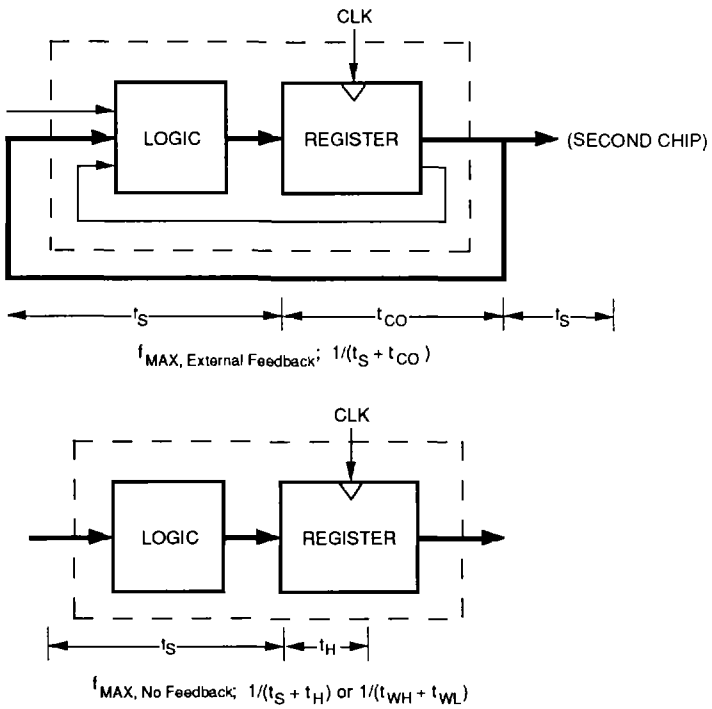
**Notes:**
1. $V_T$ = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2 – 5 ns typical

## $f_{MAX}$ Parameters

*The parameters $f_{MAX}$ is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, $f_{MAX}$ is specified in this case for two types of synchronous designs.*

*The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, $f_{MAX}$, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This $f_{MAX}$ is designated "$f_{MAX}$, External Feedback."*

*The second type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each $f_{MAX}$ type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the second $f_{MAX}$, designated "$f_{MAX,\ No\ feedback}$."*



## PLD Development

*Development software assists the user in implementing a design in one or several PLDs. The software converts the user's input into a device dependent fuse map in JEDEC format. The software packages listed below support the 20RA10Z EEPLD. For more information about PLD development software contact SEEQ Technology or the software vendor directly:*

***DATA I/O Corp.***
*10525 Willows Road, NE, P.O. Box 97046,*
*Redmont, WA 98073-9746*
*(800) 247-5700*
*Software offered: ABEL, PLD Test*

***Minc. Incorporated***
*1575 York Road, Colorado Springs, CO 80918*
*(719) 590-1155*
*Software offered: PLDesigner*

***Logical Devices, Inc.***
*1021 N.W. 65th Place, Fort Lauderdale, FL 33309*
*(305) 974-0967*
*Software offered: CUPL*

## PLD Programming

*The 20RA10Z can be programmed on standard logic programmers. Previously programmed devices can be reprogrammed easily, using exactly the same procedure as required for blank EEPLDs. If the user wants to erase a 20RA10Z, but not program it to a new pattern, an empty JEDEC file should be loaded into the device programmer.*

## PLD Programmer Vendors

***Adams MacDonald***
*800 Airport Road, Monterey, CA 93940*
*(408) 373-3607*

***DATA I/O Corp.***
*10525 Willows Road NE, P.O. Box 97046*
*Redmont, WA 98073-9746*
*(800) 247-5700*
*PLD Programming equipment:*
*System 29A or 29B*
*Logic Pak™ 303A-V04*
*Adaptor 303-011A for 24 pin DIP*
*303-011B for 28 pin PLCC*
*Family Pinout Code for 20RA10Z: 9E/45*

***Digilec Inc.***
*22736 Vanowen, Canoga Park, CA 91307*
*(800) 367-8750; CA: (818) 887-3755*

***Logical Devices Inc.***
*1201 N.W. 65th Place, Fort Lauderdale, FL 33309*
*(305) 974-0967*

***PROMOC***
*see Adams MacDonald*

***Stag Microsystems Inc.***
*1600 Wyatt Dr., Santa Clara CA 95054*
*(408) 988-1118*

*For more information about PLD programmers contact SEEQ Technology or the programmer vendor directly.*

Logic Pak is a trademark of DATA I/O Corporation.

## Ordering Information